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This Issue's Technology Perspective: Dual-Port RAMs

A dual-port RAM is a random-access memory that can be accessed simultaneously by two independent entities. This implies a dual-port memory *cell* in which both ports can be accessed simultaneously, using two independent sets of address, data, and control lines.

Early computers used the contents of a memory location as one operand and an accumulator in the CPU as the second operand. The results were usually stored in the accumulator. The first multiport memories were probably used in the CPU of the first computers; many two-operand instructions are efficiently implemented using dual-port registers for the operands and the result.

The 74181 was the first IC ALU. In it, two 4-bit operands are operated upon according to a 4-bit command, and the result is output. The 74181 is a combinatorial device and provides no storage. The MMI 67901 was the first 4-bit slice that brought sixteen 4-bit registers onto the chip. It was second-sourced by AMD, becoming the 2901. At one time, five vendors offered this industry-standard bipolar ALU. The Cypress CMOS CY7C901 is the highest-performance, TTL-compatible, 4-bit-slice workalike; it has a 16-word-deep, 4-bit-wide register array that is functionally equivalent to a 16 × 4 dual-port memory.

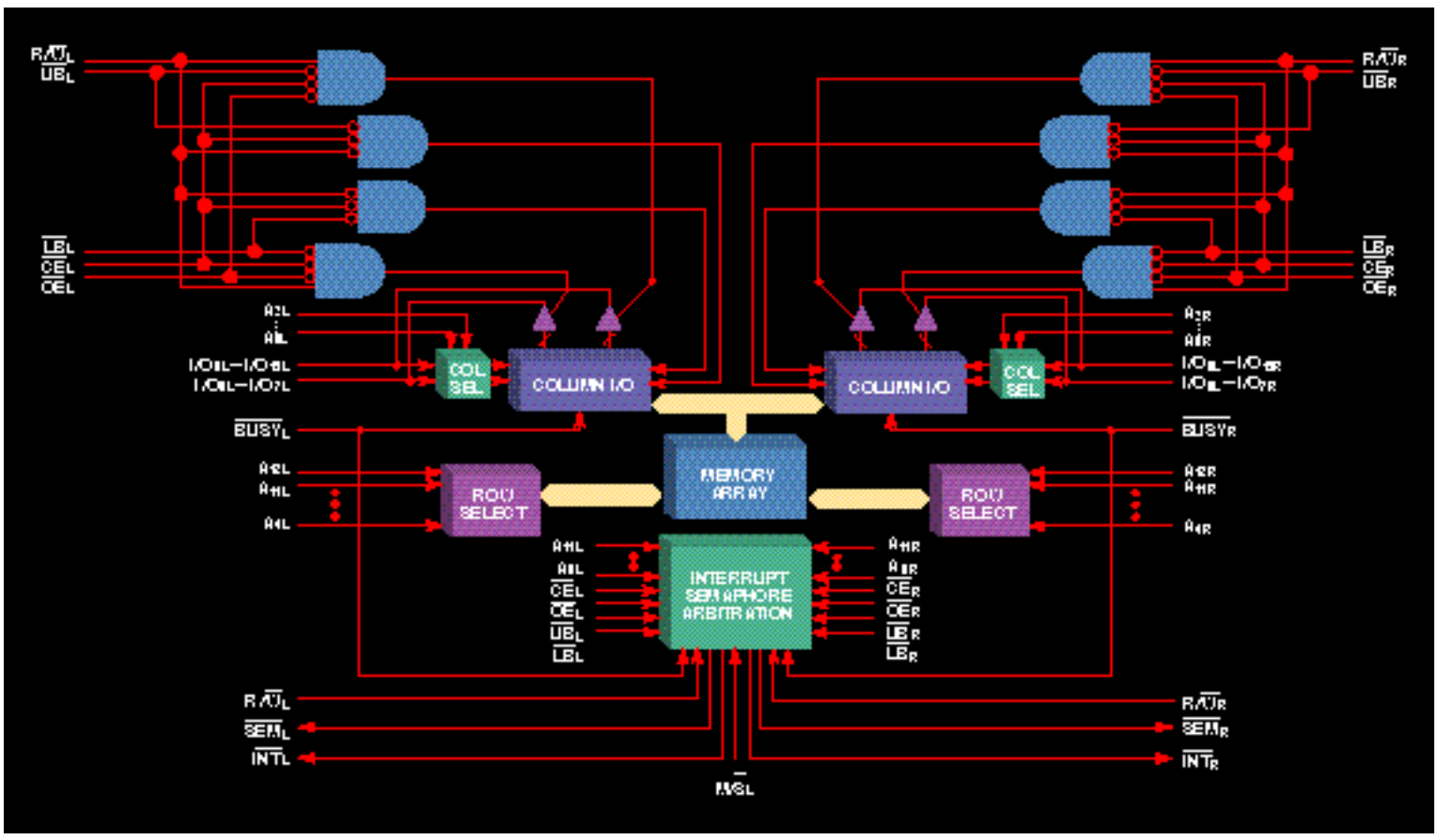
Before the dual-port memory cell existed, designers created dual-port RAMs from single-port RAMs by adding a multiplexer between the RAM and the two entities that shared it. The first applications for dual-port memories were for CPU register files. They can also serve as cache memories for data or instructions. However, the largest usage of dual-port RAMs is in communications, which includes the exchange of data between processors, processes, and systems.

Communication between systems does not require physical dual-port RAMs. Instead, a conventional RAM memory can be partitioned into virtual data-storage areas, or buffers, usually storing at least two data packets. The buffers are shared between the communications controller and the intelligent element that assembles the packets and stores them—usually a microprocessor. If the system contains only one processor, however, the data buffers are not shared and the system needs neither a virtual nor a physical dual-port RAM.

The first dual-port RAM ICs to use a dual-port RAM cell were introduced in 1983, by Synertek. Even the original dual-port RAMs included two mailboxes for message passing. The concept of a "slave" companion was introduced in 1985, as a means to expand word width under control of a "master."

Most of the dual-port RAMs on the market today are functionally equivalent to the original Synertek products. Some, however, include significant new features, among them the dedicated semaphore registers used by Cypress dual-ports to provide efficient means of allocating exclusive priority accesses to blocks of shared memory locations. ❖

To learn more about dual-port RAMs, read the Technology Perspective *starting on page 4.*



Inner workings. The left-right symmetry of a dual-port RAM calls for left (L) and right (R) sets of address, data, and control signals. Address inputs (A_0, A_1, . . .), are unidirectional into the device; their states specify the memory location to be read from or written to. Data pins (I/O_0, I/O_1, . . .) are bidirectional; their states represent either data to be written or data to be read. Besides such standard control signals as chip enable (CE), read/write (R/W), and output enable (OE), plus interrupt (INT) and BUSY flags, some dual-ports have a semaphore-enable (SEM) control pin; semaphores permit software handshaking between ports.

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