Warp2™ Release 4—Awesome Synthesis Power for Just $99!

Warp2 Release 4 is a design tool with unmatched synthesis capability. It now supports all of Cypress's programmable logic offerings, from SPLDs to MAX340™ CPLDs to UltraLogic™ FLASH370i™ CPLDs and pASIC380™ FPGAs. The new release improves synthesis efficiency and adds FPGA support to the previous version's PLD and CPLD support. No other tool in the industry has so much power for such a low price—just $99.

Automatic module synthesis

Warp2 now incorporates leading-edge UltraGen™ module generation. UltraGen technology automatically searches your design's VHDL source code for complex arithmetic and datapath operators (e.g., the plus operator). It then generates an implementation of the appropriate width, consisting of a handcrafted circuit already optimized for the architecture of your target device.

For example, if your VHDL listing has a line that reads "A ≥ B + C," and B and C are defined as 16-bit signals, *Warp2* will go to a special library and choose the optimal 16-bit adder module specific to the target. The module from the library will be generated automatically, without explicit intervention by you.

GUI intuitive, fast

Warp2 Release 4 is easier to use because the new graphical user interface (GUI) is intuitive and very fast. It will boost your productivity because it gives you more control of the synthesis process than before. Such control is a desired feature in a high-end tool, yet it is still absent in many tool offerings regardless of their price.

Optimize for speed, area

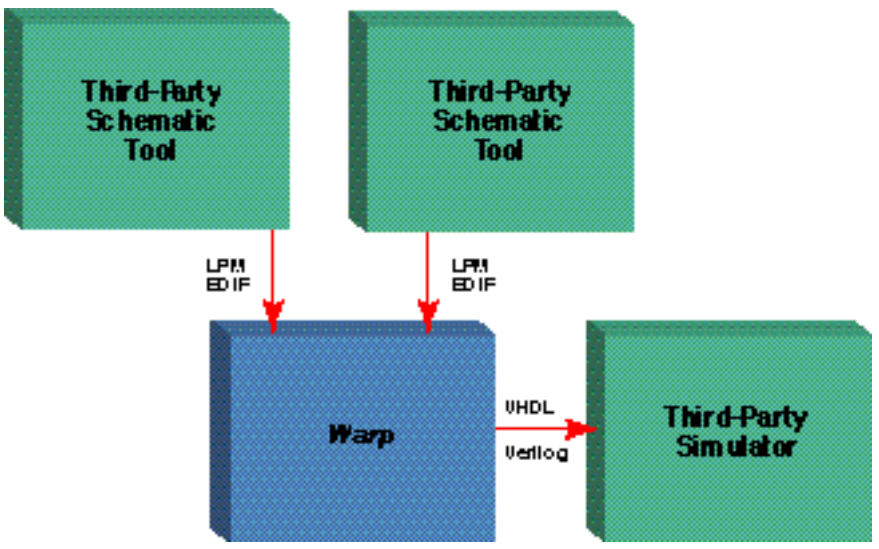
You can control the module-generation capability through directives you supply. This lets you implement modules optimized for minimum silicon area or, if superior performance is desired, generate alternative modules optimized for speed. Further, you can optimize some portions of the design for speed and other portions for area. You can even intervene to optimize selected signals manually, in situations where synthesis just doesn't quite do the job.

Such directive-driven synthesis allows you to tailor a design solution to the special needs of an application. Control of synthesis directives plus UltraGen module-generation technology lets you arrive at more-cost-effective, higher-performance design solutions—without the manual intervention sometimes required by other programmable logic tools. In fact, for behavioral VHDL design entry, the new release of *Warp2* offers a level of synthesis control previously unattainable.

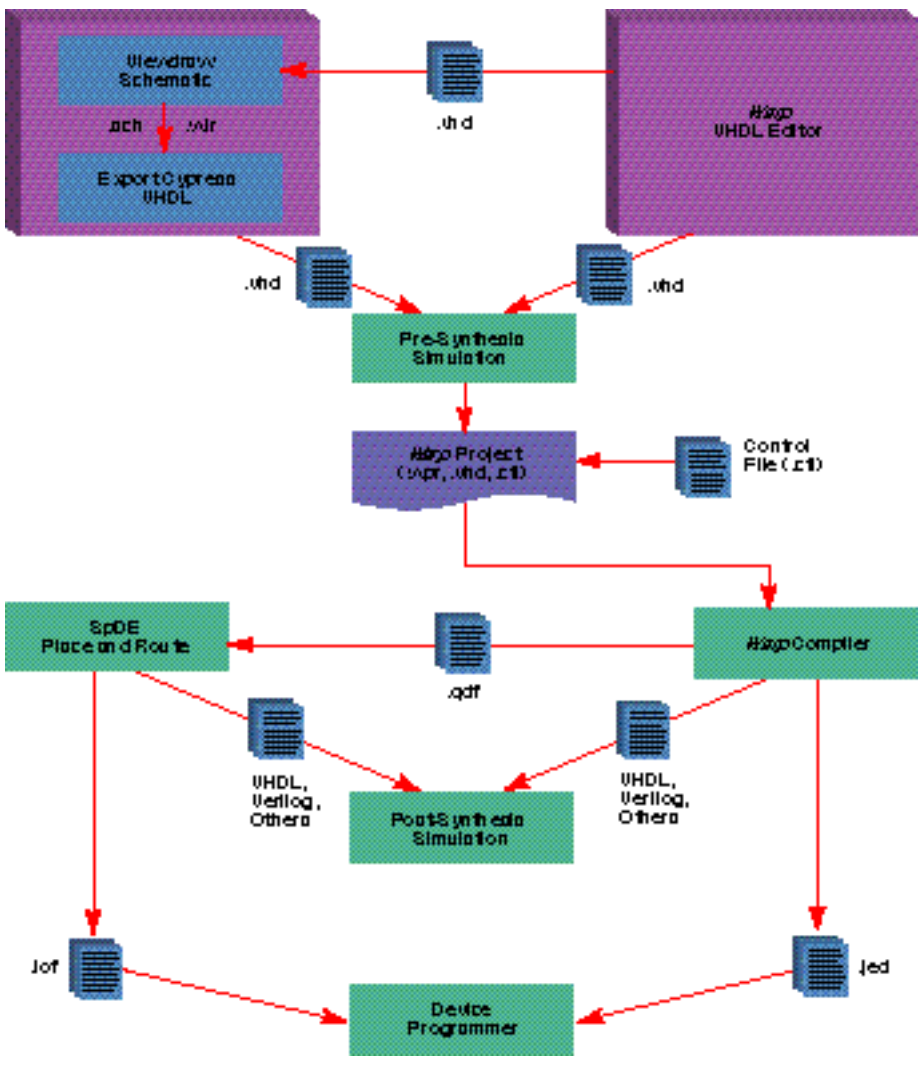
IEEE-standard simulator support

Warp2 also generates and outputs simulation models that are compatible with many third-party simulation environments. *Warp2* can now generate IEEE 1076/1164-compliant VHDL models, with timing, for all Cypress devices, for simulation with VHDL simulation tools from companies such as Mentor, Viewlogic, ModelT, Synopsys, and Cadence.

Warp2 can also generate IEEE 1364-compliant Verilog timing models, which will work with Verilog simulators from Cadence, Viewlogic, and Intergraph. This allows you to perform multiple-component, board-level simulation in an environment other than *Warp2*.



Big on LPM. Warp2 makes extensive use of the Library of Parameterized Modules (LPM), an EIA-standard way of defining components. (For example, an LPM counter's parameters, definable on Warp2's GUI, include width, loadability, count direction, presence/absence of output enables.) Besides an intuitive user interface, LPM provides portability of designs across CAE and synthesis tools. The diagram here shows design entry into Warp2 from third-party schematic or synthesis tools as LPM EDIF (Electronic Data Interchange Format) files, which Warp2 ultimately outputs as a VHDL Verilog file to a third-party simulator.



New design flow. Warp2 Release 4 accepts design entries as behavioral VHDL, VHDL Booleans, or structural VHDL. Compilation starts with a synthesis that makes use of UltraGen automatic module-generation technology. The synthesis output path splits into two parts—one for PLDs/CPLDs, which are fitted into the target device, the other for FPGAs, which use a place-and-route tool. For programming the target device, compilation ultimately produces a JEDEC file for PLDs/CPLDs or a .LOF file for FPGAs. Design verification includes waveform simulation, path timing analysis, and integration with third-party VHDL and Verilog simulators. Device programming is via third-party programmers or Cypress's Impulse3™ programmer.

Design entry

Warp2 captures a design as an IEEE 1076/1164-compliant VHDL text file that can contain a high level behavioral description and/or a Boolean description of the design function. The design may also include a structural VHDL file. The latter describes a portion of the design as a netlist of VHDL library components that you have previously designed, debugged and compiled. By allowing extensive re-use of previous design modules, the structural VHDL design mode can increase your productivity considerably. It also allows the implementation of multiple levels of hierarchy, necessary in a top-down design methodology, and supports a team approach to design of complex systems.

Because *Warp2* is IEEE 1076/1164 VHDL-compliant, you can use any design source file created in *Warp2* as a design entry source for any IEEE-compliant VHDL design tool. Such design portability makes later conversion of a PLD-based design to a mask-programmed ASIC a straightforward task. It also makes comparative evaluation of multiple PLD/CPLD/FPGA design alternatives a painless exercise. You are no longer forced to use a single device architecture for every application regardless of suitability.

Design compilation

The design description next passes to the compiler, in which it is synthesized and mapped to a target device. This step produces as outputs the appropriate device programmer files (JEDEC for CPLDS, .LOF for FPGAS) plus timing models that can be used by any IEEE-compliant VHDL or Verilog simulator.

Synthesis

Synthesis is the process by which the behavioral VHDL design description is converted into an equivalent logic representation that can be mapped to the target device. The synthesized logic representation can be generic, or you can design it to achieve specific area or speed objectives in a given target device architecture.

The synthesis process should be adjustable and should proceed in a manner that achieves your design objectives most effectively for the chosen architecture. *Warp2* UltraGen module-generation synthesis accomplishes this through directive-driven, architecture-specific synthesis. It provides menu-selectable options to input application objectives for speed and area efficiency, and it produces the most efficient logic implementation for mapping to your chosen target device.

Fitting/place-and-route

Optimization removes any logic redundancy or logic transformation that would result in reduced logic usage in the chosen target device.

In the final compilation step, the tailored, synthesized logic description is mapped to the specific device selected; the various design elements are placed in the target device in a manner consistent with the synthesis objectives; and the final interconnect routing is defined. The latter step is called fitting for CPLDS and place-and-route for FPGAS.

Design verification

Once *Warp2* achieves the specific device configuration, it creates the appropriate device programming file. An IEEE 1164 VHDL or IEEE 1364 Verilog simulation model is also created, for inclusion in a full system timing simulation. In addition, *Warp2* provides you with a functional simulator having graphical waveform output, plus waveform editing of the simulation stimulus file.

Unprecedented power for $99

In sum, *Warp2* Release 4 brings an unprecedented degree of VHDL design power for programmable logic into the realm of inexpensive, shrink-wrapped software. It frees you from the prior limitations of rudimentary, generic synthesis that is fundamentally unsuited for mapping designs to diverse programmable logic architectures. Moreover, support for the latest IEEE VHDL language standards and simulation model standards allows *Warp2* to be easily used in a custom design scheme that incorporates other popular design and verification tools.

Warp2 Release 4 runs on PCS under DOS/Windows 3.1, Windows 95, and Windows NT; on Suns under Sun OS 4.x and Solaris 2.5; and on HP machines under HP-UX. ❖

For literature, visit the Cypress web site. See the appropriate site address (URL) for article 201 in the listing on the back cover.