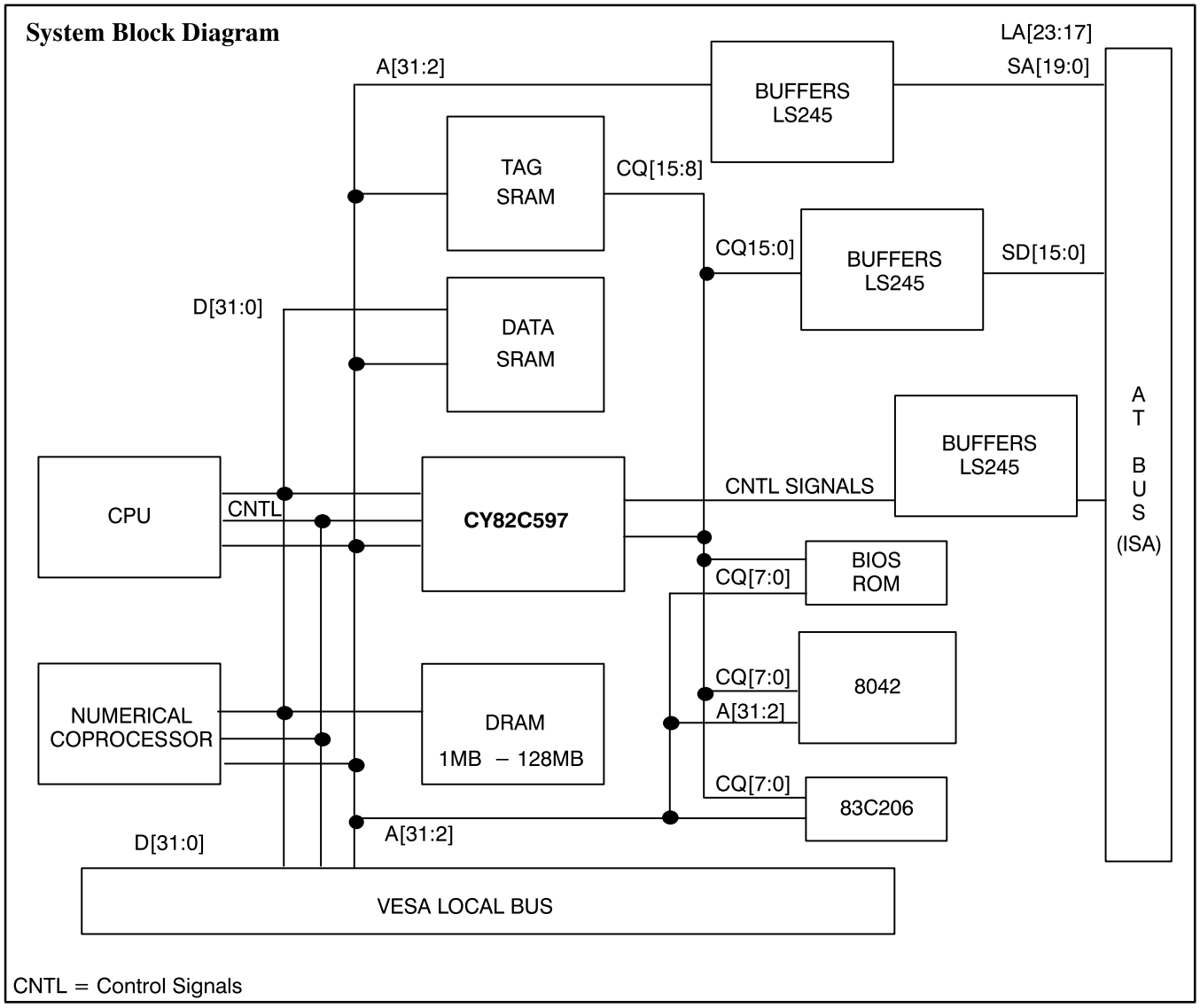
PRELIMINARY **CY82C597**

386/486 Green Chip Set

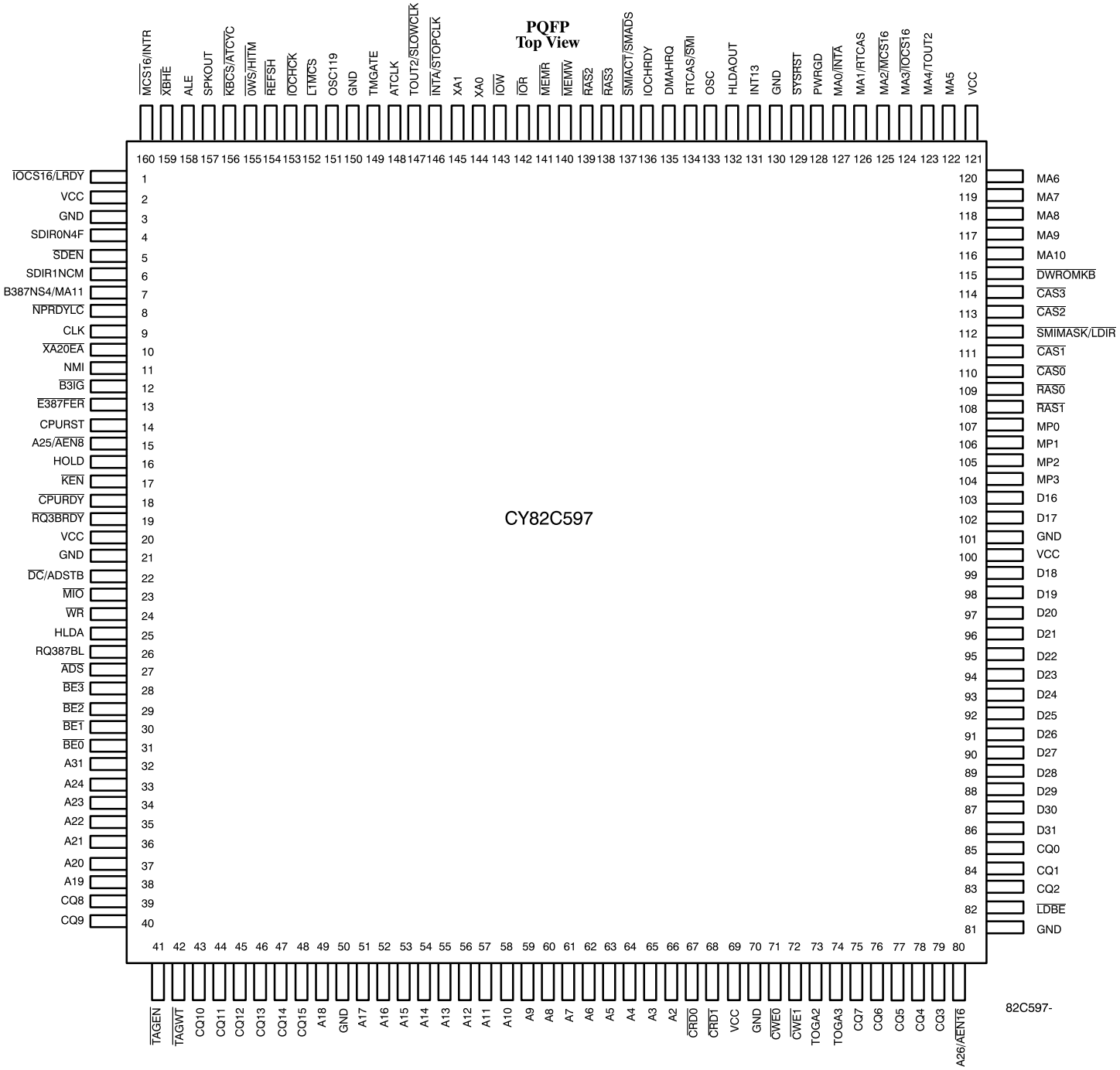
Features

- **160-Pin single chip PQFP**
- **Supports PC/AT compatible systems at 25/33/40/50 MHz**
- **Supports AMD, Cyrix level 1 write-back CPU**
- **Write-Back/Write-Through cache with 32KB/64KB/128KB/256KB/512KB/1MB cache size**
- **Non-cachable memory range support**
- **Full VESA Local Bus support. No PAL needed for VESA master mode**
- **Built-in tag address comparator for lower cost and performance enhancement**
- **Page mode DRAM controller supports mixture of 256KB/512KB/1MB/2MB/4MB/16MB devices**
- **Additional DRAM memory can be supported on the AT bus or VESA bus**
- **Supports up to 128MB of DRAM on the motherboard**
- **Shadow RAM support**
- **Memory A,B,D, and E (256KB total) can be remapped to the top of the memory space**
- **Deep Green support −hardware or software Power-down mode**
- **Unlimited system state: full speed, stand-by, suspend and any number of user-defined states**
- **Microsoft® APM support**
- **11 event detectors and 5 user-defined timers**
- **Standard AT refresh and hidden refresh support**
- **Hardware/software TURBO speed control**
- **Fast GATEA20, Fast Reset support**
- **Supports modular design−one motherboard for 386/486/486SX**
- **Supports Intel/AMD/Cyrix 386DX CPU**
- **Supports Intel 486DX/DX2/DX4/SL/SX/P24T, Cyrix Cx486, AMD Am486 CPUs**

System Block Diagram



Pin Configuration



Functional Description

The CY82C597 is a third-generation single chip PC/AT chip set featuring:

- **Single 160-pin gate array − means lower cost**
- **Higher performance − Write-back cache gives you true 0 wait state read/write support.**
- **VESA and AT bus support**
- **Supports Intel, AMD, Cyrix processors**

When combined with the 83C206, the CY82C597 can provide a highly integrated, high-performance, low cost solution for 25/33/40/50 MHz PC/AT systems.

Functional Blocks

The CY82C597 consists of the following functional blocks:

3. Reset and shutdown logic
4. Clock generation logic
5. Bus arbitration logic
6. Turbo speed control logic
7. Level 1 write-back CPU support
8. Write-back/Write-through cache controller
9. Page mode DRAM controller
10. Shadow RAM logic
11. DMA/MASTER access to DRAM
12. Refresh logic
13. VESA local bus logic
14. AT bus interface logic
15. Support logic for various processors
16. Data bus conversion logic
17. Parity generation and checking logic
18. Numerical coprocessor interface logic
19. Keyboard emulation logic
20. Port B, Port70H and NMI logic
21. Power management logic

3. Reset and Shutdown Logic

The CPURST, $\overline{\text{SYSRST}}$, and 387 reset ($\overline{\text{NPRLD}}$) are derived from either the $\overline{\text{PWRGD}}$ signal from the power supply or the reset switch. CPURST is used to reset the CPU and $\overline{\text{SYSRST}}$ is used to reset all AT bus devices. $\overline{\text{NPRLD}}$ is used to reset the 387 coprocessor. Only CPURST is activated when performing a shutdown cycle or a software reset through the keyboard. The 387 reset signal is generated through pin 80 ($\overline{\text{NPRLD}}$). A write to Port F1H will also activate the 387 reset.

4. Clock Generation Logic

For 386 systems, a 2x clock signal should be connected to the CLK pin of the CY82C597. For 486 systems, a 1x clock should be connected to the CLK pin of the CY82C597. ATCLK is generated from CLK divided by a number specified by bit [1:0] of register 10. The desired target for the ATCLK is 8 MHz. Please refer to *Tables 1* and *2* for the recommended clock divisors and ATCLK speeds.

Table 1. 486 Clock Divisors

CPU Speed	Recommended Clock Divisor	ATCLK Speed
33 MHz	4	8.2 MHz
40 MHz	5	8.0 MHz
50 MHz	6	8.3 MHz

Table 2. 386 Clock Divisors

CPU Speed	CLK input to the CY82C597 (CPUCLKx2)	Recom-mended Clock Divisor	ATCLK Speed
25 MHz	*50 MHz*	*6*	*8.33 MHz*
33 MHz	*66 MHz*	*8*	*8.25 MHz*
40 MHz	*80 MHz*	*10*	*8.00 MHz*

In addition, ATCLK can be fixed at 7.159 MHz (14.31818 MHz/2). The clock source for the 8042 keyboard controller is the same as the ATCLK.

The CY82C597 can also generate a 14.318MHz divided by 12 clock (OSC119 at 1.19 MHz) for system use.

5. Bus Arbitration Logic

The CPU will relinquish control of its bus when a HOLD request is issued by any other device. For DMA and ISA Bus Master cycles, DMAHRQ is generated by the 83C206 causing a HOLD request signal to be sent to the CPU by the CY82C597. The CPU will respond by asserting HLDA and releasing the bus to the requesting device. The CY82C597 will then send an acknowledgement to the 83C206, allowing the DMA/MASTER cycle to be performed. Upon completion of the transaction, the CY82C597 will deassert the hold request, allowing the CPU to access the bus again.

When the CPU performs a master cycle on its local bus, it starts by asserting $\overline{\text{ADS}}$ and a valid address. If the target is motherboard DRAM/SRAM, the DRAM controller inside the CY82C597 will start to access DRAM/SRAM memory and will terminate the cycle with the appropriate signal ($\overline{\text{RDY}}$ or $\overline{\text{BRDY}}$). If the target is a VESA bus device, the device will assert the $\overline{\text{LDEV}}$ (local bus device) signal which will cause the CY82C597 to ignore the cycle and not respond. In this case, it is the responsibility of the VESA target to provide the data and $\overline{\text{RDY}}$ or $\overline{\text{BRDY}}$ acknowledgement to the CPU. If the target is on the AT bus, the CY82C597 will issue an AT bus cycle and complete the CPU bus transaction when the data is available.

6. Turbo Speed Control Logic

The CY82C597 supports both software and hardware Turbo speed control. Software TURBO mode is controlled by bit 2 of register 10H. The hardware TURBO switch should be connected to the 8042 keyboard controller. When the TURBO pin of the 8042 is active, the system software should enable TURBO mode within the CY82C597 (Register 10H bit 2 should be set to 0).

The CY82C597 will assert a HOLD request every 3 µs out of a 4 µs period if bit 2 of register 10H is set to 1 (TURBO mode disabled). When the 8042 TURBO pin is tied non-active, software should disable TURBO mode. The CY82C597 controls

the arbitration between Refresh, DMA and non-TURBO hold request.

7. Level 1 Write-back CPU Support

In order to improve system performance and reduce bus bandwidth requirements, some CPUs (from Intel, AMD, Cyrix, etc.) implement an internal, level 1, write-back cache. Write−back CPUs must snoop (by way of inquiry transactions) all memory transactions. The CY82C597 will generate an inquiry cycle by asserting $\overline{\text{EADS}}$, which will be monitored by the CPU, whenever there is an ISA DMA/MASTER memory cycle. During VESA master memory cycles, the VESA master must assert $\overline{\text{EADS}}$ along with $\overline{\text{ADS}}$. For PCI master memory cycles, the CY82C599 will assert $\overline{\text{EADS}}$.

Upon seeing $\overline{\text{EADS}}$ asserted, a write−back CPU will check the status of its internal cache. If the CPU's cache contains the line and it is marked modified (the data in the level 1 cache is more up-to-date than the data in main memory), the cpu will assert the $\overline{\text{HITM}}$ signal. If the CY82C597 sees $\overline{\text{HITM}}$ asserted, it will relinquish the bus to the CPU and will not respond to the original access until the CPU first copies the cache data back to system memory (this is referred to as a write-back cycle). Write-backs consist of burst write cycles (the CY82C597 will handle burst writes to memory), The CY82C597 will wait until the CPU has completed the write-back transaction before allowing any bus master to access the modified memory location.

The CY82C597 has an inquiry filter to reduce the overhead of unnecessary snoop cycles. Every time a bus master attempts to access system memory, the CY82C597 will check to see if the address was previously used for an inquiry cycle. If the address was "snooped" in the previous transaction, the CY82C597 will not generate an inquiry cycle (for ISA/DMA MASTER cycles) or will ignore the results of the inquiry cycle (for VESA/PCI Bus Master cycles) and will allow the transaction to pass directly to system memory.

8. Write-back/Write-through Cache Controller

Write-back Operation

The CY82C597 implements a Burst mode, write-back cache controller. It monitors TAGA[6:0] and compares it with the CPU TAG address. If the cache is enabled and the Tag address matches the CPU address, a "cache hit" is detected. During a read hit, the CY82C597 will burst four double words to the CPU by alternating $\overline{\text{CRD0}}$ and $\overline{\text{CRD1}}$ (2 Banks of cache) or strobing $\overline{\text{CRD0}}$ four times (1 Bank of cache).

In the case of a write hit, the CPU data will be written to the cache RAMs by asserting $\overline{\text{CWE0}}$ or $\overline{\text{CWE1}}$. DRAM data is not updated.

During a read miss, the DIRTY bit will be checked before reading in new data from the DRAMs. If DIRTY=1, the displaced data from the SRAMs is copied to the DRAMs before the line fill. In the case of a write miss, data will only be written to DRAM.

The CY82C597 also supports an 8-bit tag size (TAGA[7:0]) without a DIRTY bit. All lines are considered dirty. On a cache read miss, the line in the cache is automatically written back to memory before the new line in memory is read. In the case of a write miss, data will only be written to DRAM memory.

Write-through Operation

The CY82C597 also supports write-through cache operation. During a write hit, the CY82C597 writes data to both the SRAMs and the DRAMs. Additional wait states are required especially when a DRAM page miss occurs. For a write miss, data is written to DRAM memory only. Only the 8-bit tag configuration is supported in write-through mode.

The selection between write-through or write-back cache policies is controlled by bit 6 of register 11.

DMA/ISA Master Transactions

When a DMA/MASTER memory read hit occurs, data will be supplied from the cache SRAMs instead of the DRAMs. On a memory read miss, data is supplied by the DRAMs. In the case of a DMA/MASTER memory write hit cycle, data will be written into the DRAMs and SRAMs. A DMA/MASTER write miss cycle will only write data into the DRAMs.

Tag RAM/Data RAM Configurations

The CY82C597 supports 32KB, 64KB, 128KB, and 256KB cache sizes for the 386, and 64KB, 128KB, 256KB, 512KB, and 1MB cache sizes for the 486. In write-back mode, the CY82C597 combines the DIRTY RAM with the Tag RAM, thereby saving one SRAM for cache systems. The dirty bit can be replaced by a tag address in order to increase the cachable range. See *Tables 3*, *4*, and *5*. Dirty bit support vs. more cachable memory is controlled through bit 4 of control register 16.

Table 3. Tag RAM/Data RAM Requirements without a Dirty Bit

Cache Size	Tag RAM	Tag Address	Tag Field	Cachable Size[1]
32KB	2K x 8	A14 − A4	A22 − A15	8 MB
64KB	4K x 8	A15 − A4	A23 − A16	16 MB
128KB	8K x 8	A16 − A4	A24 − A17	32 MB
256KB	16K x 8	A17 − A4	A25 − A18	64 MB
512KB	32K x 8	A18 − A4	A26 − A19	128 MB
1MB	64K x 8	A19 − A4	A26 − A20	128 MB

Note:
1. 128MB is the maximum DRAM size supported.

Table 4. Cache with Dirty Bit (TAGA7 will serve as dirty bit)[2, 3, 4, 5]

Cache Size	Tag RAM	Tag Address	Tag Field	Cachable Size
32KB	2K x 8	A14 – A4	A21 – A15	4 MB
64KB	4K x 8	A15 – A4	A22 – A16	8 MB
128KB	8K x 8	A16 – A4	A23 – A17	16 MB
256KB	16K x 8	A17 – A4	A24 – A18	32 MB
512KB	32K x 8	A18 – A4	A25 – A19	64 MB
1MB	64K x 8	A19 – A4	A26 – A20	128 MB

Notes:
2. For 386 cache systems, the cache data RAMs need to be: 32KB cache: 1 bank (4 pieces) 8K x 8 SRAM, 64KB cache: 2 bank (8 pieces) 8K x 8 SRAM, 128KB cache: 1 bank (4 pieces) 32K x 8 SRAM, 256KB cache: 2 bank (8 piece) 32K x 8 SRAM.
3. For 486 cache systems, the cache data RAMs need to be: 32KB cache: 1 bank (4 pieces) 8K x 8 SRAM, 64KB cache: 2 bank (8 pieces) 8K x 8 SRAM, 128KB cache: 1 bank (4 pieces) 32K x 8 SRAM, 256KB cache: 2 bank (8 piece) 32K x 8 SRAM., 512KB: 1 bank (4 pieces) 128K x 8 SRAM, 1MB cache: 2 banks (8 pieces) 128K x 8 SRAM.
4. Cache line size is fixed at 16 bytes.
5. Cachable range is handled automatically by hardware.

Table 5. Tag RAM/Data RAM speed[2, 3]

CPU Speed	Tag RAM Speed	Data RAM Speed (Single Bank)	Data RAM Speed Interleaved (Dual Bank)
25 MHz (386+486)	20 ns	20 ns	25 ns
33 MHz (386+486)	15 ns	20 ns	25 ns
40 MHz (386)	15 ns	15 ns	20 ns
50 MHz (486) 3222 mode	20 ns	20 ns	25 ns

9. Page Mode DRAM Controller

Introduction

A pure Page mode DRAM controller is used in this design. No Interleaving is required. The CY82C597 can support mixed DRAM sizes. The starting address of each DRAM bank is calculated by internal hardware. The user can configure DRAM memory from 1MB to 128MB, as long as the memory stays continuous. The DRAM controller supports up to four banks of DRAM memory. Four RAS and four CAS signals (for three and four bank systems) or two RAS and four CAS signals (for one and two bank systems) are the allowed options. The DRAM controller also provides the multiplexed row and column addresses for the DRAMs. The address split is configurable, and the supported DRAM splits are given in the following tables.

DRAM Row/Column Address

The DRAM row address is listed as follows:

Address Split		DRAM Type	Row Address											
Row	Col.		MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9	MA10	MA11
9	9	256KB	A12	A13	A14	A15	A16	A17	A18	A19	A11	X	X	X
9	10	512KB	A12	A13	A14	A15	A16	A17	A18	A19	A20	X	X	X
10	10	1MB	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	X	X
11	9	1MB	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A11	X
12	8	1MB	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A11	A10
11	10	2MB	A22	A13	A14	A15	A16	A17	A18	A19	A20	A21	A12	X
12	9	2MB	A22	A13	A14	A15	A16	A17	A18	A19	A20	A21	A12	A11
11	11	4MB	A23	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	X
12	10	4MB	A23	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A12
16	6	4MB	A23	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	X
12	12	16MB	A23	A24	A14	A15	A16	A17	A18	A19	A20	A21	A22	A25

The DRAM column address is listed as follows: [6]

Address Split			Column Address											
Row	Col.	DRAM TYPE	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9	MA10	MA11
9	9	256KB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	X	X	X
9	10	512KB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	$\overline{A11}$	X	X
10	10	1MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	$\overline{A11}$	X	X
11	9	1MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	X	X	X
12	8	1MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	X	X	X	X
11	10	2MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	$\overline{A11}$	X	X
12	9	2MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	X	X	X
11	11	4MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	$\overline{A11}$	$\overline{A12}$	X
12	10	4MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	$\overline{A11}$	X	X
16	6	4MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	$\overline{A11}$	$\overline{A12}$	X
12	12	16MB	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$	$\overline{A5}$	$\overline{A6}$	$\overline{A7}$	$\overline{A8}$	$\overline{A9}$	$\overline{A10}$	$\overline{A11}$	$\overline{A12}$	$\overline{A13}$

Notes:
6. The column address lines are inverted from the CPU address.

DRAM Speed

Table 6. DRAM Speed/Wait States (Based on Page Mode DRAMs)

CPU Speed	DRAM Speed	DRAM Wait States (READ, WRITE)
25 MHz	100 ns	(R1WT, W0WT)
	80 ns	(R1WT, W0WT)
33 MHz	100 ns	(R2WT, W0WT)
	80 ns	(R2WT, W0WT)
40 MHz	100 ns	(R2WT, W1WT)
	80 ns	(R2WT, W1WT)
50 MHz	100 ns	(R3WT, W1WT)
	80 ns	(R3WT, W1WT)

10. Shadow RAM Logic

DRAM accesses are generally much faster than accesses to ROM or EPROM. The CY82C597 provides shadow RAM support to speed up system ROM and adapter ROM access time. ROM code can be moved into a reserved RAM space (Shadowed). After the move, the RAM area will be protected (set to read-only). All subsequent accesses to ROM are automatically routed to the protected RAM area. By moving ROM code to DRAM, performance can be improved dramatically. Shadow RAM on blocks C and F can also be configured as cachable or non-cachable (the default is non-cachable).

11. DMA/Master Access to DRAM

DMA cycles are controlled by the 83C206. DMA and ISA MASTER cycles are treated similarly. The arbitration for DMA and ISA MASTER cycles are coordinated through the 83C206. The ISA card will issue a DMA request to the 83C206. The 83C206 will assert DMAHRQ (DMA hold request) to the CY82C597. The CY82C597 will immediately issue a HOLD request to the CPU. Upon receipt of the HLDA (hold acknowledge) from the CPU, the CY82C597 will issue a DMA hold acknowledge to the 83C206 allowing the DMA or ISA MASTER cycle to commence. Once the internal arbitration logic grants a DMA/MASTER cycle, it will monitor the internal cache hit signals, $\overline{\text{MEMR}}$, and $\overline{\text{MEMW}}$. If the cycle is a memory read hit, the CY82C597 will provide data from the SRAMs. A memory read miss cycle will cause data to be accessed from the DRAMs. In the case of a memory write hit cycle, data will be written into both DRAM and SRAM memory. For a write miss cycle, data will be written into DRAM memory only.

12. Refresh Logic

The CY82C597 has an internal counter to generate a refresh request signal every 15.6 µs. Once the internal refresh request signal goes active, the refresh logic will check to see if it is an AT or Hidden refresh (Register 16, bit 6). In the case of an AT refresh, a HOLD request will be issued to the CPU. After receiving HLDA from the CPU, the arbitration logic will grant the refresh cycle. Refresh logic will start the cycle by sending the refresh address and 2 staggered $\overline{\text{RAS}}$ signals to the DRAMs. At the same time, the CY82C597 will send a refresh address and $\overline{\text{REFSH}}$ to the ISA bus. If hidden refresh is programmed, the CY82C597 will not send out a CPU HOLD signal. Instead, the CY82C597 will grant a refresh cycle to the refresh logic if the AT state machine is not busy. If the CPU tries to access the AT bus or DRAM during a hidden refresh, wait states will be inserted into the cycle until the refresh completes.

13. VESA Local Bus Logic

The CY82C597 supports VESA Local Bus devices by monitoring pin 8 ($\overline{\text{NPRDYLC}}$) at the end of T2 (2-1-1-1 mode) or the end of the second T2 (3-1-1-1/3-2-2-2 mode). All VESA $\overline{\text{LDEV}}$ signals should be externally ANDed together to provide the $\overline{\text{NPRDYLC}}$ signal. If a local device cycle is detected ($\overline{\text{NPRDYLC}}$ asserted LOW by any local device), the CY82C597 will allow the local device to fully control the bus.

The CY82C597 can also perform the arbitration for up to 2 VESA masters. The arbitration is fixed priority (device 1 has a higher VESA priority than device 2). When the CY82C597 detects a local request from a VESA master, it immediately issues a HOLD request to the CPU. Upon receiving HLDA from the CPU, the CY82C597 will grant the VESA bus to the highest priority master (provided that a refresh request is not pending). The CY82C597 will release the grant to the VESA master when its request is deactivated.

14. AT Bus Interface Logic

An AT bus cycle begins when the CPU wants to access an AT bus device. When ALE is generated, the AT state machine monitors $\overline{\text{MCS16}}$, $\overline{\text{IOCS16}}$, $\overline{\text{0WS}}$ and IOCHRDY from the AT bus and generates the command and control signals to the AT bus. The current AT bus cycle is terminated when a ready signal ($\overline{\text{CPURDY}}$) is returned to the CPU.

In order to support DMA/MASTER accesses, the CY82C597 will generate $\overline{\text{ADS}}$, M/$\overline{\text{IO}}$, and W/$\overline{\text{R}}$, after detecting HOLDA from the CPU.

15. Support for Various Processors via Modular Design

Modular design means all common components reside on the motherboard with the CPU and the cache memory socketed for easy upgrade. With this technology, the user can build a 386, 486, or 486SX cache/non-cache system using the same motherboard.

The CY82C597 supports various processors. When pin 7 ($\overline{\text{B387S4}}$) is pulled to V_{CC} through a 10 KΩ resistor, a 386 processor is selected. If pin 7 is pulled down to V_{SS}, the CY82C597 will consider the processor to be a 486. With this feature, the user can build one motherboard to support 386 cache/non-cache, and 486DX/SX cache/non-cache system.

16. Data Bus Conversion Logic

As the 486 CPU bus is 32 bits wide and the ISA bus has 8 and 16 bit residents, the CY82C597 performs data bus conversion for the following cycles: (1) CPU accesses 8- or 16-bit devices on the CQ bus through 16/32-bit instructions, (2) DMA/MASTER cycles from AT devices to local DRAM, cache memory, or on-board I/O devices (8/16 bit device translation to a 32/16 bit CPU bus).

During the conversion, the CY82C597 automatically provides all the necessary control signals to the external bidirectional data buffers.

17. Parity Generation and Checking Logic

For local DRAM write cycles from both the CPU and DMA/MASTER devices, the CY82C597 generates byte parity bits MP[3:0]. The parity bits are stored in the local DRAM along with the data.

During the local DRAM read cycle, the data and parity bits are read from the DRAMs into the CY82C597. Parity checking logic compares the parity bits with the parity generated from the read data. If a mismatch is detected and the system memory parity check is enabled, an NMI will be asserted by the CY82C597, if NMI reporting in enabled.

18. Numerical Coprocessor Interface Logic

The CY82C597 supports the Weitek 4167 Numerical Coprocessor (486SX systems), the Weitek 3167, and the Intel 387 Numerical Coprocessor (386 systems) without any external logic.

For 486SX systems, INT13 will be asserted when either $\overline{\text{FERR}}$ or WTINTR is activated. As soon as the $\overline{\text{FERR}}$ is asserted, the interrupt service routine will handle the error and clear the interrupt by executing a dummy write to I/O port F0H. The $\overline{\text{IGNNE}}$ signal is also activated by writing to the I/O port F0H.

For 386 systems, $\overline{\text{BUSY386}}$ is asserted when $\overline{\text{BUSY387}}$ is active to signal the 386 that the coprocessor is currently executing an instruction. If $\overline{\text{BUSY387}}$ is active when $\overline{\text{ERR387}}$ is active, the $\overline{\text{BUSY387}}$ will be latched and IRQ will be generated. The latched $\overline{\text{BUSY387}}$ can be cleared by performing a write to I/O port F0H. If the Weitek 3167 is being used and the interrupt signal (WTINTR) is active, IRQ will be asserted. The $\overline{\text{ERR386}}$ signal is asserted after system reset if a 387 is present. It will stay active until the first CPU cycle begins.

19. Keyboard Emulation Logic

I/O Port 60H and 64H are used to implement keyboard controller emulation. The keyboard emulation is enabled by programming register 10, bit 3 to a 0. When fast GA20 is enabled, writing D1H to Port 64H followed by DDH to Port 60H, A20 will be forced LOW in a 386 system. For a 486 system, the $\overline{\text{A20M}}$ pin should be connected to the 8042 and E386NGT functions as the A25 input. If the system is designed to support 32 MB of main memory or less, the E386NGT signal can be connected to the $\overline{\text{A20M}}$ signal on the 486 for fast GATEA20 operation.

The CY82C597 also performs fast RESET by intercepting the keyboard reset command sequence and performing the reset directly. The CY82C597 can be programmed to wait for a HALT instruction before asserting reset to the CPU.

20. Port B (61H), NMI, and Port 70H

When a parity error is detected by the CY82C597 , an NMI will be generated to the CPU if NMI reporting is enabled. NMI reporting can be enabled by setting bit 7 of Port 70H to 0. The CY82C597 provides access to the Port B register defined for a PC/AT. The chart below illustrates the bit definition for Port B (61H):

Address	Bit	Access	Description
61H	7	Read Only	System memory parity check
	6	Read Only	I/O channel check
	5	Read Only	Timer 2 output
	4	Read Only	Refresh detection
	3	Read/Write	0: Enable I/O channel check 1: Disable I/O channel check
	2	Read/Write	0: Enable system memory parity check. 1: Disable system memory parity check
	1	Read/Write	Speaker data
	0	Read/Write	Timer 2 gate

21. Power Management Logic

The CY82C597 implements flexible power management logic. When used with the CY82C599 (for a full VESA/ISA/PCI system), most of the power management functions are performed by the CY82C599. The CY82C597 will only perform the SMM memory mapping. All other power management functions in the CY82C597 are disabled. For VESA/ISA-only systems, the CY82C597 provides all of the chipset power management.

There are eleven event detectors and five user-programmable timers in the CY82C597 allowing it to support full hardware power management (for CPUs that do not support SMM, System Management Mode) and software power management (through SMM).

Monitored Events

The CY82C597 allows the following events to be monitored:

1. VESA master request
2. Keyboard command
3. Serial Port command
4. Parallel Port command
5. Hard Disk command
6. DMA/MASTER request from the ISA bus
7. Non-motherboard memory access
8. Video memory access
9. A specific I/O address
10. A specific memory range
11. A specific I/O range

When events are detected, the CY82C597 will transition to different power-down states.

Hardware Power Management

For hardware power management, the CY82C597 supports Full-speed/Stand-by/Suspend/Off states. In Stand-by state, the CY82C597 will assert the $\overline{\text{SLOWCLK}}$ signal that can be used by the system to slow down the CPU's clock frequency. In the Suspend state, the CY82C597 will assert the $\overline{\text{STOPCLK}}$ signal. $\overline{\text{STOPCLK}}$ can be used to stop the CPU's clock or turn off the monitor and other supported peripherals.

In the Full-speed state, the CY82C597 will monitor all stand-by events. Any monitored event will reset the stand-by timer. If no events occur within the period specified by the stand-by timer, the CY82C597 will enter the Stand-by state and assert the $\overline{\text{SLOWCLK}}$ signal. Once Stand-by state has been entered, the CY82C597 will monitor Suspend state events. If no event occurs within the period specified by the suspend timer, the CY82C597 will assert $\overline{\text{STOPCLK}}$ and enter the Suspend state. In the Suspend state, the assertion of $\overline{\text{STOPCLK}}$ can be used to stop the CPU's clock or power-down any supported peripherals. If any monitored event is detected, the CY82C597 will return to the Full-speed state and $\overline{\text{STOPCLK}}$/$\overline{\text{SLOWCLK}}$ will be deasserted.

Any interrupt will temporarily cause the $\overline{\text{STOPCLK}}$ signal (and optionally the $\overline{\text{SLOWCLK}}$ signal) to be deasserted (allowing the CPU to service the interrupt). If the interrupt timer expires before a monitored event occurs, the CY82C597 will automatically return to the power-down state it was in prior to the interrupt (with the appropriate signal asserted).

Software Power Management

For software power management, the CY82C597 can fully utilize Intel's, AMD's, and Cyrix's power management modes to reduce system power requirements.

In the Full-speed state, the CY82C597 will monitor all stand-by events. If no events occur within the period specified by the stand-by timer, the CY82C597 will enter the Stand-by state and assert the $\overline{SMI}$ signal. In Stand-by state, the system clock can be slowed down by the assertion of the $\overline{SLOWCLK}$ signal. $\overline{SLOWCLK}$ is controlled through software (See Register 64). Once Stand-by state has been entered, the CY82C597 will monitor Suspend state events. If no event occurs within the period specified by the suspend timer, the CY82C597 will assert $\overline{SMI}$ and enter the Suspend state. In the Suspend state, software assertion of $\overline{STOPCLK}$ (See register 64) can be used to stop the CPU's clock, the monitor can be turned off using a software driver, or the hard disk can be spun down. Please note that the assertion/deassertion of $\overline{STOPCLK}$ and $\overline{SLOWCLK}$ is fully software controlled and can be implemented in any power-down state (Stand-by and Suspend are customary).

The Suspend timer is fully reprogrammable. In the Suspend state, the Suspend timer can be disabled, the timer value changed, and the timer reenabled. After the new timer value has expired, $\overline{SMI}$ will once again be activated to allow for a user-defined power management mode.

The CY82C597 also contains three independent timers that can be used during the power-down control period. Different events and different time periods can be specified for each timer. Each timer will cause $\overline{SMI}$ to be asserted after the specified time period has expired. The three timers allow for more user-defined, power-down system states.

In order to identify the source of the $\overline{SMI}$ (System Management Interrupt), the CY82C597 maintains a status register (register 58) that keeps track of which event caused $\overline{SMI}$ to be asserted. Power-management software should read the status register before determining a course of action. The CPU and peripherals can be individually powered-down based on the source of the System Management Interrupt.

If any specified event is detected during Stand-by, Suspend, or any other power-down state, the CY82C597 will automatically return to the Full-speed state (with the stand-by timer reset). If the system is using software power management, the CY82C597 will assert $\overline{SMI}$ and within the $\overline{SMI}$ handler, software should bring all of the system clocks to their full-speed, full-power states through the deassertion of $\overline{STOPCLK}$/$\overline{SLOWCLK}$.

The CY82C597 supports SMM (System Management Mode) memory. If $\overline{SMACT}$ (Intel) or $\overline{SMADS}$ (Cyrix, AMD) is seen asserted, all memory accesses will be sent to a protected memory space (physical DRAM blocks A and B). The SMI handler and SMM data must be stored in the protected space. If software power management is used, ROM or video RAM cannot be shadowed in blocks A and B.

CY82C597 Control Registers

The control registers for the CY82C597 are defined in this section. The registers can be accessed through I/O Ports 22H and 23H. To access each register, the user must first write the index number of the register into Port 22, which forces the internal decoding logic to point to the selected register. Data can be accessed by then reading/writing to/from Port 23.

Register 10: AT Bus Control, Index: 10

Bit	Function	Default
7	486 speed indicator 0: 20/25 MHz 1: 33/40/50 MHz	0
6	Parity check disable [7] 0: Enable parity checking 1: Disable parity checking	0
5	386 speed indicator 0: 40 MHz 1: 33 MHz (or any speed below 33 MHz)	0
4	Reserved, BIOS should set to 1.	0
3	Fast Gate A20 Emulation Control (386 only) 0: Enable 1: Disable	0
2	Turbo speed control: 0: Enable turbo speed (high speed) 1: Enable low speed	0
1:0	ATCLK control Bits 01 486 system: (pin 4 tied to V_{CC} through a 51KΩ resistor) 00: CLK/4 01: CLK/6 10: CLK/8 11: CLK/5 Bits 01 486 system: (pin 4 tied to V_{SS} through a 1KΩ resistor) 00: CLK/2 01: CLK/3 10: CLK/4 11: CLK/2.5 Bits 01 386 system: 00: CLK/4 01: CLK/6 10: CLK/8 11: CLK/10	00

Notes:

7. If parity checking is disabled, the parity bits are used as VESA local bus request and grant signals (see pin description). If parity is required in the system, an external PAL must be used to control VESA local arbitration signals (if bus mastership from the VESA slots is allowed).

Register 11: Cache Control, Index: 11

Bit	Function	Default
7	486 Burst control mode: [8] 0: 3111 Burst Mode. For 33/40/50 MHz systems. 1: 2111 Burst Mode. For 20/25/33 MHz systems. For 386 systems, this bit should be set to 1 by the BIOS.	0
6	486 external cache type control: 0: Write-back cache. 1: Write-through cache. For 386 systems, only write-back cache is supported. This bit is ignored.	0
5	SRAM write wait states: 0: 1 wait 1: 0 wait	0
4	Direct SRAM access control: 0: Disable 1: Enable	0
3:2	Cache size: [9] Bits 32 Size (386 system) 00: 32KB 01: 64KB 10: 128KB 11: 256KB Bits 32 Size (486 system) 00: 64KB 01: 128KB 10: 256KB 11: 512KB	00
1	Cache hit/miss control 0: All cache accesses are forced to miss 1: Normal cache access	0
0	Cache enable control 0: Disable cache 1: Enable cache	0

Before enabling direct SRAM access, the cache should be disabled. After direct SRAM access is enabled, all CPU accesses to address 40000H to 7FFFFH will be forced to SRAM when the cache size is smaller than 512KB. If the cache size is 512KB, or larger, addresses from 20000H to 9FFFFH will be forced to SRAM. This feature can be used to debug/test cache memory.

Register 12: DRAM Type, Index: 12

Bit	Function	Default
7	Reserved, BIOS should set to 0.	0
6	Reserved, BIOS should set to 0.	0
5	Reserved, BIOS should set to 1.	0
4	0: Enable Flash write[10] 1: Disable Flash write	0
3:2	Bank 1 [11] Bits 32 Type 00: Disabled 01: 256KB 10: 1MB 11: 4MB	00
1:0	Bank 0 [12] Bits 10 Type 00: 256KB 01: 1MB 10: 4MB 11: Disabled	00

Notes:
8. See register 1B, bit 6.
9. See register 1A, bit 1.
10. If Flash write is disabled, writes into ROM space will not be executed.
11. See register 1A, bit 7.
12. See register 1A, bit 5.

Register 13: DRAM Wait State and Cachable Range Control, Index: 13[13]

Bit	Function	Default
7:4	Bits 7654 Range 0000: 0−128MB 0001: 0−8MB 0010: 0−16MB 0011: 0−24MB 0100: 0−32MB 0101: 0−40MB 0110: 0−48MB 0111: 0−56MB 1000: 0−64MB 1001: 0−72MB 1010: 0−80MB 1011: 0−88MB 1100: 0−96MB 1101: 0−104MB 1110: 0−112MB 1111: 0−128MB	0000
3	Reserved, BIOS should set to 1.	0
2	DRAM write wait states: 0: 1 wait state 1: 0 wait states	0
1:0	DRAM read wait states: Bits 10 # of wait states 00: 3 01: 2 10: 1 11: 0	00

Notes:
13. The CY82C597 will take care of the cachable range. Bits [7:4] are for custom memory configurations.

Register 14: DRAM Wait State and Cachable Range Control, Index: 14

Bit	Function	Default
7	CPU reset control: 0: CPU reset will not wait for HALT instruction 1: CPU reset will wait for HALT instruction.	0
6	RAS precharge time[14] 0: 3 clocks 1: 2 clocks	0
5	Reserved, BIOS should set to 0	0
4:0	Remap location Bits 43210 Location 00000: Disable remap 00001: 1M 00010: 2M 00100: 4M 00101: 5M 01000: 8M 10000: 16M 10001: 17M 10100: 20M	00000

If blocks A, B, D, E on the local bus are not used for shadowing peripheral ROM, they can be remapped to the top of the memory space. By doing this, a 4-MB memory space can become 4MB +256KB. The physical location of the remapped 256KB are in DRAM blocks A, B, D, and E. If any of blocks A, B, D, and E are being used to shadow peripheral ROM, remapping is not allowed.

Register 15: Shadow RAM Block C, F Control, Index: 15

Bit	Function	Default
7	Block F RAM access control (F0000H−FFFFFH) 0: Write only 1: Read only	0
6	Block F RAM enable control 0: Disable. Access on board ROM. 1: Enable. Access RAM	0
5	Shadow RAM at CC000H−CFFFFH control 0: Disable. Will access AT bus memory. 1: Enable.	0
4	Shadow RAM at C8000H−CBFFFH control. 0: Disable. Will access AT bus memory. 1: Enable.	0
3	Shadow RAM at C4000H−C7FFFH control. 0: Disable. Will access AT bus memory. 1: Enable	0
2	Shadow RAM at C0000H−C3FFFH control. 0: Disable. Will access AT bus memory. 1: Enable.	0
1	Block C RAM access control (C0000H−CFFFFH) 0: Write only. 1: Read only.	0
0	Block C RAM/ROM control 0: Access RAM. If RAM is disabled, access will go to AT bus memory. 1: Access on board ROM.	0

Notes:
14. When DRAM read wait states are set to 3, the RAS precharge time will be forced to 4 clocks (50 MHz system).

Shadowing Instructions

To shadow system BIOS (Block F), you must::

1. Set register 15, bit 6 to “0” to enable ROM access.
2. Read ROM data into the CPU register.
3. Set register 15, bit 6 to “1” to enable RAM access.
4. Set register 15, bit 7 to “0” to enable RAM write.
5. Write the data stored in the CPU register to RAM.
6. Go to step 1 if not done. Else, go to step 7.
7. Set register 15, bit 7 to “1” to enable shadow RAM read access and write protect it.

Shadowing on-board ROM is similar to shadowing system ROM. The following example is used to shadow Block C from on-board ROM:

1. Set register 15, bit 0 to “1” to enable ROM access.
2. Read ROM data into the CPU register.
3. Set register 15, bit 0 to “0” to enable RAM access.
4. Set register 15, bit 1 to “0” to enable RAM write.
5. Write the data stored in the CPU register to RAM.
6. Go to step 1 if not done. Else, go to step 7.
7. Set register 15, bit 1 to “1” to enable shadow RAM read access and write protect it.

Shadowing AT bus ROM is slightly different than shadowing on-board ROM.
The following example is used to shadow Block C from AT bus ROM:

1. Set register 15, bit 0 to 0 to disable on-board ROM access.
2. Set register 15, bits 2, 3, 4, and 5 to 0 to disable RAM access. All access to Block C will go to the AT bus.
3. Read AT ROM data into CPU register.
4. Set register 15, bits 2, 3, 4, and 5 to 1 to enable RAM access.
5. Set register 15, bit 1 to 0 to enable RAM write.
6. Write the data stored in CPU register to RAM.
7. Go to step 1 if not done. Else, go to step 8.
8. Set register 15, bit 1 to 1 to enable shadow RAM read access and write protect it.

Register 16: Miscellaneous Control 1 Register, Index: 16

Bit	Function	Default
7	SRAM $\overline{\text{TAGWT}}$ delay control 0: For 1 wait state SRAM 1: For 0 wait state SRAM	0
6	Hidden Refresh Control 0: AT refresh 1: Hidden refresh.	0
5	DRAM $\overline{\text{RAS}}$ to MA [10:0], MA [10:0] to $\overline{\text{CAS}}$ delay. 0: 2 clocks. 1: 1 clock.	0
4	Dirty bit enable control: 0: Disable. No dirty bit (8 bit tag). 1: Enable. TAGA7 becomes the dirty bit (7 bit tag).	0
3	DRAM 15−16 MB disable control: 0: Normal. 1: Address 15−16 MB will not be on the motherboard.	0
2	Non-cachable block dual-function control: (for register 18, 19, and 1A) 0: For non-cachable block. 1: Non-cachable block becomes a non-local memory block.	0
1	Reserved, BIOS should set to 0.	0
0	Reserved, BIOS should set to 0.	0

Register 17: Miscellaneous Control 2 Register, Index: 17

Bit	Function	Default
7	Block F(F0000H−FFFFFH) Cachable control 0: Non-cachable. 1: Cachable.	0
6	Block C(C0000H−CFFFFH) Cachable control 0: Non-cachable. 1: Cachable.	0
5	Reserved, BIOS should set to 1.	0
4	Reserved, BIOS should set to 0.	0
3	Reserved, BIOS should set to 0.	0
2	Reserved, BIOS should set to 1.	0
1	Reserved, BIOS should set to 1.	0
0	$\overline{\text{EADS}}$ control 0: $\overline{\text{EADS}}$ is a dedicated output. 1: $\overline{\text{EADS}}$ is three-state.	0

Register 18: Non-Cachable/non-local Block 0 Starting Address, Index: 18[15, 16, 17]

Bit	Function	Default
7:0	Bits 7 6 5 4 3 2 1 0 A23 A22 A21 A20 A19 A18 A17 A16	00000000

Notes:
15. Bits 0, 1, 2, 3, 4, and 5 may not be needed. Please see note on Register 19.
16. A24 of the non-cachable/non-local Block 0 starting address is bit 0 of Register 19.
17. A25 and A26 of the non-cachable/non-local Block 0 starting address are bits 2 and 3 of Register 1A.

Register 19: Non-cachable Block 0 Starting Address and Size, Index: 19[18]

Bit	Function	Default
7	Slow DRAM select 0: Fast page mode DRAM supported. 1: Fast page mode DRAM not supported	0
6	486 Single bank SRAM select 0: Support interleaved SRAMs (2 banks of SRAMs). 1: Support 1 bank of SRAMs. This is for 128KB cache using 32Kx8 SRAMs and 512KB cache using 128Kx8 SRAMs.	0
5	Reserved, BIOS should set to 0.	0
4	Non-cachable Block 0 control 0: Disable. 1: Enable.	0
3:1	Non-cachable size Bits 321 Size 000: 64KB 010: 128KB 100: 256KB 110: 512KB 001: 1MB 011: 2MB	000
0	Non-cachable/non-local Block 0 starting address A24.	0

Note:

18. For 64KB non-cachable size, the starting address is bound by A24−A16 from the configuration registers.
For 128KB non-cachable size, the starting address is bound by A24−A17 from the configuration registers.
For 256KB non-cachable size, the starting address is bound by A24−A18 from the configuration registers.
For 512KB non-cachable size, the starting address is bound by A24−A19 from the configuration registers.
For 1MB non-cachable size, the starting address is bound by A24−A20 from the configuration registers.
For 2MB non-cachable size, the starting address is bound by A24−A21 from the configuration registers.

Please note that the non-cachable size is independent of cache size. The non-cachable starting address and non-cachable size are used to define an address range that will not be cached.

When Register 16, bit 2 is set to 1, the non-cachable block will be changed to a non-local block. All addresses within this block will not be on the motherboard, i.e., they will go to the AT bus or VESA bus.

For 386 systems, 32KB/128KB cache is fixed to 1 bank of SRAMs. 64KB/256KB is fixed to 2 banks of SRAMs. For 486 systems, 64KB/128KB/256KB/512KB/1MB can be either 1 or 2 banks of SRAMs.

Register 1A: Control Register, Index: 1A

Bit	Function	Default
7:6	Bank 1 DRAM size modification[19] Bits 00: Bank 1 size is determined by Register 12, bit [3:2] 01: 512KB DRAM 10: 16MB DRAM 11: 2MB DRAM	00
5:4	Bank 0 DRAM size modification [20] Bits 00: Bank 0 size is determined by register 12, bit [1:0] 01: 512KB DRAM 10: 16MB DRAM 11: 2MB DRAM	00
3:2	Non-cachable/non-local Block 0 starting address (See register 18) 3=A26 2=A25	0
1	Bits 1: 1MB cache size 0: Refer to Register 11, but [3:2]	0
0	Reserved, BIOS should set to 0.	0

Register 1B: Miscellaneous Control Register 3, Index: 1B

Bit	Function	Default
7	Reserved, BIOS should set to 0.	0
6	Additional cache speed control 0: No additional delay. 1: Additional delay, 3222 mode for 50 MHz. Once set, it will overwrite register 11, bit 7, which is used to control cache SRAM 2111 or 3111 burst sequence.	0
5	Reserved, BIOS should set to 1.	0
4	Reserved, BIOS should set to 0.	0
3:2	Reserved, BIOS should set to 11.	00
1:0	Reserved, BIOS should set to 00.	00

Register 1C: Miscellaneous Control Register, Index: 1C

Bit	Function	Default
7	Bits 0: Symmetrical 4MB DRAM 1: Special 4MB DRAM with 16 row addresses and 6 column addresses	0
6	Bits 0: Symmetrical 4MB DRAM 1: Special 4MB DRAM with 12 row addresses and 10 column addresses	0
5	Bits 0: Normal mode (For 40/50 MHz systems, this bit should be set to 0) 1: Fast write at 25/33 MHz	0
4	Reserved, BIOS must set to 1.	0
3	Bits 0: Keyboard soft reset will not generate NPRST 1: Keyboard soft reset will generate NPRST	0
2	Reserved, BIOS should be set to 0.	0
1	Bits 0: ATCLK controlled by register 10, bit [1:0] 1: ATCLK fixed at 7.159 MHz	0
0	Bits 0: Normal mode (no additional IDLE AT CYCLES between AT command cycles) 1: Add one extra IDLE AT CYCLE between AT command cycles	0

Register 1D: Miscellaneous Control Register, Index: 1D

Bit	Function	Default
7	Bits 0: Normal mode (enable upper DRAM) 1: Upper 64KB or 1KB DRAM memory will be disabled	0
6	Bits 0: Upper 64K of DRAM will be disabled if bit 7=1 1: Upper 1K of DRAM will be disabled if bit 7=1	0
5	Reserved, BIOS should set to 0.	0
4	Bits 0: Add one SYSCLK cycle of delay before AT cycle detection 1: Add two SYSCLK cycles of delay before AT cycle detection	0
3	Fast DRAM write, BIOS should set to 1.	0
2	Reserved, BIOS should be set to 0.	0
1	Bits 0: AT cycle detection at end of T2 if register 11, bit 7=1 (2111 mode) AT cycle detection at end of second T2 if register 11, bit 7=0 (3111/3222 mode) 1: Add extra delay on AT cycle detection, extra delay based on register 1D, bit 4 setting	0
0	Reserved, BIOS should set to 0.	0

Notes:

19. If Bank 1 is selected for 512KB/16MB/2MB operation, the value in register 12, bits [3:2], will be ignored.
20. If Bank 0 is selected for 512KB/16MB/2MB operation, the value in register 12, bits [1:0], will be ignored.

Registered 1E: Power Management Stand-by Timer and Event Control Register 1, Index: 1E

Bit	Function	Default
7	Reserved	0
6	Bits 0: Do not monitor VESA master request 1: Monitor VESA master request	0
5	Stand-by mode timer control, please see BIT (3:1). If Bit 5=0 / If Bit 5=1 000: 30 sec. / 000: 0.2 sec. 001: 3.8 min. / 001: 0.4 sec. 010: 7.5 min. / 010: 1 sec. 011: 15 min. / 011: 1.8 sec. 100: 30 min. / 100: 3.5 sec. 101: 60 min. / 101: 7 sec. 110: 120 min. / 110: 14 sec. 111: 240 min. / 111: 30 sec.	0
4	Reserved	0
3:1	Stand-by mode timer (Values for bits 3:1 are given in bit 5 definition)	000
0	Bits 0: Disable power management mode 1: Enable power management mode	0

Register 1F: Stand-by Mode Event Control, Index: 1F

Bit	Function	Default
7	Bits 0: Disable keyboard detection 1: Enable keyboard detection	0
6	Bits 0: Disable serial port detection 1: Enable serial port detection	0
5	Bits 0: Disable parallel port detection 1: Enable parallel port detection	0
4	Bits 0: Disable hard disk detection 1: Enable hard disk detection	0
3	Bits 0: Disable DMA/ISA MASTER detection 1: Enable DMA/ISA MASTER detection	0
2	Bits 0: Disable non-motherboard memory detection 1: Enable non-motherboard memory detection	0
1	Reserved	0
0	Bits 0: Disable video memory (Block A,B) detection 1: Enable video memory (Block A,B) detection	0

Register 60: I/O Address (for Address Detection), Index: 60

Bit	Function	Default
7:0	Bits 7:0 I/O Address to be Monitored	00000000

Register 61: I/O Address Detection and Miscellaneous Control, Index: 61

Bit	Function	Default
7	Bits 0: VESA/AT only mode (82C597 stand-alone) 1: 82C599 PCI bridge is present in the system	0
6	Bits 0: NMI output is non three-state 1: NMI output is three-state	0
5	Reserved	0
4	Reserved	0
3	Bits 0: Disable I/O address detection 1: Enable I/O address detection	0
2	Reserved, must be 0	0
1:0	I/O address (9:8)	00

Register 62: Suspend Timer and Interrupt Timer Control, Index: 62

Bit	Function	Default
7:4	Bits (Suspend Timer Period) 0000: 3.8 min. 0001: 7.5 min. 0010: 15 min. 0011: 30 mins. 0100: 60 mins. 0101: 120 mins. 0110: 240 mins. 0111: 480 mins. 0000: 1 sec. 1001: 1.8 sec. 1010: 3.5 sec. 1011: 7 sec. 1100: 14 sec. 1101: 28 sec. 1110: 56 sec. 1111: 2 min.	0000
3:0	Bits (Interrupt Timer Period) 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 54 usec. 0110: 107 usec. 0111: 215 usec. 0000: 430 usec. 1001: 860 usec. 1010: 1.7 msec. 1011: 3.4 msec. 1100: 7 msec. 1101: 14 msec. 1110: 28 msec. 1111: 55 msec.	0000

The suspend timer is enabled when register 64 bit 1=0. When enabled, the suspend timer always follows the stand-by timer (i.e., it will not start counting until the stand-by timer has reached its terminal count. For hardware Power-down mode, the 82C597 will assert $\overline{\text{STOPCLK}}$ after the suspend timer has reached its terminal count. For software Power-down mode, the 82C597 will generate an $\overline{\text{SMI}}$ after its terminal count. $\overline{\text{STOPCLK}}$ and other power-down features can be implemented in $\overline{\text{SMI}}$ subroutines.

The interrupt timer is used for interrupt service routines. When the INTR input becomes active, the 82C597 will deassert $\overline{\text{STOPCLK}}$ and start the interrupt timer. After the interrupt timer reaches its terminal count, the 82C597 will assert $\overline{\text{STOPCLK}}$ again (if no event occurs during the interrupt period). This timer is used for both hardware and software Power-down modes and is enabled by register 63, Bit 2.

Register 63: Power-down Mode and DRAM Non-cachable Control, Index: 63

Bit	Function	Default
7	Bits 0: Disable hardware Power-down mode 1: Enable hardware Power-down mode	0
6	Bits 0: Disable software Power-down mode 1: Enable software Power-down mode	0
5	Bits 0: Disable interrupt input (INTR) 1: Enable interrupt input (INTR) Should be 1 when Power-down mode is enabled	0
4	Should be 0	0
3	Bits 0: $\overline{\text{SLOWCLK}}$ does not change when input INTR active 1: $\overline{\text{SLOWCLK}}$ will be inactive when input INTR active	0
2	Bits 0: Enable interrupt timer (default) 1: Disable interrupt timer	0
1	0: Top 128K DRAM is not cachable 1: Top 128K DRAM is cachable	0
0	Must have the same value as bit 6.	

Hardware Power-down mode allows $\overline{\text{STOPCLK}}$ and $\overline{\text{SLOWCLK}}$ to be controlled by the 82C597 hardware. Software Power-down mode will use System Management Mode ($\overline{\text{SMM}}$) subroutines to implement power-down control.

Register 64: Power-Down Mode Control, Index: 64

Bit	Function	Default
7	Bits Software initial $\overline{\text{SMI}}$ 0: Normal 1: Writing an 1 to this bit will generate an $\overline{\text{SMI}}$ to CPU. After a 1 is written, software should write a 0 to this bit.	0
6	Bits $\overline{\text{SMI}}$ inactive control 0: Normal 1: Writing a 1 to this bit will deassert the $\overline{\text{SMI}}$ signal. This is the only way to cause the 82C597 to deassert $\overline{\text{SMI}}$. After a 1 is written, 0 should be written to this bit.	0
5	Bits $\overline{\text{STOPCLK}}$ Active Control 0: Normal 1: Writing a 1 to this bit will assert $\overline{\text{STOPCLK}}$. Software should subsequently write a 0 to this bit to allow $\overline{\text{STOPCLK}}$ to be deasserted.	0
4	Bits Software $\overline{\text{STOPCLK}}$ Inactive Control 0: Normal 1: Writing a 1 will deassert $\overline{\text{STOPCLK}}$. Software should subsequently write a 0 to this bit to allow $\overline{\text{STOPCLK}}$ to be asserted.	0
3	Bits Software $\overline{\text{SLOWCLK}}$ Active Control 0: Normal 1: Writing a 1 will assert $\overline{\text{SLOWCLK}}$. Software should subsequently write a 0 to this bit to allow $\overline{\text{SLOWCLK}}$ to be deasserted.	0
2	Bits Software $\overline{\text{SLOWCLK}}$ Inactive Control 0: Normal 1: Writing a 1 will deassert $\overline{\text{SLOWCLK}}$. Software should subsequently write a 0 to this bit to allow $\overline{\text{SLOWCLK}}$ to be asserted.	0
1	Bits Suspend Timer Control 0: Enable suspend timer (default) 1: Disable suspend timer The 82C597 allows a second Suspend mode to be started after current suspend timer has reached its terminal count (i.e. When the current suspend timer expires, it will assert $\overline{\text{SMI}}$.) Within the $\overline{\text{SMI}}$ subroutine, the suspend timer can be disabled and the suspend timer reenabled. After the new terminal count has been reached, the 82C597 will initiate another $\overline{\text{SMI}}$.	0
0	Bits Disable Software Reset Mask 0: Normal 1: Force 82C597 to activate pin 153. This bit should be set to 1, then set to 0 before leaving the SMI subroutine.	0

Register 65: Power Management Control, Index: 65

Bit	Function	Default
7	Bits 0: Disable $\overline{\text{SMIACT}}$/$\overline{\text{SMADS}}$ input signal 1: Enable $\overline{\text{SMIACT}}$/$\overline{\text{SMADS}}$ input signal	0
6	Bits 0: INTEL SMM mode 1: Cyrix/AMD SMM mode	0
5	Bits 0: Disable quick power-down mode 1: Enable quick power-down mode when power-down key is pushed.	0
4	Reserved, must be 0	0
3:0	Reserved	0000

Register 66: Special Memory and I/O Event Detection, Index; 66

Bit	Function	Default
7:0	Memory cycle: memory address A31, A26, A25, A24, A23, A22, A21, A20 detection. I/O cycle: I/O address A7, A6, A5, A4, A3, A2, A1, A0 detection.	00000000

Register 67: Special Memory and I/O Event Detection, Index: 67

Bit	Memory Cycle	I/O Cycle	Default
7	Mask A31	A15	0
6	Mask A26	A14	0
5	Mask A25	A13	0
4	Mask A24	A12	0
3	Mask A23	A11	0
2	Mask A22	A10	0
1	Mask A21	A9	0
0	Mask A20	A8	0

Register 68: Special Memory and I/O Event Detection, Index: 68

Bit	Function	Default
7	Bits 0: Disable special memory I/O detection 1: Enable special memory I/O detection	0
6	Bits 0: Detect I/O cycle 1: Detect memory cycle	0
5	Bits 0: No write cycle detection 1: Detect write cycles	0
4	Bits 0: No read cycle detection 1: Detect ready cycles	0
3	I/O address A19	0
2	I/O address A18	0
1	I/O address A17	0
0	I/O address A16	0

Registers 66, 67, and 68 allow for special memory or I/O event detection. For memory detection, address A31, A26, A25, A24, A23, A22, A21, and A20 are monitored. Memory detection can also be limited to read cycles or write cycles. Certain memory addresses can also be masked. (Register 67) If the corresponding mask bit (e.g., mask A20) is set, then address (A20) will not be decoded. For I/O detection, addresses A19−A0 can be monitored. I/O detection can also be limited to read-only or write-only. I/O detection does not allow for address masking.

Register 69: Scratch Pad Register, Index: 69

Bit	Function	Default
7:0	This register is readable/writable and can be used by BIOS as a scratch register.	00000000

Register 6A: 82C597 Status Register, Index: 6A

Read Cycle:	Set A	Set B
Bit 7=1	SMI caused by start of stand-by mode	SMI caused by timer 5 reaching its terminal count
Bit 6=1	SMI caused by end of stand-by mode	SMI caused by timer 5 reset by an event
Bit 5=1	SMI caused by suspend timer reaching its terminal count	82C597 is in power-down mode (stand-by or suspend mode)
Bit 4=1	SMI caused by register 64, bit 7	82C597 is in suspend mode. Once in suspend mode, this bit will stay 1 unless any suspend event becomes active, or power-down mode is disabled.
Bit 3=1	SMI caused by timer 3 reaching its terminal count	$\overline{\text{STOPCLK}}$ pin is active
Bit 2=1	SMI caused by timer 3 reset by an event	$\overline{\text{SLOWCLK}}$ pin is active
Bit 1=1	SMI caused by timer 4 reaching its terminal count	Suspend timer has reached its terminal count. It will be 0 if register 64, bit 1 is set to 1 later.
Bit 0=1	SMI caused by timer 4 reset by an event	$\overline{\text{SMI}}$ pin is active

The CY82C597 has two status registers (16 bits total) that can be read through register 6A. Writing a 0 into bit 7 will cause A status set to be read on a read cycle. Writing a 1 into bit 7 will cause B status set to be read on a read cycle.

Register 6A contains the source of an $\overline{\text{SMI}}$ and some internal status. The status can be used to power-down/power-up individual system devices (monitor, CPU, hard disk, etc.).

Register 6B: DRAM Bank 2/3 Control, Index: 6B

Bit	Function	Default
7	Reserved	0
6:4	Bits 000: Disable Bank 3 001: Bank 3 is 256KB 010: Bank 3 is 1MB 011: Bank 3 is 4MB 100: Reserved 101: Bank 3 is 512KB 110: Bank 3 is 16MB 111: Bank 3 is 2MB	000
3	Bits 0: Disable Bank 2 and 3 1: Enable Bank 2 and 3	0
2:0	Bits 000: Disable Bank 2 001: Bank 2 is 256KB 010: Bank 2 is 1MB 011: Bank 2 is 4MB 100: Reserved 101: Bank 2 is 512KB 110: Bank 2 is 16MB 111: Bank 2 is 2MB	000

Register 6C: DRAM Bank Remap Register, Index: 6C

Bit	Function	Default
7:6	00: Bank 3 $\overline{RAS}$ is mapped to $\overline{RAS0}$ 01: Bank 3 $\overline{RAS}$ is mapped to $\overline{RAS1}$ 10: Bank 3 $\overline{RAS}$ is mapped to $\overline{RAS2}$ 11: Bank 3 $\overline{RAS}$ is mapped to $\overline{RAS3}$	11
5:4	00: Bank 2 $\overline{RAS}$ is mapped to $\overline{RAS0}$ 01: Bank 2 $\overline{RAS}$ is mapped to $\overline{RAS1}$ 10: Bank 2 $\overline{RAS}$ is mapped to $\overline{RAS2}$ 11: Bank 2 $\overline{RAS}$ is mapped to $\overline{RAS3}$	10
3:2	00: Bank 1 $\overline{RAS}$ is mapped to $\overline{RAS0}$ 01: Bank 1 $\overline{RAS}$ is mapped to $\overline{RAS1}$ 10: Bank 1 $\overline{RAS}$ is mapped to $\overline{RAS2}$ 11: Bank 1 $\overline{RAS}$ is mapped to $\overline{RAS3}$	01
1:0	00: Bank 0 $\overline{RAS}$ is mapped to $\overline{RAS0}$ 01: Bank 0 $\overline{RAS}$ is mapped to $\overline{RAS1}$ 10: Bank 0 $\overline{RAS}$ is mapped to $\overline{RAS2}$ 11: Bank 0 $\overline{RAS}$ is mapped to $\overline{RAS3}$	00

By allowing any DRAM logical bank to be remapped to any physical bank, DRAM modules can be installed in any empty socket. There are no limitations on the order of DRAM banks.

Register 6D: First Level Write-back (L1WB) CPU Control, Index: 6D

Bit	Function	Default
7	Bits 0: Update inquiry filter on memory read cycles 1: Update inquiry filter on memory read/write cycles	0
6	Bits 0: For 82C597 PCI mode (82C597 and 82C596) 1: For 82C597 VESA mode (82C597, only) and register 6D, Bit (0)=1	0
5	Reserved	0
4	$\overline{HITM}$ detection control 0: Normal 1: Delay $\overline{HITM}$ detection by 1 cycle (for AMD write-back CPUs)	0
3	Reserved, must be 0	0
2	Bits 0: Disable inquiry filter 1: Enable inquiry filter	0
1	Bits 0: Disable CPU bus burst-write support 1: Enable CPU bus burst-write support	0
0	Bits 0: Disable L1WB CPU support logic 1: Enable L1WB CPU support logic	0

Register 6E: Shadow RAM Block D, C Control, Index: 6E

Bit	Function	Default
7	Register 15, Bit 1 control (Block C RAM R/W control) Bits 0: Enable Register 15, Bit 1 1: Disable Register 15, Bit 1 (Replaced by Register 6E, Bit 6)	0
6	Block C RAM enable control (see Bit 7) Bits 0: Read or Write 1: Read only	0
5	Shadow RAM at DC000H−DFFFFH control Bits 0: Disable. Will access AT Bus memory 1: Enable.	0
4	Shadow RAM at D8000H−DBFFFH control Bits 0: Disable. Will access AT Bus memory 1: Enable.	0
3	Shadow RAM at D4000H−D7FFFH control 0: Disable. Will access AT Bus memory 1: Enable.	0
2	Shadow RAM at D0000H−D3FFFH control 0: Disable. Will access AT Bus memory 1: Enable.	0
1	Block D RAM access control (D0000H−DFFFFH) 0: Read or Write 1: Read only	0
0	Block D RAM/ROM control 0: Access RAM. For those disabled RAM, access will go to AT Bus memory. 1: Access on board ROM.	0

Register 6F: Shadow RAM Block E Control, Index: 6F

Bit	Function	Default
7	Block D cachable control Bits 0: Non-cachable 1: Cachable	0
6	Block E cachable control Bits 0: Non-cachable 1: Cachable	0
5	Shadow RAM at EC000H−EFFFFH control Bits 0: Disable. Will access AT Bus memory 1: Enable.	0
4	Shadow RAM at E8000H−EBFFFH control Bits 0: Disable. Will access AT Bus memory 1: Enable.	0
3	Shadow RAM at E4000H−E7FFFH control 0: Disable. Will access AT Bus memory 1: Enable.	0
2	Shadow RAM at E000H−E3FFFH control 0: Disable. Will access AT Bus memory 1: Enable.	0
1	Block E RAM access control (E0000H−EFFFFH) 0: Read or Write 1: Read only	0
0	Block E RAM/ROM control 0: Access RAM. When RAM is disabled, accesses will go to AT Bus memory. 1: Access on board ROM.	0

Register 70: DRAM and Miscellaneous Control, Index: 70

Bit	Function	Default
7	Bits 0: Normal 1: Enable 2MB DRAM with 11 row address and 10 column address	0
6	Bits 0: Normal 1: Enable 2MB DRAM with 12 row address and 9 column address	0
5	Bits 0: Normal 1: Enable 1MB DRAM with 11 row address and 9 column address	0
4	Bits 0: Normal 1: Enable 1MB DRAM with 12 row address and 8 column address	0
3	Reserved	0
2	Bits 0: Normal 1: Remap address Block 0004XXXX to 000AXXXX, remap address Block 0005XXXX to 000BXXXX.	0
1	Reserved	0
0	Reserved	0

Register 71: Timer 3 Event Detection Control, Index: 71

Bit	Function	Default
7	Bits 0: Disable key-board event detection 1: Enable key-board event detection	0
6	Bits 0: Disable serial port event detection 1: Enable serial port event detection	0
5	Bits 0: Disable parallel port event detection 1: Enable parallel port event detection	0
4	Bits 0: Disable hard disk event detection 1: Enable hard disk event detection	0
3	Bits 0: Disable DMA/ISA master event detection 1: Enable DMA/ISA master event detection	0
2	Bits 0: Disable non-motherboard memory event detection 1: Enable non-motherboard memory event detection	0
1	Reserved	0
0	Bits 0: Disable video memory (Block A,B) event detection 1: Enable video memory (Block A,B) event detection	0

Register 72: Timer 3 Control, Index: 72

Bit	Function	Default
7:4	Bits Terminal Time 0000: 1 sec. 0001: 1.8 sec 0010: 3.5 sec 0011: 7 sec. 0100: 14 sec. 0101: 28 sec. 0110: 56 sec. 0111: 2 min. 1000: 3.8 min. 1001: 7.5 min. 1010 15 min. 1011: 30 min. 1100: 60 min. 1101: 120 min. 1110: 240 min. 1111: 480 min.	0
3	Bits 0: Disable timer 3 1: Enable timer 3	0
2	Bits 0: Disable special memory I/O event detection (please see register 66, 67, and 68) 1: Enable special memory I/O event detection	0
1	Bits 0: Disable I/O event detection (please see registers 60 and 61) 1: Enable I/O event detection	0
0	Bits 0: Disable VESA master event detection 1: Enable VESA master event detection	0

Register 73: Timer 4 Event Detection Control, Index: 73

Bit	Function	Default
7	Bits 0: Disable key-board event detection 1: Enable key-board event detection	0
6	Bits 0: Disable serial port event detection 1: Enable serial port event detection	0
5	Bits 0: Disable parallel port event detection 1: Enable parallel port event detection	0
4	Bits 0: Disable hard disk event detection 1: Enable hard disk event detection	0
3	Bits 0: Disable DMA/ISA master event detection 1: Enable DMA/ISA master event detection	0
2	Bits 0: Disable non-motherboard memory event detection 1: Enable non-motherboard memory event detection	0
1	Reserved	0
0	Bits 0: Disable video memory (Block A,B) event detection 1: Enable video memory (Block A,B) event detection	0

Register 74: Timer 4 Control, Index: 74

Bit	Function	Default
7:4	Bits Terminal Time 0000: 1 sec. 0001: 1.8 sec 0010: 3.5 sec 0011: 7 sec. 0100: 14 sec. 0101: 28 sec. 0110: 56 sec. 0111: 2 min. 1000: 3.8 min. 1001: 7.5 min. 1010 15 min. 1011: 30 min. 1100: 60 min. 1101: 120 min. 1110: 240 min. 1111: 480 min.	0000
3	Bits 0: Disable timer 4 1: Enable timer 4	0
2	Bits 0: Disable special memory I/O event detection (please see register 66, 67, and 68) 1: Enable special memory I/O event detection	0
1	Bits 0: Disable I/O event detection (Please see register 60, 61) 1: Enable I/O event detection	0
0	Bits 0: Disable VESA master event detection 1: Enable VESA master event detection	0

Register 75: Timer 5 Event Detection Control, Index: 75

Bit	Function	Default
7	Bits 0: Disable key-board event detection 1: Enable key-board event detection	0
6	Bits 0: Disable serial port event detection 1: Enable serial port event detection	0
5	Bits 0: Disable parallel port event detection 1: Enable parallel port event detection	0
4	Bits 0: Disable hard disk event detection 1: Enable hard disk event detection	0
3	Bits 0: Disable DMA/ISA master event detection 1: Enable DMA/ISA master event detection	0
2	Bits 0: Disable non-motherboard memory event detection 1: Enable non-motherboard memory event detection	0
1	Reserved	0
0	Bits 0: Disable video memory (Block A,B) event detection 1: Enable video memory (Block A,B) event detection	0

Register 76: Timer 5 Control, Index: 76

Bit	Function	Default
7:4	Bits Terminal Time 0000: 1 sec. 0001: 1.8 sec 0010: 3.5 sec 0011: 7 sec. 0100: 14 sec. 0101: 28 sec. 0110: 56 sec. 0111: 2 min. 1000: 3.8 min. 1001: 7.5 min. 1010 15 min. 1011: 30 min. 1100: 60 min. 1101: 120 min. 1110: 240 min. 1111: 480 min.	0000
3	Bits 0: Disable timer 5 1: Enable timer 5	0
2	Bits 0: Disable special memory I/O event detection (please see register 66, 67, and 68) 1: Enable special memory I/O event detection	0
1	Bits 0: Disable I/O event detection (Please see register 60, 61) 1: Enable I/O event detection	0
0	Bits 0: Disable VESA master event detection 1: Enable VESA master event detection	0

Register 77: Power-Down Control, Index: 77

Bit	Function	Default
7	Bits Timer 5 event control 0: Normal 1: Timer 5 will ignore all events (once enabled, timer 5 will start counting until it reaches the specified terminal count. No events will reset the timer.).	0
6	Bits Timer 4 event control 0: Normal 1: Timer 4 will ignore all events (once enabled, timer 4 will start counting until it reaches the specified terminal count. No events will reset the timer.).	0
5	Bits SMI retry timer 0: Disable SMI retry timer 1: Enable SMI retry timer	0
4:3	Bits SMI retry timer terminal count 00: 55 msec. 01: 0.2 msec 10: 1 sec. 11: 3.5 sec Once the SMI retry timer is enabled and any system management interrupt ($\overline{SMI}$) is active longer than the value specified by $\overline{SMI}$ retry timer, the 82C597 will generate a new $\overline{SMI}$.	00
2	Bits $\overline{STOPCLK}$ timer control 0: Disable $\overline{STOPCLK}$ timer 1: Enable $\overline{STOPCLK}$ timer	0
1:0	Bits $\overline{STOPCLK}$ timer 00: 430 usec. 01: 860 usec. 10: 1.7 msec. 11: 7 msec. In software power-down mode, the assertion of $\overline{STOPCLK}$ can be delayed. The delay time is determined by $\overline{STOPCLK}$ timer.	00

Register 78: Non-Cachable/Non-Local Block 1 Starting Address, Index: 78[21, 22, 23]

Bit	Function	Default
7:0	Bits 7 6 5 4 3 2 1 0 A23 A22 A21 A20 A19 A18 A17 A16	00000000

Notes:
21. Bits 0, 1, 2, 3, 4, and 5 may not be needed. Please see note on Register 79.
22. A24 of the non-cachable/non-local Block 1 starting address is bit 0 of Register 79.
23. A25 and A26 of the non-cachable/non-local Block 1 starting address are bits 6 and 7 of Register 79.

Register 79: Non-Cachable Block 1 Starting Address and Size, Index: 79[24]

Bit	Function	Default
7	Non-cachable/non-local Block 1 starting address A26	0
6	Non-cachable/non-local Block 1 starting address A25	0
5	Non-cachable Block 1 dual Functions control: 0: For non-cachable Block 1: For non-local memory Block	0
4	Non-cachable non-local Block 1 control 0: Disable. 1: Enable.	0
3:1	Non-cachable size Bits 321 Size 000: 64KB 010: 128KB 100: 256KB 110: 512KB 001: 1MB 011: 2MB	000
0	Non-cachable/non-local Block 1 starting address A24.	0

Register 7B: Miscellaneous Control Register, Index: 7B

Bit	Function	Default
7	Reserved	0
6	Reserved	0
5	1: Enable Non-turbo speed set-up 0: Disable Non-turbo speed set-up	0
4	1: Non-turbo speed 0: Normal speed	0
3	1: Disable OSC119 output 0: Enable OSC119 output	0
2	1: Enable 0 ws input 0: Disable 0 ws input	0
1:0	Reserved	00

Register 7C: Reserved, Index: 7C

Bit	Function	Default
7:4	Not implemented	0
3	Reserved	0
2	Reserved, BIOS shall set to 1	0
1	Reserved, BIOS shall set to 1	0
0	Reserved	0

Note:

24. For 64KB non-cachable size, the starting address is bound by A24−A16 from the configuration registers.
For 128KB non-cachable size, the starting address is bound by A24−A17 from the configuration registers.
For 256KB non-cachable size, the starting address is bound by A24−A18 from the configuration registers.
For 512KB non-cachable size, the starting address is bound by A24−A19 from the configuration registers.
For 1MB non-cachable size, the starting address is bound by A24−A20 from the configuration registers.
For 2MB non-cachable size, the starting address is bound by A24−A21 from the configuration registers.

Please note that the non-cachable size is independent of cache size. The non-cachable starting address and non-cachable size are used to define an address range that will not be cached.

When Register 79, bit 4 is set to 1, the non-cachable block will be changed to a non-local block. All addresses within this block will not be on the motherboard, i.e., they will go to the AT bus, VESA bus, or PCI bus.

CY82C597 Pin Descriptions

Clock and Reset

Name	I/O	Pin Number	Description
CLK	I	9	Clock input for internal state machines. A 386 system needs a 2x clock, a 486 system needs a 1x clock.
ATCLK	O	148	Clock signal to the AT bus. Frequency is controlled by register 10, bit [0:1].
OSC	I	133	This input should be connected to a 14.318 MHz oscillator. It is used to generate OSC119.
OSC119	O	151	14.318 MHz divided by 12 output (1.19 MHz). This signal should be connected to the timer clock input (TMRCLK) of the 83C206.
PWRGD	I	128	Power good signal from the power supply or reset key. When LOW, it will activate CPURST, $\overline{\text{SYSRST}}$, and 387 reset ($\overline{\text{NPRLD}}$).
CPURST	O	14	This is an active HIGH signal to reset the CPU. When PWRGD is LOW, keyboard reset is active, or there is a shutdown, CPURST will be activated.
$\overline{\text{SYSRST}}$	O	129	This is an active LOW signal. It is asserted when PWRGD is LOW. This signal is used to reset all ISA peripheral cards.
A26/$\overline{\text{AEN16}}$	I/O	80	This is the CPU A26 input signal during CPU cycles and the $\overline{\text{AEN16}}$ input signal during DMA cycles.

Numerical Coprocessor Interface

Name	I/O	Pin Number	Description
$\overline{\text{NPRDYLC}}$	I	8	A dual function pin. During numerical coprocessor cycles, it is the numerical processor ready input ($\overline{\text{NPRDY}}$). During local bus cycles, it is the local bus device input ($\overline{\text{LOCAL}}$). Each $\overline{\text{LDEV}}$ signal from the VESA slots should be ANDed together to provide $\overline{\text{LOCAL}}$. The $\overline{\text{NPRDY}}$ and $\overline{\text{LOCAL}}$ should be ANDed externally and connected to this pin.
B387NS4/MA11	I	7	A dual function pin that is latched by the rising edge of PWRGD. For a 386 system, this pin should be tied HIGH through a 10KΩ resistor. After the power-up sequence, this pin operates as the $\overline{\text{BUSY387}}$, a signal from the 387 numerical coprocessor that indicates the 387 is still performing an operation. For a 486 system, this pin should be tied to Ground (V_{SS}) through a 1KΩ resistor. After power-up, this pin becomes the MA11 output.
$\overline{\text{B3IG}}$	O	12	A dual function pin. For 486 systems, it is an output ($\overline{\text{IGNNE}}$) to tell the 486 to ignore numerical errors and continue executing non-control floating point instructions. For 386 systems, it is an output ($\overline{\text{BUSY386}}$) that tells the 386 that the 387 is still busy.
$\overline{\text{E387FER}}$	I	13	A dual function pin. For 486 systems, it is an input ($\overline{\text{FERR}}$) from the 486 that indicates that there is a floating point error. For 386 systems, it is an input ($\overline{\text{ERR387}}$) that indicates that a 387 error has occurred.
INT13	O	131	Numerical coprocessor interrupt request to the 83C206.

CPU Control

Name	I/O	Pin Number	Description
A31	I	32	CPU address line 31.
A[24:21]	I	33−36	CPU address lines [24:21].
A20	I/O	37	CPU address line 20. Output during DMA/MASTER cycles for 386 systems.
A19	I	38	CPU address line 19.
A18	I	49	CPU address line 18.
A17	I	51	CPU address line 17.
A[16:2]	I/O	52−66	CPU address lines [16:2]. Outputs during DMA/MASTER cycles.
BE[3:0]	I/O	28−31	Byte enable [3:0]. Inputs during CPU cycles. Outputs during DMA/MASTER.
$\overline{ADS}$	I/O	27	CPU address strobe. Output during DMA/MASTER accesses on the VESA local bus.
$\overline{MIO}$	I/O	23	CPU memory I/O cycle status. Output during DMA/MASTER accesses on the VESA local bus cycles.
$\overline{DC}$/ADSTB	I	22	This pin is the CPU data/code status input during CPU cycles and the ADSTB signal during DMA cycles.
$\overline{WR}$	I/O	24	CPU write/read status. Output during DMA/MASTER accesses on VESA local bus.
$\overline{CPURDY}$	I/O	18	Ready output to terminate CPU cycle. During local bus/numerical processor cycles, the CY82C597 monitors this signal to see when the cycle has ended.
D[31:18]	I/O	86−99	CPU data bus for read/write data.
D[17:16]	I/O	102−103	CPU data bus for read/write data.
CQ[15:10]	I/O	48−43	Contaq bus or CQ bus [15:10]. The CQ bus sits between the CPU data bus and the AT SD bus. Used also as TAGA[7:2].
CQ[9:8]	I/O	40−39	CQ bus [9:8]. Used also as TAGA[1:0]
CQ[7:3]	I/O	75−79	CQ bus [7:3].
CQ[2:0]	I/O	83−85	CQ bus [2:0]
NMI	O	11	Non-maskable interrupt output to the CPU. When active, it indicates the CY82C597 has detected either a local memory or AT memory parity error.

Bus Arbitration

Name	I/O	Pin Number	Description
DMAHRQ	I	135	DMA hold request from the 83C206.
HOLD	O	16	Hold request to the CPU. Hold goes active due to a refresh request or a de-turbo request.
HLDA	I	25	Hold acknowledge from the CPU.
HLDAOUT	O	132	DMA/MASTER cycle hold acknowledge output to the 83C206. After receiving this signal, the DMA/MASTER can begin its cycle.
$\overline{REFSH}$	I/O	154	$\overline{REFRESH}$, an active LOW signal. An output to the AT bus during non-master cycles. An input during MASTER cycles.

DRAM Control

Name	I/O	Pin Number	Description
$\overline{\text{DWROMKB}}$	O	115	A dual function pin. In the 82C597 PCI mode, this signal is the $\overline{\text{DWE}}$ (DRAM write enable) during DRAM write cycles and the $\overline{\text{ROMCS}}$ (ROM chip select) signal during ROM access cycles. When the 82C597 is used without a CY82C599 present in the system, this signal is used as $\overline{\text{DWE}}$, $\overline{\text{ROMCS}}$, and $\overline{\text{KBCS}}$ (keyboard controller chip select) during keyboard controller accesses.
$\overline{\text{RAS}}$[1:0]	O	108−109	DRAM bank 1,0 row address strobe.
$\overline{\text{CAS0}}$	O	110	DRAM bank 0,1 column address strobe 0.
$\overline{\text{CAS1}}$	O	111	DRAM bank 0,1 column address strobe 1.
$\overline{\text{CAS2}}$	O	113	DRAM bank 0,1 column address strobe 2.
$\overline{\text{CAS3}}$	O	114	DRAM bank 0,1 column address strobe 3.
MA10	I/O	116	DRAM address line 10. When this pin is pulled down through a 1KΩ resistor, CY82C597 will use MP[3:0] as VESA Bus Master arbitration signals. This pin is an input only during system reset.
MA9	I/O	117	DRAM address line 9. This pin must be pulled down through a 1KΩ resistor for 128-MB of DRAM.
MA8	I/O	118	DRAM address line 8.
MA[7:6]	O	119−120	During power on, tying MA[7:6] HIGH or LOW through pull-up/pull-down resistors sets different internal 82C597 modes according to the following table: MA7 MA6 0 0 82C597 stand-alone 0 1 82C597 PCI mode (in conjunctions with an 82C599). 1 X 82C596 emulation mode. During normal operation, MA[7:6] are used as DRAM address lines [7:6]. When the CY82C597 is configured for 596 mode, it can support 2 banks of DRAM up to 128 MB total. Please see the CY82C596 spec for 596 mode configuration.
MA5	I/O	122	DRAM address bit 5.
MA4/TOUT2	I/O	123	DRAM address line 4. In 597 mode, this pin is also used as the TOUT2 input signal during AT cycles.
MA3/$\overline{\text{IOCS16}}$	I/O	124	DRAM address line 3. In 597 mode, this pin is also used as the $\overline{\text{IOCS16}}$ input signal during AT cycles.
MA2/$\overline{\text{MCS16}}$	I/O	125	DRAM address line 2. In 597 mode, this pin is also used as the $\overline{\text{MCS16}}$ input signal during AT cycles.
MA1/RTCAS	I/O	126	DRAM address line 1. In 597 mode, this pin is also used as the RTCAS input signal during AT cycles.
MA0/$\overline{\text{INTA}}$	I/O	127	DRAM address line 0. In 597 mode, this pin is also used as the $\overline{\text{INTA}}$ input signal during AT cycles.
MP[3:0]	I/O	104−107	DRAM parity bits [3:0]. During DRAM read cycles, they are inputs. The CY82C597 will generate byte parity bits from D[31:0] and compare them with MP[3:0]. If a mismatch occurs and NMI reporting is enabled, the CY82C597 will generate an NMI to the CPU. During DRAM write cycles, the CY82C597 will generate byte parity bits from D[31:0] and put them on MP[3:0] and write them into the DRAM. When register 10, bit 6=1 and MA10 is pulled down through a 1KΩ resistor, these 4 signals are used as VESA bus master arbitration signals: MP0 =VESA bus master 2 request to CY82C597 MP1 =VESA bus master 1 request to CY82C597 MP2 = VESA bus master 2 grant from CY82C597 MP3 = VESA bus master 1 grant from CY82C597 If parity and VESA bus master capability are both required, an external PAL is needed to handle the VESA arbitration.

DRAM Control (continued)

Name	I/O	Pin Number	Description
$\overline{\text{L1MCS}}$	O	152	Indicates the current address is below 1 MB.

Cache Control

Name	I/O	Pin Number	Description
$\overline{\text{CRD0}}$	O	67	Cache read for the even bank of SRAMs. Connected to $\overline{\text{OE}}$ of Bank 0 cache data SRAMs.
$\overline{\text{CRD1}}$	O	68	Cache read for the odd bank of SRAMs. Connected to $\overline{\text{OE}}$ of Bank 1 cache data SRAMs.
$\overline{\text{CWE0}}$	O	71	Cache write enable for the even bank of SRAMs.
$\overline{\text{CWE1}}$	O	72	Cache write enable for the odd bank of SRAMs.
TOGA2	O	73	A dual function pin. For 386 systems, it is used to toggle CPU address A2 during cache accesses. For 486 systems with 1 bank of SRAMs, it is address 2 to bank 0. For 486 systems with 2 banks of SRAMs, it is address 3 input to bank 0.
TOGA3	O	74	A dual function pin. For 386 systems, it is used to toggle CPU address A3 during cache accesses. For 486 systems with 1 bank of SRAM, it is address 3 to bank 0. For 486 systems with 2 banks of SRAMs, it is address 3 input to bank 1.
$\overline{\text{TAGWT}}$	O	42	Tag RAM write enable, active LOW. It is active during a cache write hit or cache move in cycle.
$\overline{\text{TAGEN}}$	O	41	An active LOW signal. When active, it will enable the CY82C597 to read/write the Tag RAM.
$\overline{\text{XA20EA}}$	I/O	10	This is a dual function pin. For 486 systems, it is $\overline{\text{EADS}}$ to invalidate a 486 internal cache line. It is active during DMA/MASTER memory write hit cycles. For 386 systems, the CPU is from CYRIX, this pin is the $\overline{\text{EADS}}$ output to invalidate the CPU‘s cache line during DMA/MASTER memory write cycles. If Intel or AMD, this pin the SA20 output or input for DMA/MASTER cycles.
A25/$\overline{\text{AEN8}}$	I/O	15	This is the CPU A25 input signal during CPU cycles and the $\overline{\text{AEN8}}$ input signal during DMA cycles.
$\overline{\text{KEN}}$	O	17	$\overline{\text{KEN}}$ to the 486 to indicate that the cycle is cachable. It can also be connected to C&T 38605 and CYRIX CPU $\overline{\text{KEN}}$ pins making an external PAL unnecessary.
$\overline{\text{RQ3BRDY}}$	I/O	19	A dual function pin. For 486 systems, it is an I/O pin, $\overline{\text{BRDY}}$. During VESA local cycles, it is an input that monitors $\overline{\text{BRDY}}$ from the local device and determines when the cycle has terminated. During local memory cycles, it is an output that terminates the burst transfer. For 386 systems, it is an output connected to PEREQ of the 386.
RQ387BL	I	26	A dual function pin. For 486 systems, it is an input signal ($\overline{\text{BLAST}}$) from the 486. When active, it tells the CY82C597 that the next cycle will be the last burst cycle. For 386 systems, it is an input from the 387 (PRQ387) that requests a data operand to be transferred to/from memory by the 386.

AT Control

Name	I/O	Pin Number	Description
XA0	I/O	144	System address line 0. It is an input during MASTER and 8 bit DMA cycles, otherwise it is an output.
XA1	I/O	145	System address line 1. It is an input during DMA/MASTER cycles, otherwise it is an output.
$\overline{\text{MEMR}}$	I/O	141	AT memory read command. It is an input during DMA/MASTER cycles, otherwise it is an output.
$\overline{\text{MEMW}}$	I/O	140	AT memory write command. It is an input during DMA/MASTER cycles, otherwise it is an output.

AT Control (continued)

Name	I/O	Pin Number	Description
$\overline{\text{IOR}}$	I/O	142	AT I/O read command. It is an input during DMA/MASTER cycles, otherwise it is an output.
$\overline{\text{IOW}}$	I/O	143	AT I/O write command. It is an input during DMA/MASTER cycles, otherwise it is an output.
ALE	O	158	AT bus address latch enable. Indicates the start of an AT bus cycle.
$\overline{\text{IOCS16}}$/$\overline{\text{LRDY}}$	I	1	In 597 mode, this is the ready input signal from the local bus. In 597 PCI mode, this is the signal from the AT bus to indicate a 16-bit AT I/O cycle.
$\overline{\text{MCS16}}$/INTR	I	160	In 597 mode, this is the interrupt request signal for the 83C206. In 597 PCI mode, this is the signal from the AT bus to indicate a 16-bit AT memory cycle.
0WS/$\overline{\text{HITM}}$	I	155	This pin is the $\overline{\text{HITM}}$ input signal when the CY82C597 interfaces to a CPU that has a level 1, write-back cache. Otherwise, it is the AT bus 0WS (zero wait states) input signal.
$\overline{\text{XBHE}}$	I/O	159	AT bus byte high indicator. It is an input during DMA/MASTER cycles, otherwise it is an output.
IOCHRDY	I/O	136	AT bus I/O channel ready input. It is an output during numerical coprocessor reset.
$\overline{\text{IOCHCK}}$	I	153	AT bus I/O channel parity check. When active, it indicates that AT memory has a parity error.
$\overline{\text{INTA}}$/$\overline{\text{STOPCLK}}$	O	146	In 597 mode, this is the $\overline{\text{STOPCLK}}$ signal to CPU. In 597 PCI mode, this is the interrupt acknowledge pulse to the interrupt controller in the 83C206.
TOUT2/$\overline{\text{SLOWCLK}}$	I/O	147	In 597 mode, this is the $\overline{\text{SLOWCLK}}$ output signal. In 597 PCI mode, this is an input from the 83C206 timer 2 output that is used to generate a speaker tone.
TMGATE	O	149	Timer 2 gate control. It is used to enable /disable the tone to the speaker.
RTCAS/$\overline{\text{SMI}}$	I/O	134	In 597 mode, this is the system management interrupt signal. In 597 PCI mode, this is the real-time clock address strobe connected to the 83C206.
$\overline{\text{KBCS}}$/$\overline{\text{ATCYC}}$	O	156	In 597 stand-alone mode, this is an output signal that indicates that a cycle is bound for the AT bus. In 597 PCI mode, this is the keyboard controller chip select signal when an access is targeted for the keyboard controller.
SPKOUT	O	157	Output to speaker.
$\overline{\text{SMIACT}}$/$\overline{\text{SMADS}}$	I	137	This signal indicates that the processor is operating in system management mode (SMM) when the CY82C597 is interfaced to an Intel CPU. It is the SMI address strobe input signal when using a Cyrix or AMD CPU.
$\overline{\text{RAS2}}$	I/O	139	DRAM bank 2 row address strobe.
$\overline{\text{RAS3}}$	I/O	138	DRAM bank 3 row address strobe.
$\overline{\text{SDEN}}$	O	5	An active LOW system data bus enable to turn on/off bidirectional buffers between SD[15:0] and CQ [15:0] bus.
SDIR0N4F	I/O	4	A dual function pin. During 486 power-on reset, if this pin is pulled HIGH by a 51KΩ resistor, ATCLK will be CLK divided by 4/6/8/5 according to register 10, bit 1,0. If this pin is pulled LOW during power-on reset, ATCLK will be changed to CLK divided by 2/3/4/2.5. After power-on reset, this pin becomes SDIR0, which is used to control the LOW byte bus direction: SDIR0=0: for SD[7:0] to CQ[7:0] transfer. SDIR0=1: for CQ[7:0] to SD[7:0] transfer.
SDIR1NCM	I/O	6	A dual function pin. During 386 power-on reset, if this pin is pulled HIGH by 51KΩ resistor, the CY82C597 will know that the CPU manufacturer is Intel or AMD. If this pin is pulled LOW during power-on reset, the CY82C597 will recognize the CPU manufacturer as C&T or CYRIX. After power-on reset, this pin becomes SDIR1, which is used to control the HIGH byte bus direction. SDIR1=0: for SD[15:8] to CQ[15:8] transfer. SDIR1=1: for CQ[15:8] to SD[15:8] transfer.

AT Control (continued)

Name	I/O	Pin Number	Description
$\overline{\text{LDBE}}$	O	82	An active LOW system data bus enable signal to turn on/off the bidirectional buffer between D[15:0] bus and CQ[15:0] bus.
$\overline{\text{SMIMASK}}/\overline{\text{LDIR}}$	I/O	112	In 597 mode, this pin is an output that controls the Data bus to CQ bus buffer direction. In 597 PCI mode, this pin is an input that masks out SMI generation during the reset period.

Ground and V_{CC}

Name	I/O	Pin Number	Description
GND	I	3, 21, 50, 70, 81, 101, 130, and 150	Ground
V_{CC}	I	2, 20, 69, 100, and 121	+5V

CY82C597 DC Characteristics

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... +6.5 V

Ambient Operating Temperature ..... −25°C to +70°C

Ambient Storage Temperature ..... −40°C to 125°C

DC Voltage Applied to Outputs ..... −0.5V to +5.5V

DC Input Voltage ..... −.5V to +5.5V

Electrical Characteristics Over the Operating Range (0°C to 70°C, V_{CC} = +5V ± 5%)

Parameter	Description		CY82C597 Min.	CY82C597 Max.	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{OL}	Output LOW Voltage			0.4	V
V_{OH}	Output HIGH Voltage		2.4		V
I_{IL}	Input Leakage Current			10	µA
I_{OZ}	Three-state Leakage Current			10	µA
C_{IN}	Input Capacitance			20	pF
C_{OUT}	Output Capacitance			20	pF
I_{CC}	Power Supply Current	33 MHz		150	mA
		50 MHz		200	mA

Switching Characteristics

Parameter	Description	CY82C597		Unit
		Min.	Max.	
CLOCK RESET AND TIMING				
T_{100}	CLK period	20		ns
T_{101}	CLK HIGH time at 2.0V	7		ns
T_{102}	CLK LOW time at 0.8V	7		ns
T_{103}	CLK rise time		2	ns
T_{104}	CLK fall time		2	ns
T_{105}	CPURST active delay from CLK	5	15	ns
T_{106}	CPURST inactive delay from CLK	5	15	ns
T_{107}	NPRST active delay from CLK	5	15	ns
T_{108}	NPRST inactive delay from CLK	5	15	ns
AT/DMA ARBITRATION/REFRESH TIMING				
T_{110}	$\overline{ADS}$ set-up time to CLK	5		ns
T_{111}	$\overline{CPURDY}$ active delay from CLK HIGH	5	16	ns
T_{112}	$\overline{CPURDY}$ inactive delay from CLK HIGH	5	14	ns
T_{113}	HOLD active delay from CLK HIGH	5	15	ns
T_{114}	HOLD inactive delay from CLK HIGH	5	15	ns
T_{115}	HLDAOUT active delay from HLDA HIGH	5	20	ns
T_{116}	HLDAOUT inactive delay from HLDA HIGH	5	20	ns
T_{117}	$\overline{REFSH}$ active delay from HLDA HIGH	5	20	ns
T_{118}	$\overline{REFSH}$ inactive delay from ATCLK HIGH	5	20	ns
T_{119}	$\overline{MEMR}$ active delay from ATCLK HIGH	5	20	ns
T_{120}	$\overline{MEMR}$ inactive delay from ATCLK LOW	5	20	ns
T_{121}	$\overline{RAS0}$ to $\overline{RAS1}$ active delay	5	10	ns
T_{122}	$\overline{RAS0}$ to $\overline{RAS1}$ inactive delay	5	10	ns
T_{123}	$\overline{MEMR}$ inactive delay from ATCLK HIGH	5	20	ns
CACHE/DRAM TIMING				
T_{306}	CLK LOW to $\overline{CWE}$ active delay	4	14	ns
T_{307}	CLK HIGH to $\overline{CWE}$ inactive delay	4	14	ns
T_{307A}	CLK LOW to $\overline{CWE}$ inactive delay	4	14	ns
T_{308}	CLK LOW to $\overline{TAGWT}$ active delay	4	14	ns
T_{309}	CLK HIGH to $\overline{TAGWT}$ inactive delay	5	16	ns
T_{310}	CLK HIGH to $\overline{TAGEN}$ active delay	4	14	ns
T_{311}	CLK HIGH to $\overline{TAGEN}$ inactive delay	5	16	ns
T_{312}	CLK LOW to $\overline{CPURDY}$ active delay	4	12	ns
T_{313}	CLK HIGH to $\overline{CPURDY}$ inactive delay	7	16	ns
T_{314}	CLK HIGH to $\overline{CPURDY}$ active delay	5	15	ns
T_{315}	CLK LOW to $\overline{TAGWT}$ inactive delay	5	16	ns
T_{316}	$\overline{BLAST}$ set-up to CLK HIGH	7		ns

Switching Characteristics (continued)

Parameter	Description	CY82C597		Unit
		Min.	Max.	
T_{320}	TAGA[7:0] set-up time to CLK LOW	15		ns
T_{321}	$\overline{CRD}$ active delay from CLK HIGH	5	15	ns
T_{322}	$\overline{CRD}$ inactive delay from CLK HIGH	6	13	ns
T_{323}	TOGA2/TOGA3 delay from CLK HIGH	3	15	ns
T_{324}	$\overline{BRDY}$ active delay from CLK LOW	4	15	ns
T_{325}	$\overline{BRDY}$ inactive delay from CLK HIGH	4	13	ns
T_{330}	CLK HIGH to $\overline{DWROMKB}$ active delay	5	18	ns
T_{331}	CLK HIGH to $\overline{DWROMKB}$ inactive delay	4	14	ns
T_{332}	CLK LOW to $\overline{CAS}$ active delay	6	18	ns
T_{333}	CLK LOW to $\overline{CAS}$ inactive delay	4	15	ns
T_{334}	CLK HIGH to $\overline{CAS}$ active delay	6	18	ns
T_{335}	CLK HIGH to $\overline{CAS}$ inactive delay	4	17	ns
T_{336}	A[31:2] to MA[10:0] delay	5	18	ns
T_{337}	CLK HIGH to $\overline{RAS}$ inactive delay	5	20	ns
T_{338}	CLK HIGH to $\overline{RAS}$ active delay	5	18	ns
T_{339}	CLK HIGH to MA[10:0] delay	5	18	ns
T_{340}	CLK HIGH to $\overline{CRD}$ active delay	4	15	ns
T_{341}	CLK LOW to $\overline{CRD}$ inactive delay	4	13	ns
T_{342}	A[31:3] to TOGA2/TOGA3 delay	5	16	ns
T_{343}	CLK HIGH to TOGA2/TOGA3 valid delay	5	16	ns
T_{344}	CLK HIGH to $\overline{CPURDY}$ active delay	4	16	ns
T_{345}	CLK HIGH to $\overline{CPURDY}$ inactive delay	4	14	ns
T_{346}	CLK LOW to $\overline{TAGWT}$ active delay	4	14	ns
T_{347}	CLK LOW to $\overline{TAGWT}$ inactive delay	4	14	ns
T_{348}	CLK LOW to $\overline{CWE}$ active delay	5	15	ns
T_{349}	CLK LOW to $\overline{CWE}$ inactive	4	13	ns
T_{350}	CLK LOW to $\overline{TAGEN}$ active		18	ns
T_{351}	CLK LOW to CQ[15:8]		18	ns
DMA/MASTER TIMING				
T_{360}	COMMAND active to $\overline{RAS}$ active delay	9	25	ns
T_{361}	COMMAND inactive to $\overline{RAS}$ inactive	9	25	ns
T_{362}	CLK HIGH to MA[10:0] delay	5	18	ns
T_{363}	CLK HIGH to $\overline{CAS}$ active delay	5	20	ns
T_{364}	COMMAND inactive to $\overline{CAS}$ inactive delay	5	22	ns
T_{365}	COMMAND active $\overline{CRD}$ active delay	5	16	ns
T_{366}	COMMAND inactive to $\overline{CRD}$ inactive delay	6	18	ns
T_{367}	COMMAND active to $\overline{DWROMKB}$ active delay	5	20	ns
T_{368}	COMMAND inactive to $\overline{DWROMKB}$ inactive	5	18	ns

Switching Characteristics (continued)

Parameter	Description	CY82C597		Unit
		Min.	Max.	
T_{369}	CLK HIGH to $\overline{CWE}$ active delay	5	19	ns
T_{370}	CLK HIGH to $\overline{CWE}$ inactive delay	5	19	ns
T_{371}	HLDA to $\overline{RAS}$ inactive delay	9	30	ns
DATA CONVERSION TIMING				
T_{400}	CQ[15:0] valid from D[31:0]	5	18	ns
T_{401}	CQ[15:0] hold time to D[31:0]	5	18	ns
T_{406}	D[31:0] valid from CQ[15:0]	5	18	ns
T_{407}	D[31:0] hold time to CQ[15:0]	5	18	ns
NUMERICAL COPROCESSOR TIMING				
T_{500}	IRQ asserted from $\overline{FERR}$ LOW	4	14	ns
T_{501}	IRQ deasserted from CNTL HIGH	4	12	ns
T_{502}	IRQ asserted from WTINTR HIGH	4	14	ns
T_{503}	IRQ deasserted from WTINTR LOW	4	12	ns
T_{504}	$\overline{IGNNE}$ asserted from CNTL HIGH	4	14	ns
T_{505}	$\overline{IGNNE}$ deasserted from $\overline{FERR}$ HIGH	3	12	ns
POWER MANAGEMENT TIMING				
T_{601}	$\overline{SMI}$ delay from CLK HIGH	8	15	ns
T_{602}	$\overline{SMIACT}$ setup to CLK HIGH	5		ns
T_{603}	$\overline{SLOWCLK}$ delay from CLK HIGH	8	15	ns
T_{604}	$\overline{STOPCLK}$ delay from CLK HIGH	8	15	ns

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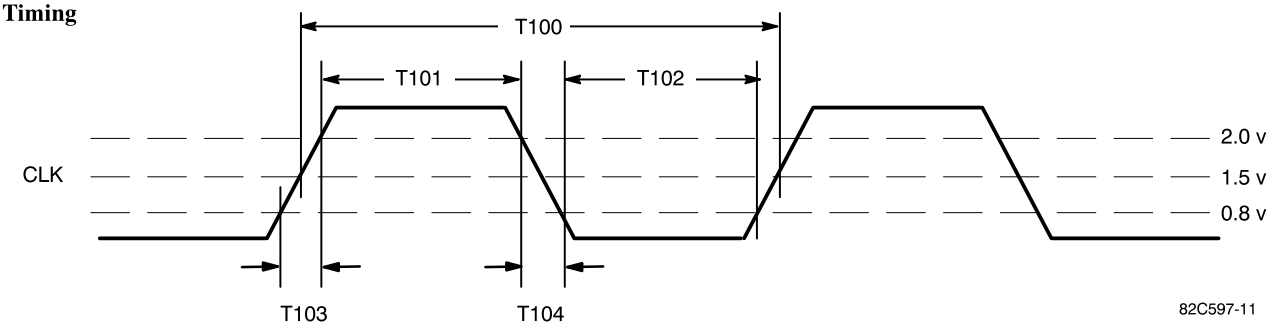
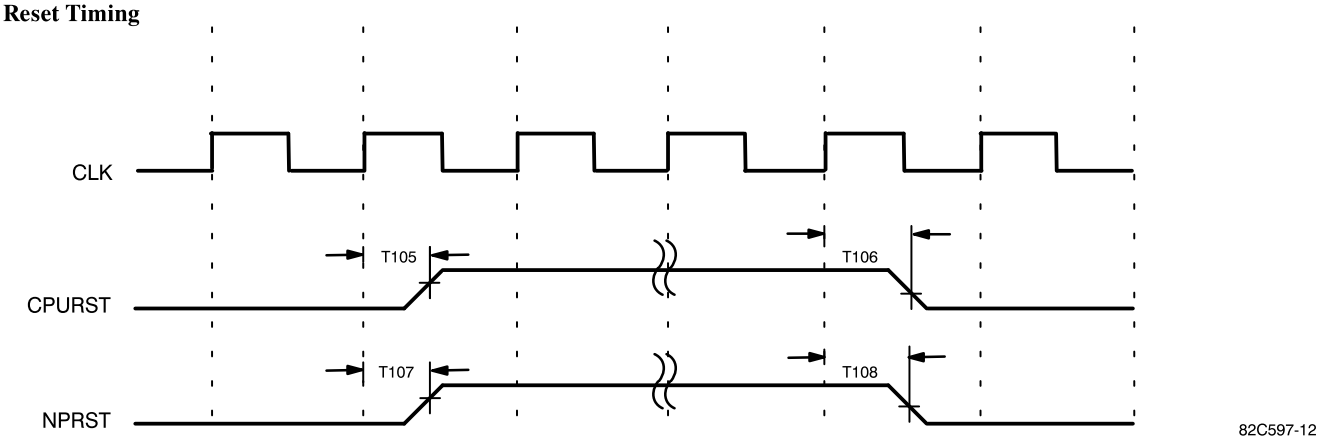
Switching Waveforms

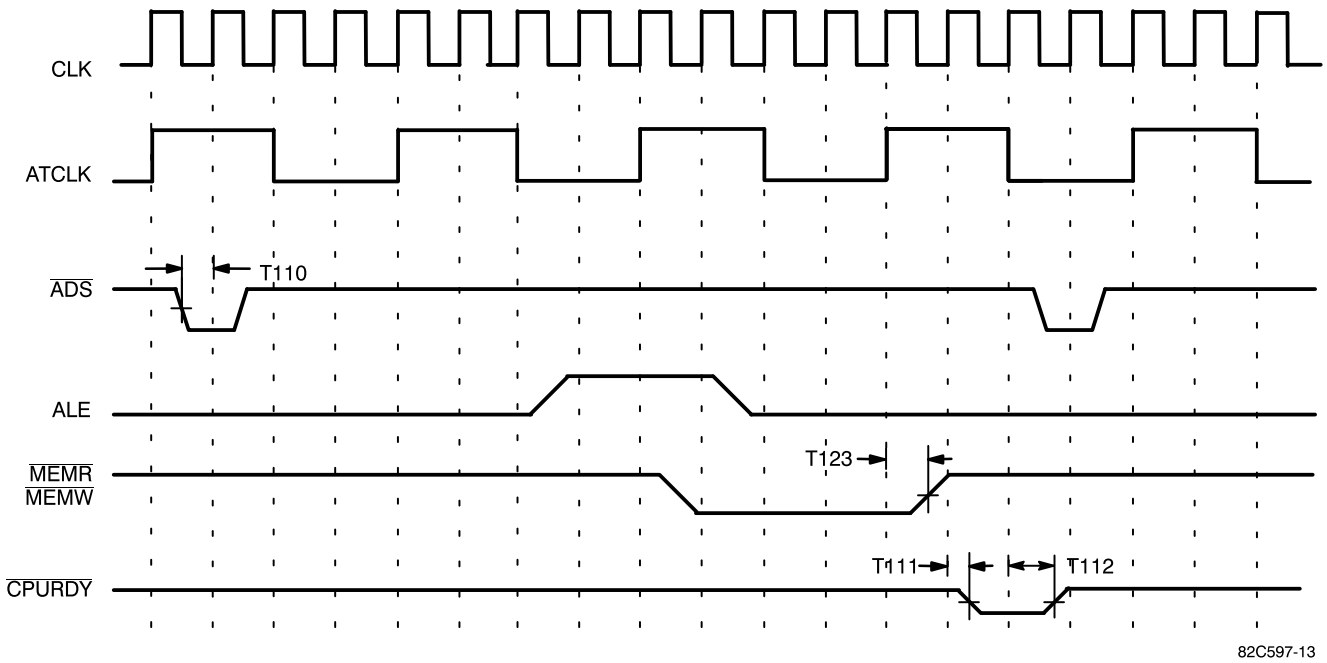
Clock Timing



Reset Timing

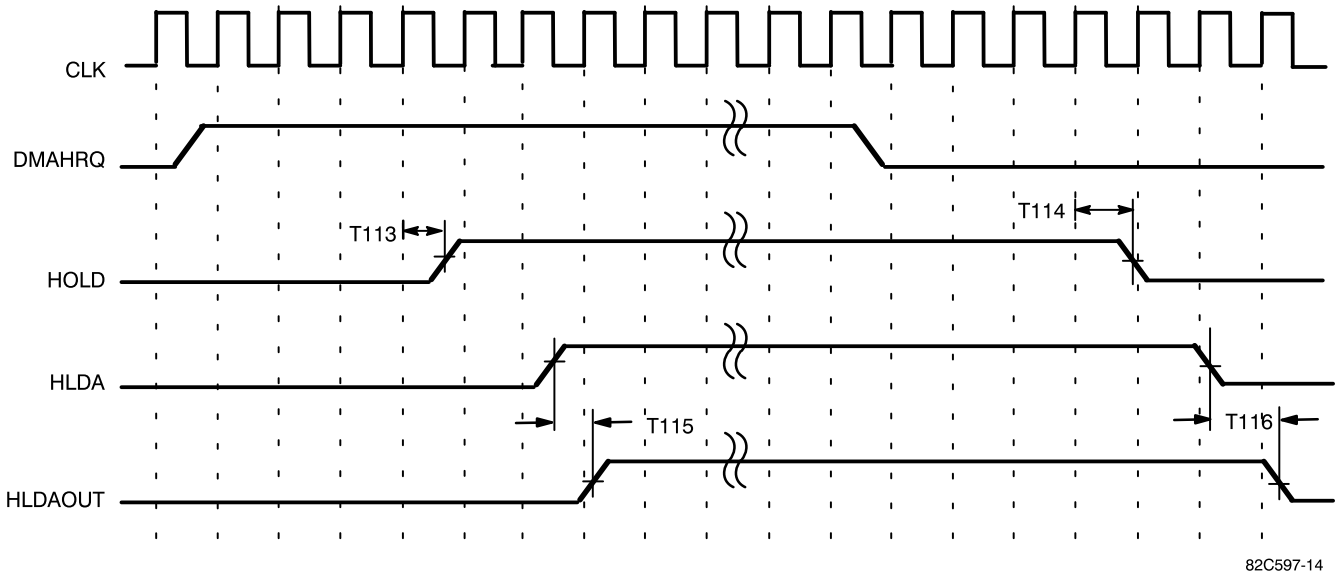


AT Cycle Timing

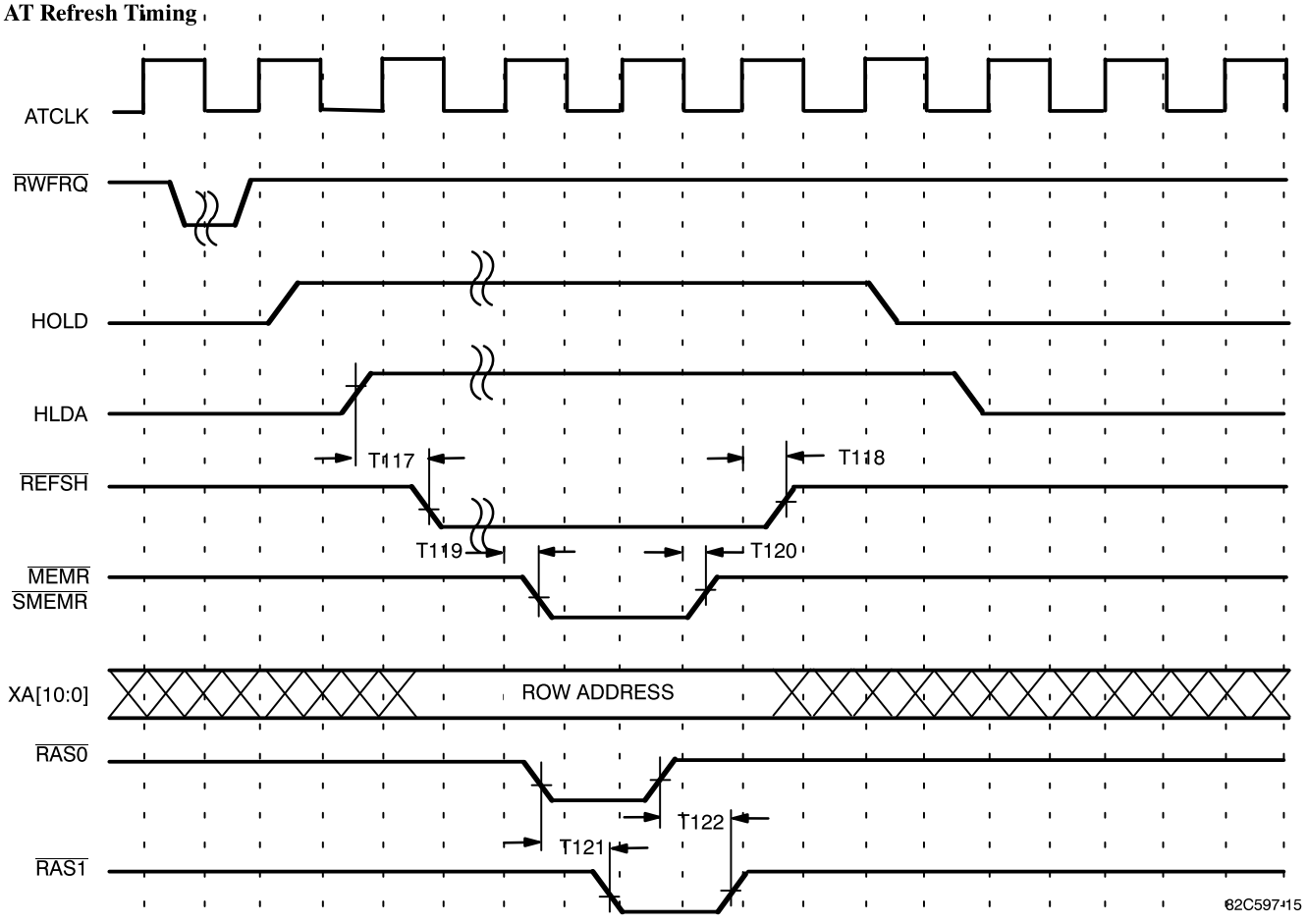


Switching Waveforms (continued)

DMA Arbitration Timing

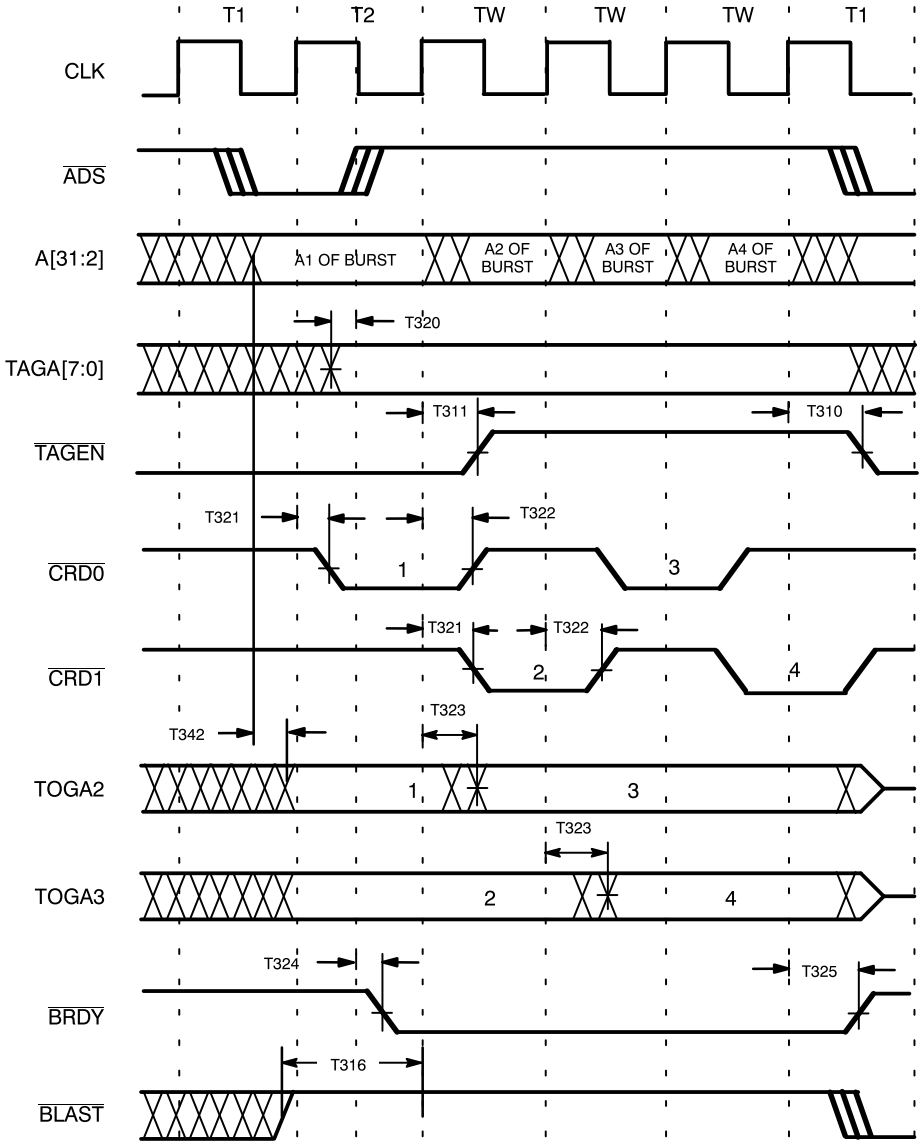


AT Refresh Timing



Switching Waveforms (continued)

486 Cache Read Hit (2-1-1-1 Burst Mode), 2 Banks of Cache, Interleaved



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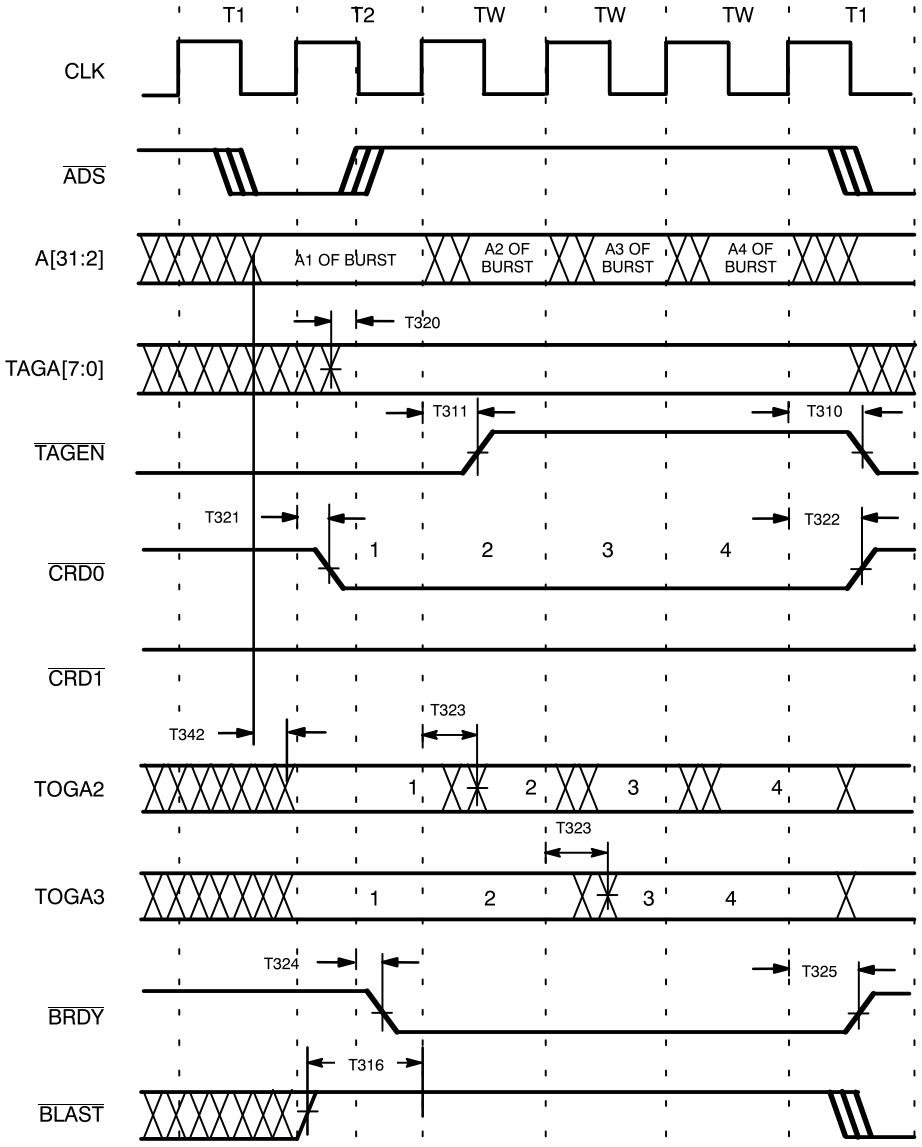
Switching Waveforms (continued)

486 Cache Read Hit (2-1-1-1 Burst Mode), 1 Bank of Cache



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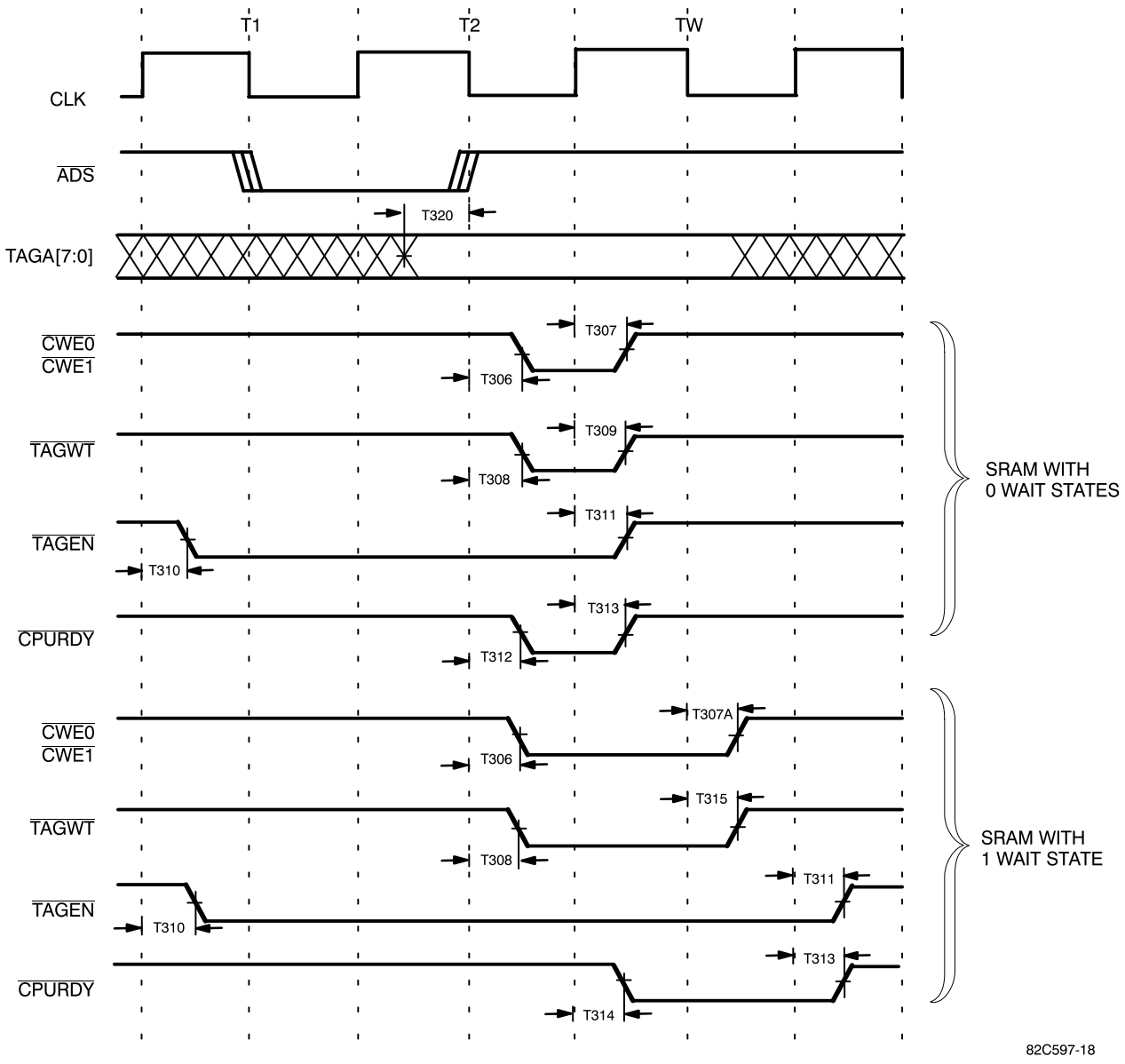
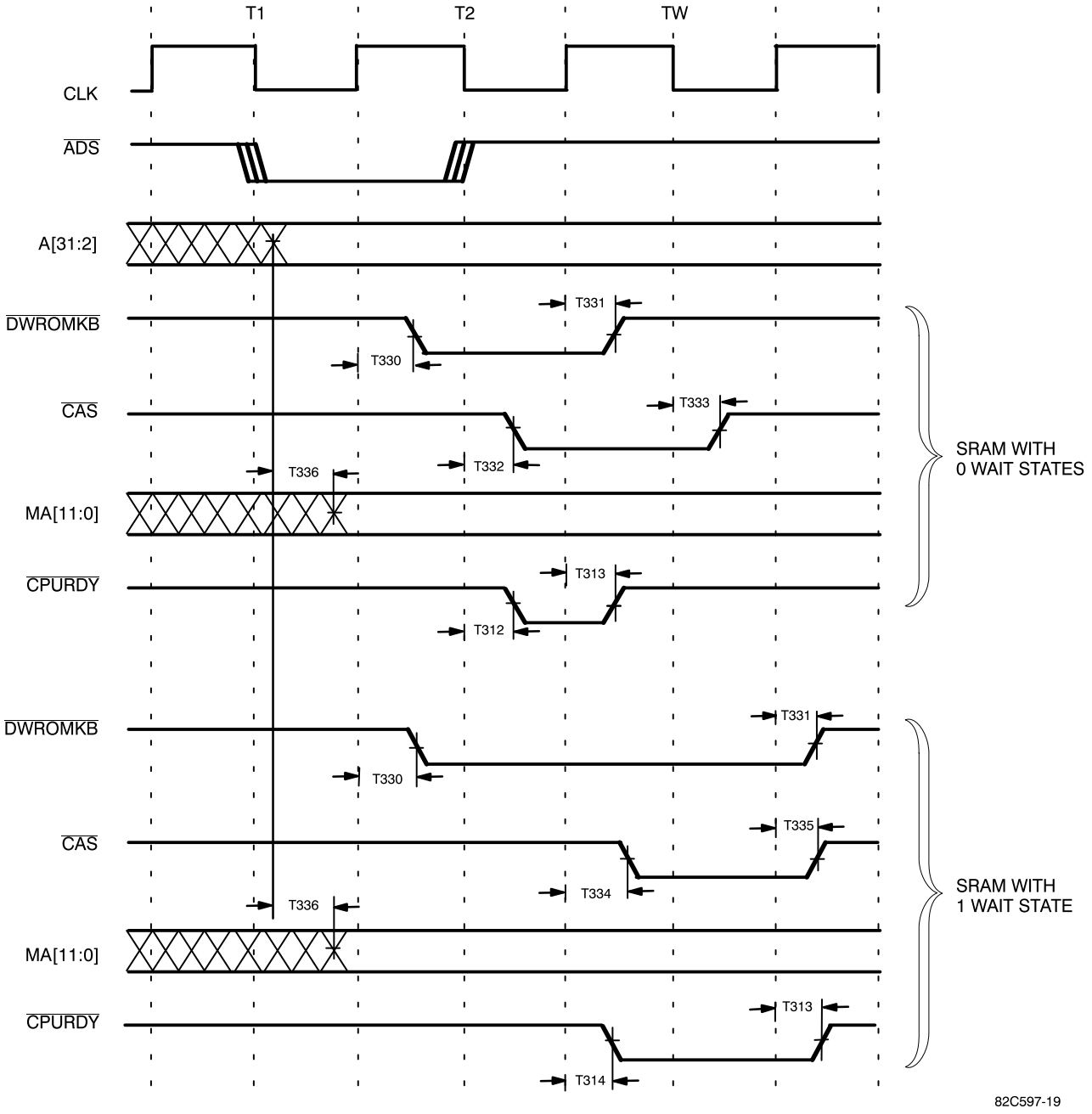
Switching Waveforms (continued)

Cache Write Hit Cycle (Write-Back)



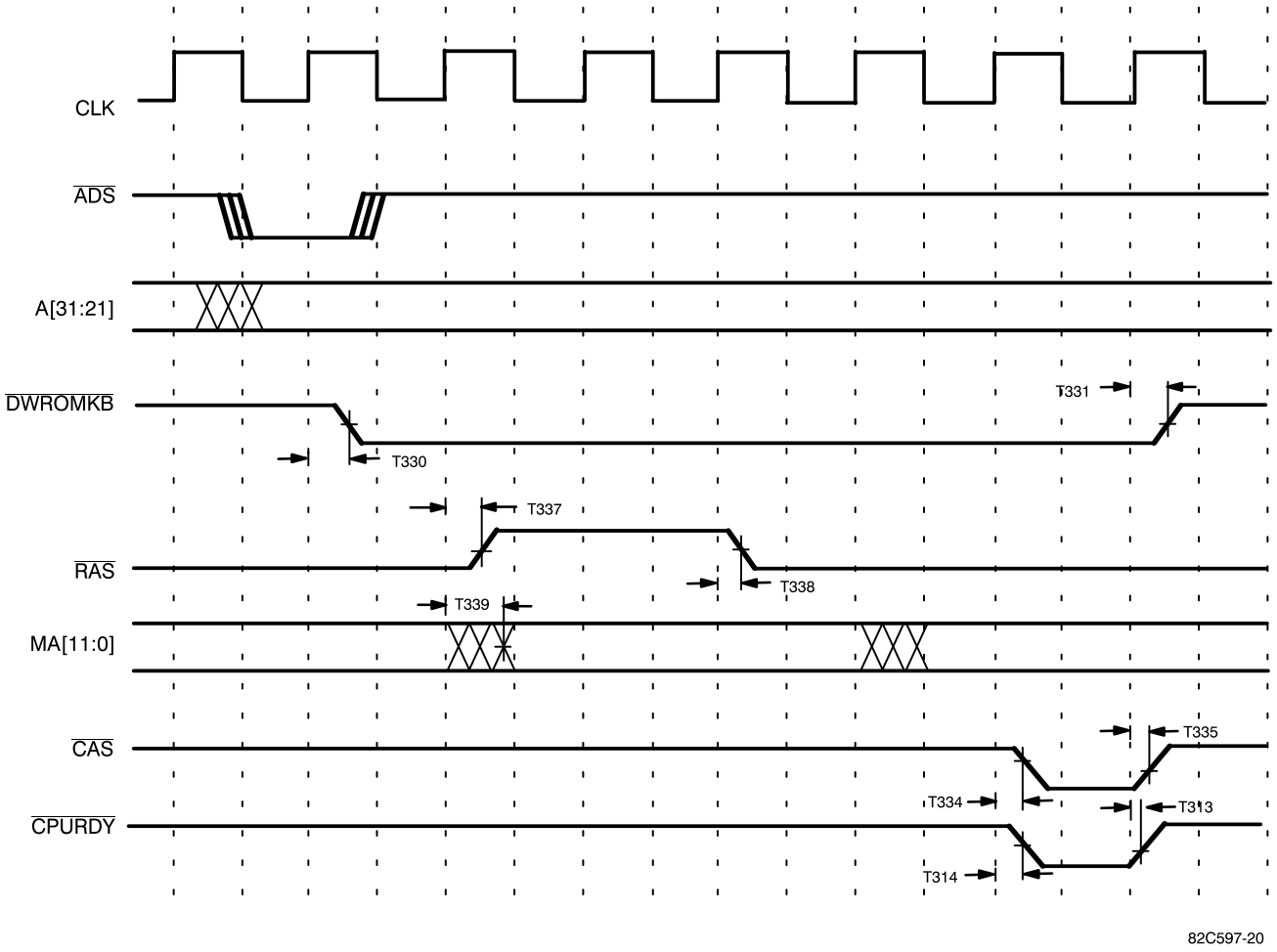
Switching Waveforms (continued)

Cache Write Miss, Page Hit Cycle



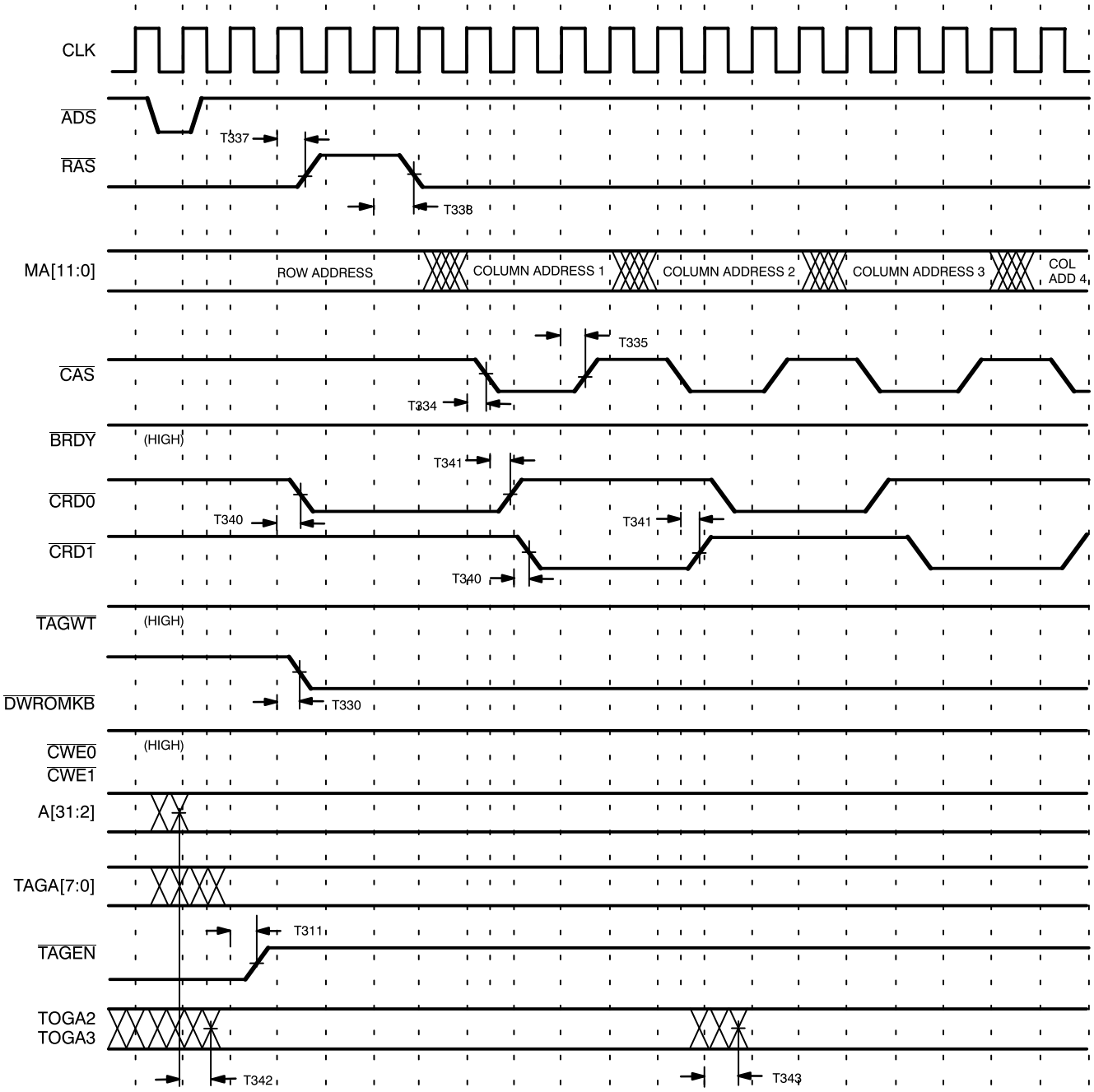
Switching Waveforms (continued)

Cache Write Miss, Page Miss Cycle



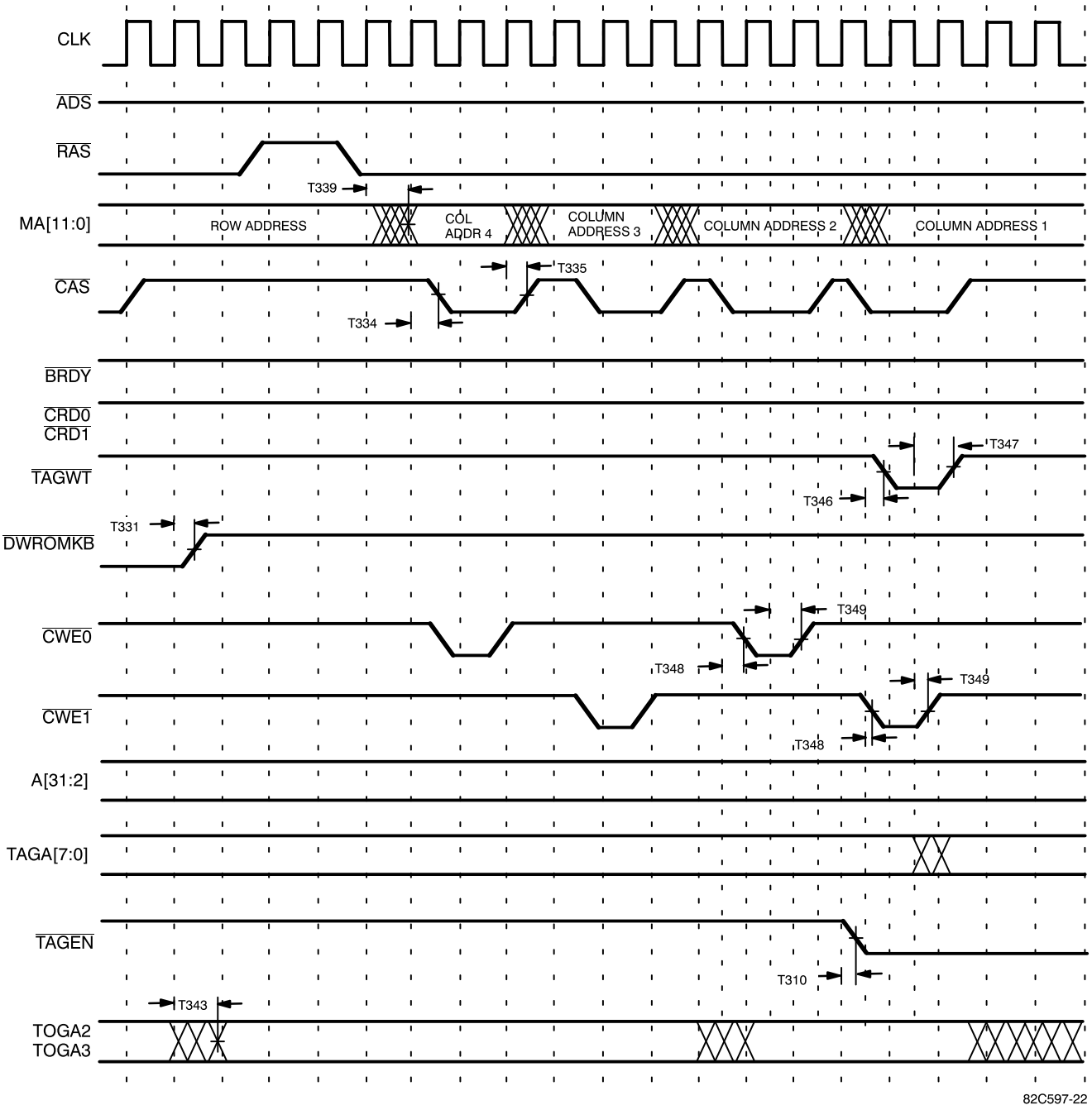
Switching Waveforms (continued)

Cache Burst Read Miss (2-1-1-1 Mode), Page Miss, Dirty = 1, DRAM R1WT Cycle (Page 1 of 3)



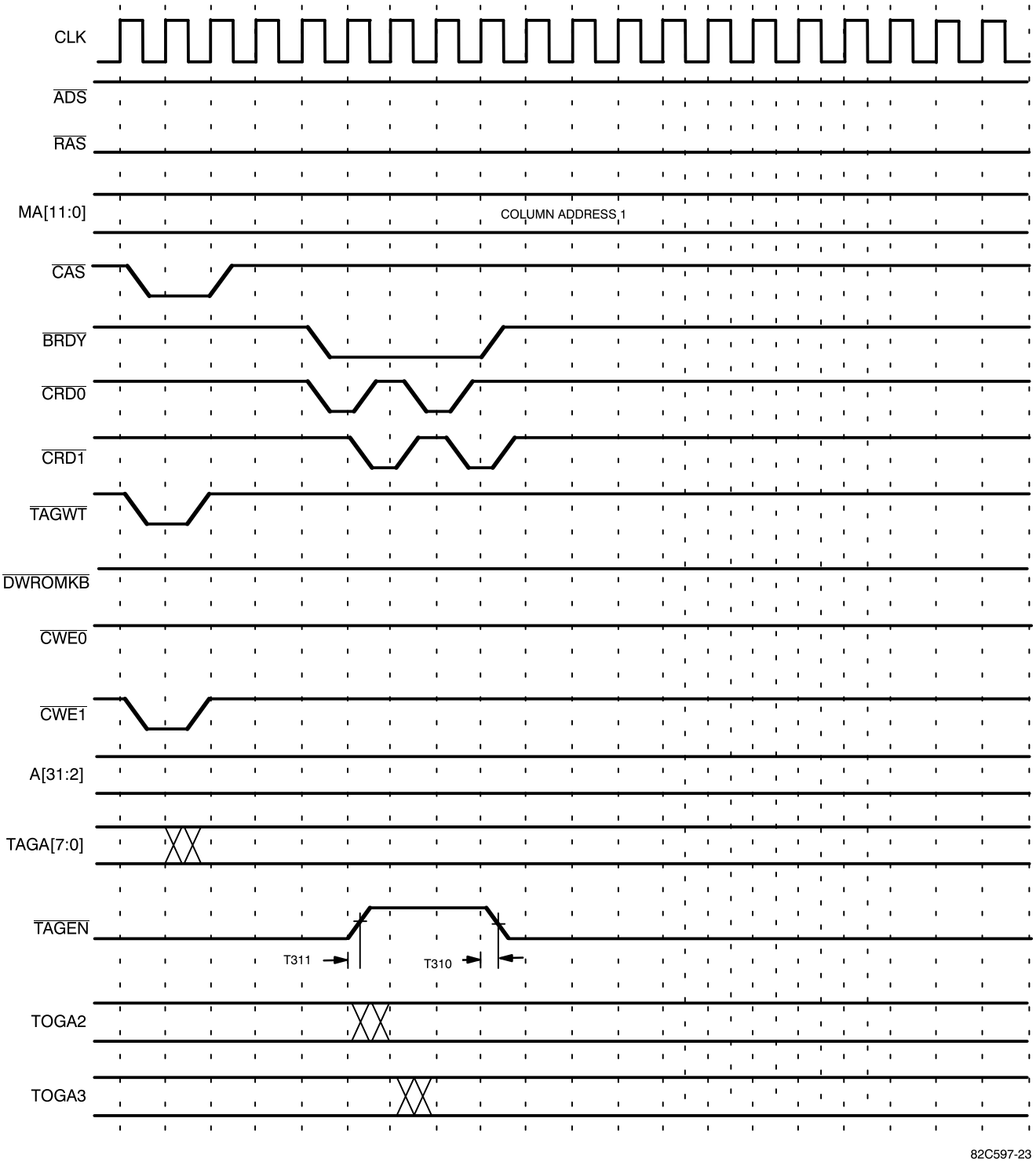
Switching Waveforms (continued)

Cache Burst Read Miss (2-1-1-1 Mode), Page Miss, Dirty = 1, DRAM R1WT Cycle (Page 2 of 3)



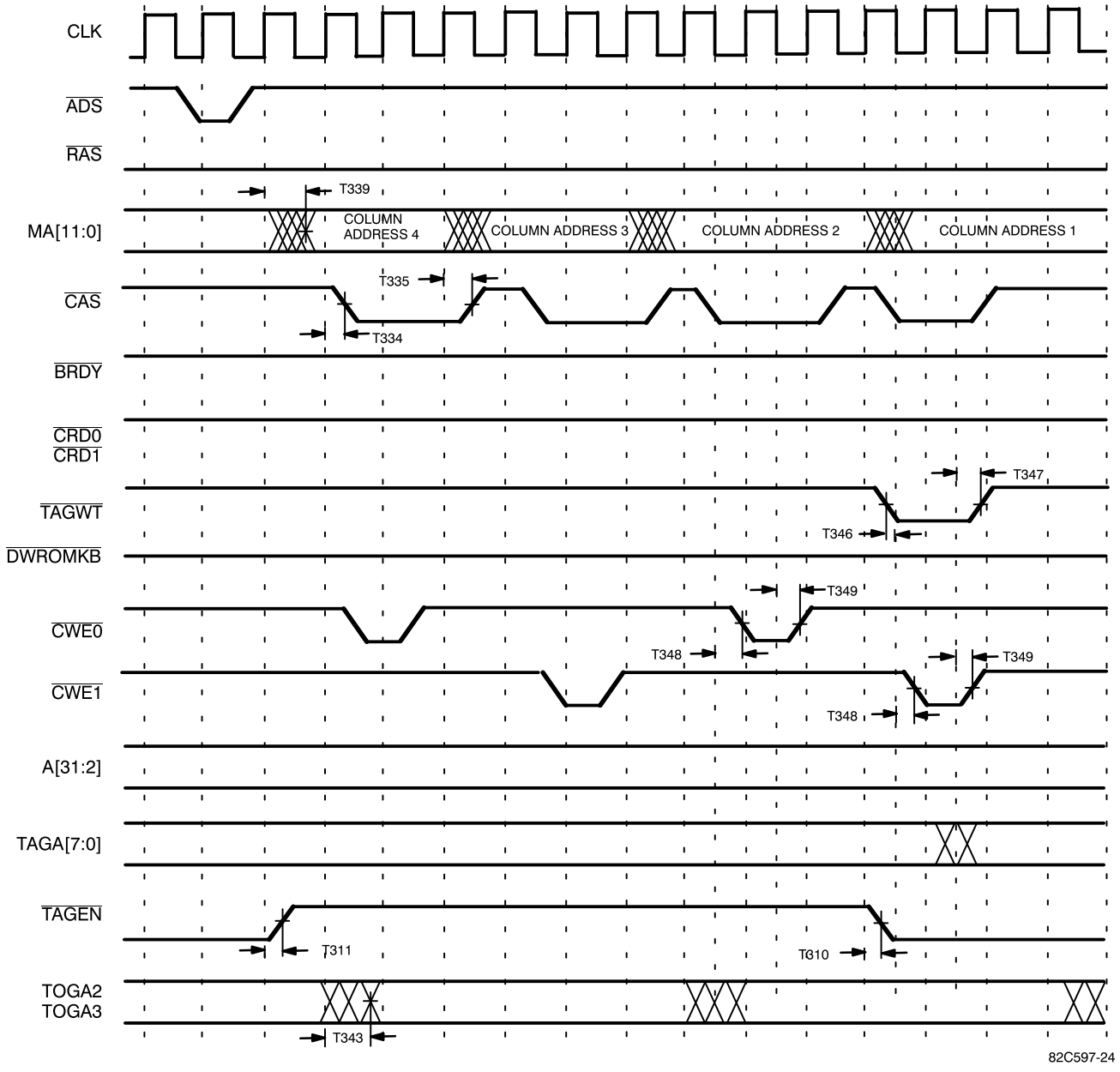
Switching Waveforms (continued)

Cache Burst Read Miss (2-1-1-1 Mode), Page Miss, Dirty = 1, DRAM R1WT Cycle (Page 3 of 3)



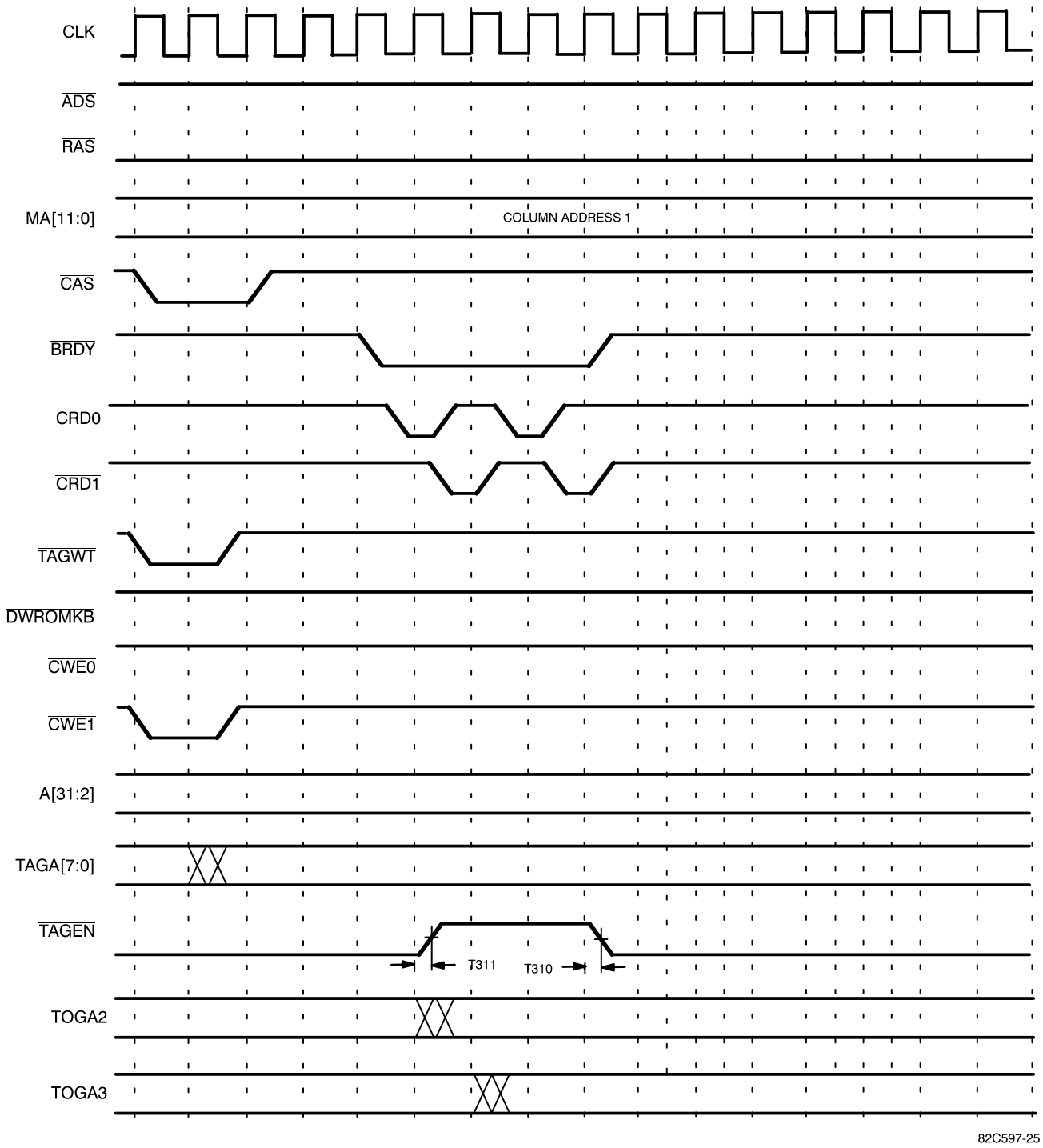
Switching Waveforms (continued)

Cache Burst Read Miss (2-1-1-1 Mode), Page Hit, Dirty = 0, DRAM R1WT Cycle (Page 1 of 2)



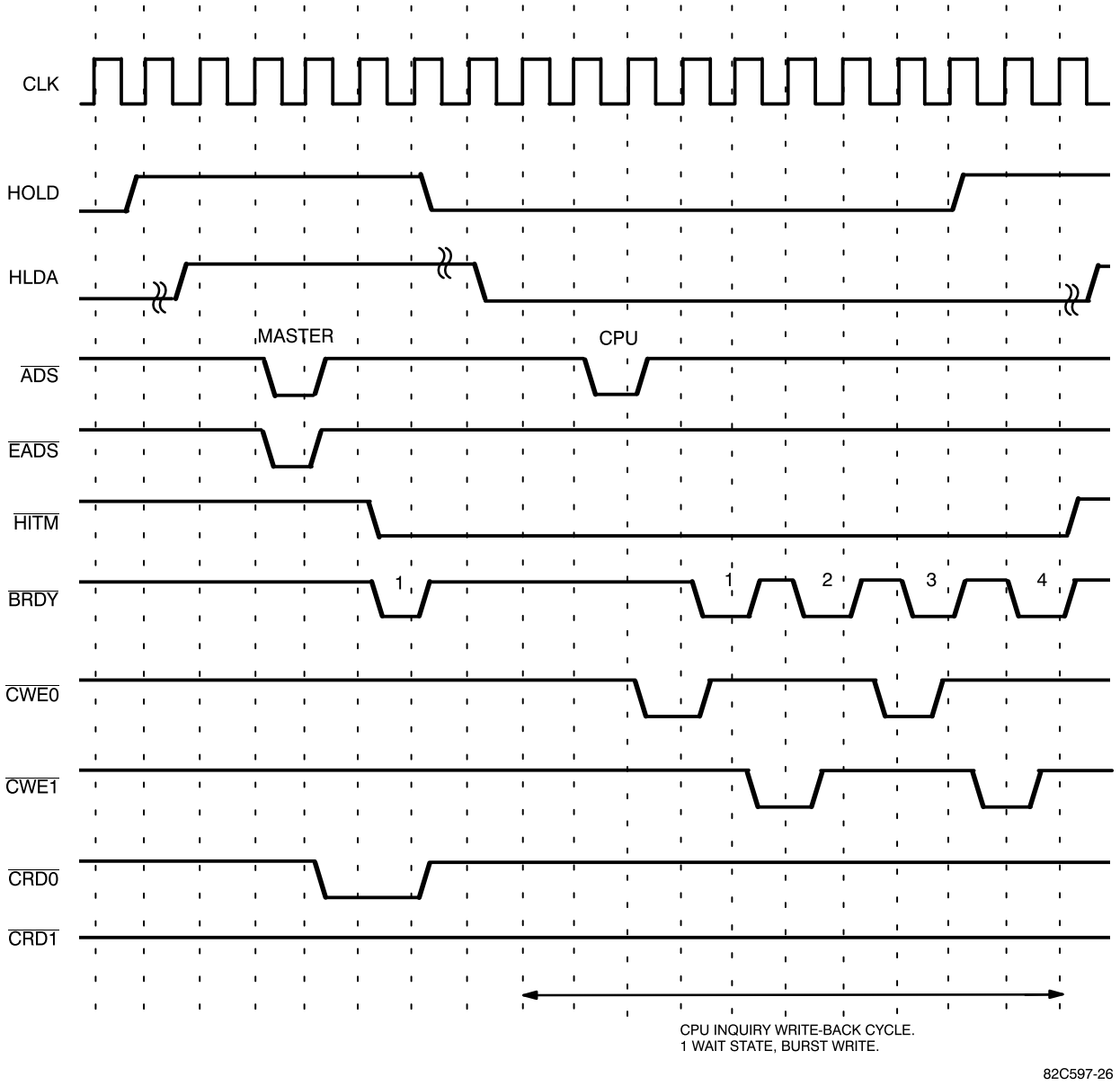
Switching Waveforms (continued)

Cache Burst Read Miss (2-1-1-1 Mode), Page Hit, Dirty = 0, DRAM R1WT Cycle (Page 2 of 2)



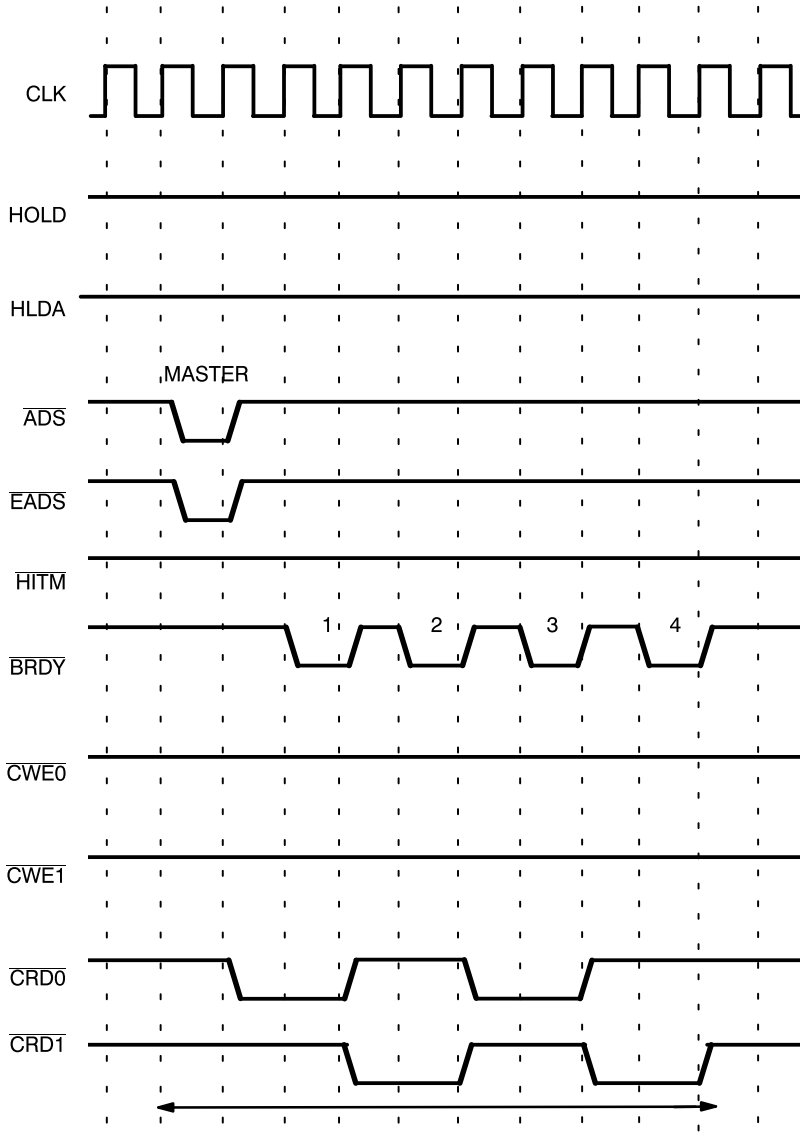
Switching Waveforms (continued)

VESA/PCI Master Read Memory Cycle with Inquiry Hit and Dirty ($\overline{HITM}$=0) (Part 1 of 2)



Switching Waveforms (continued)

VESA/PCI Master Read Memory Cycle with Inquiry Hit and Dirty ($\overline{HITM}$=0) (Part 2 of 2)



MASTER READ MEMORY CYCLE
CACHE HIT, 3222 MODE

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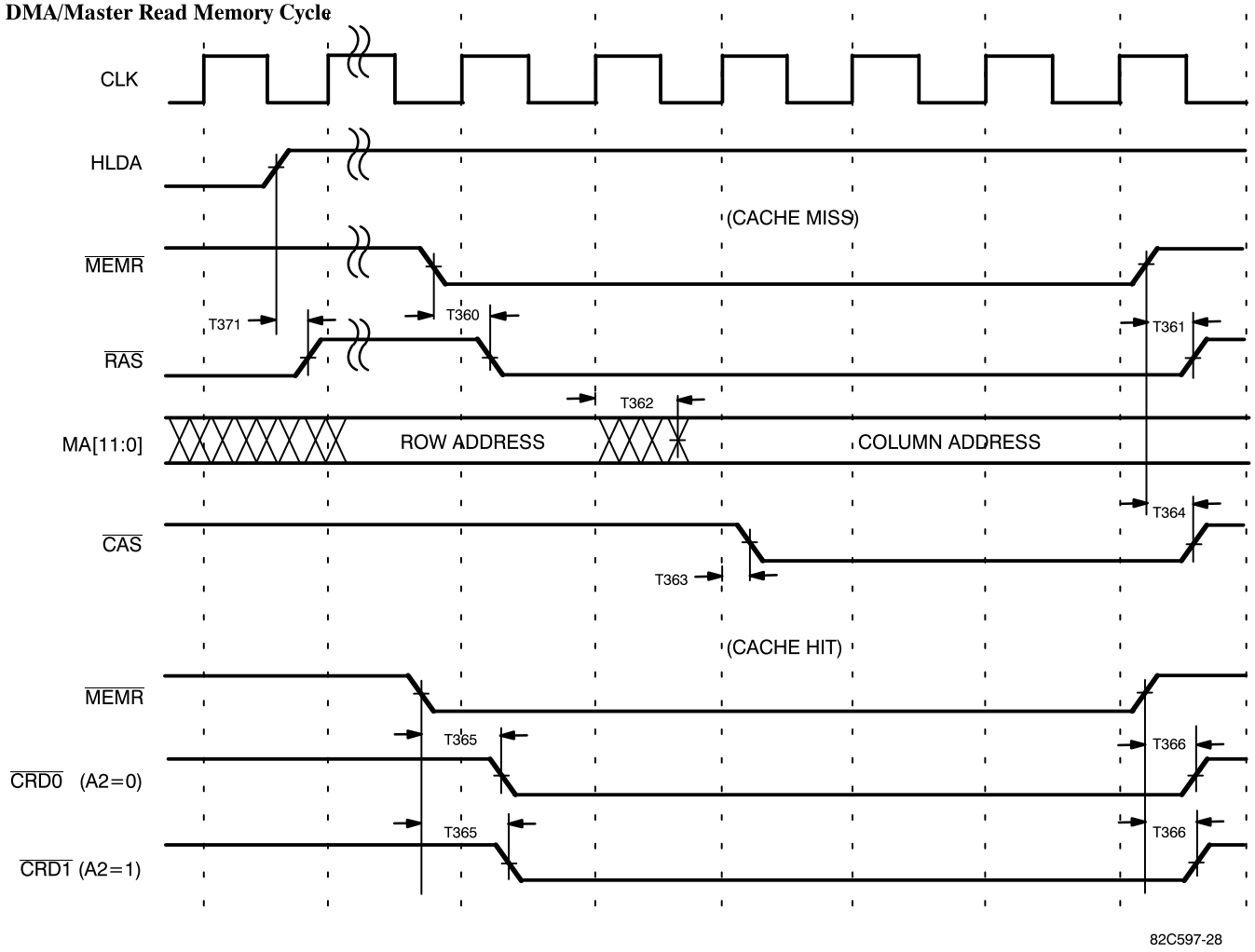
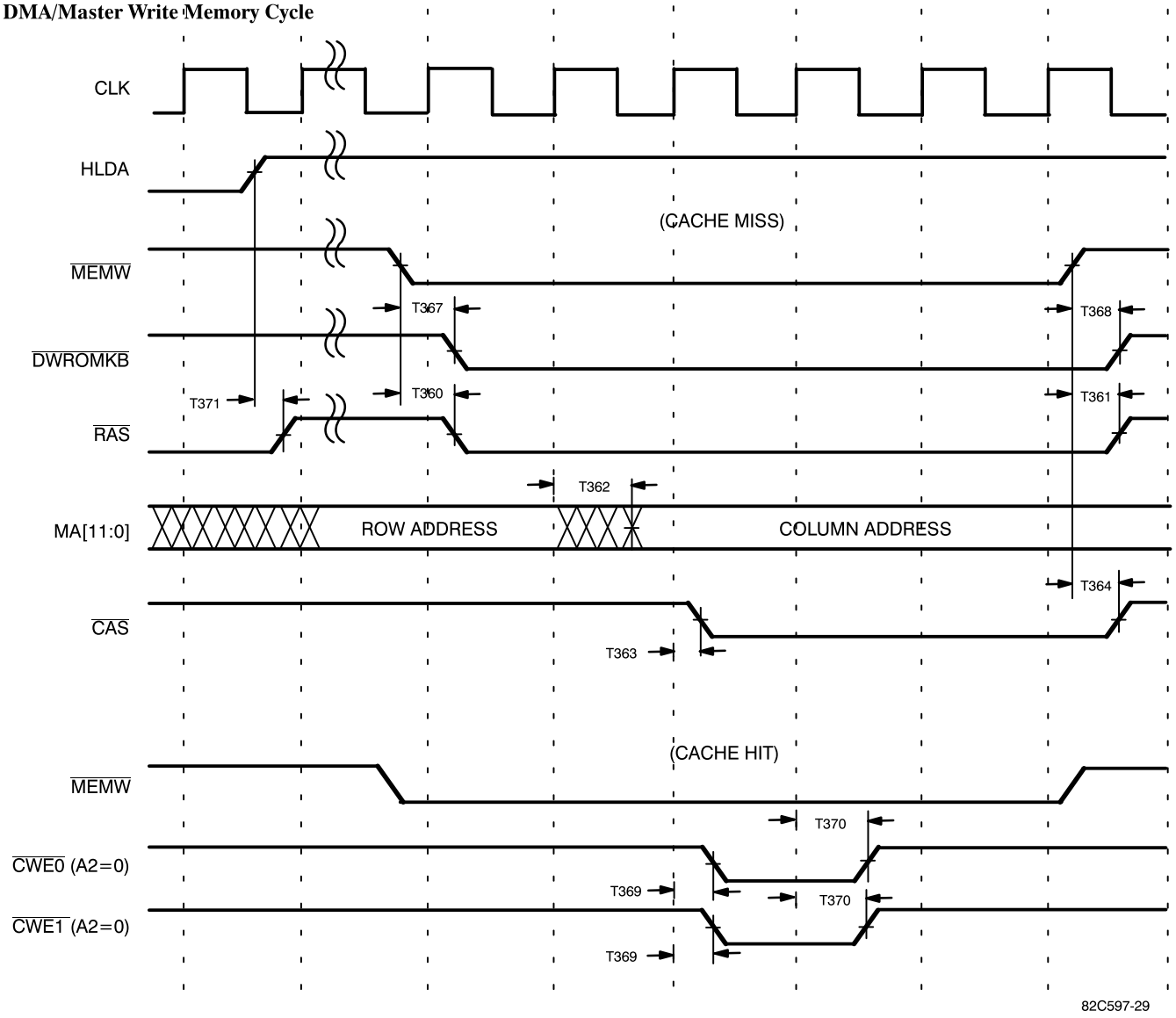
Switching Waveforms (continued)

DMA/Master Read Memory Cycle



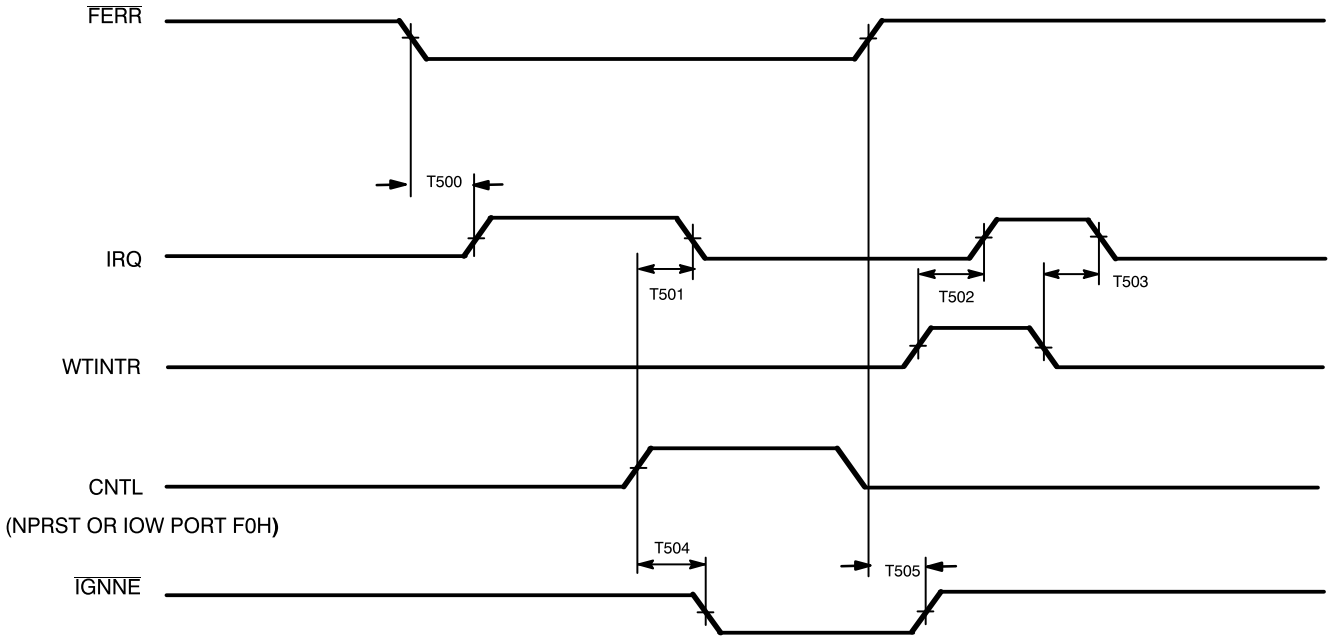
Switching Waveforms (continued)

DMA/Master Write Memory Cycle



Switching Waveforms (continued)

Numerical Coprocessor Interface Timing



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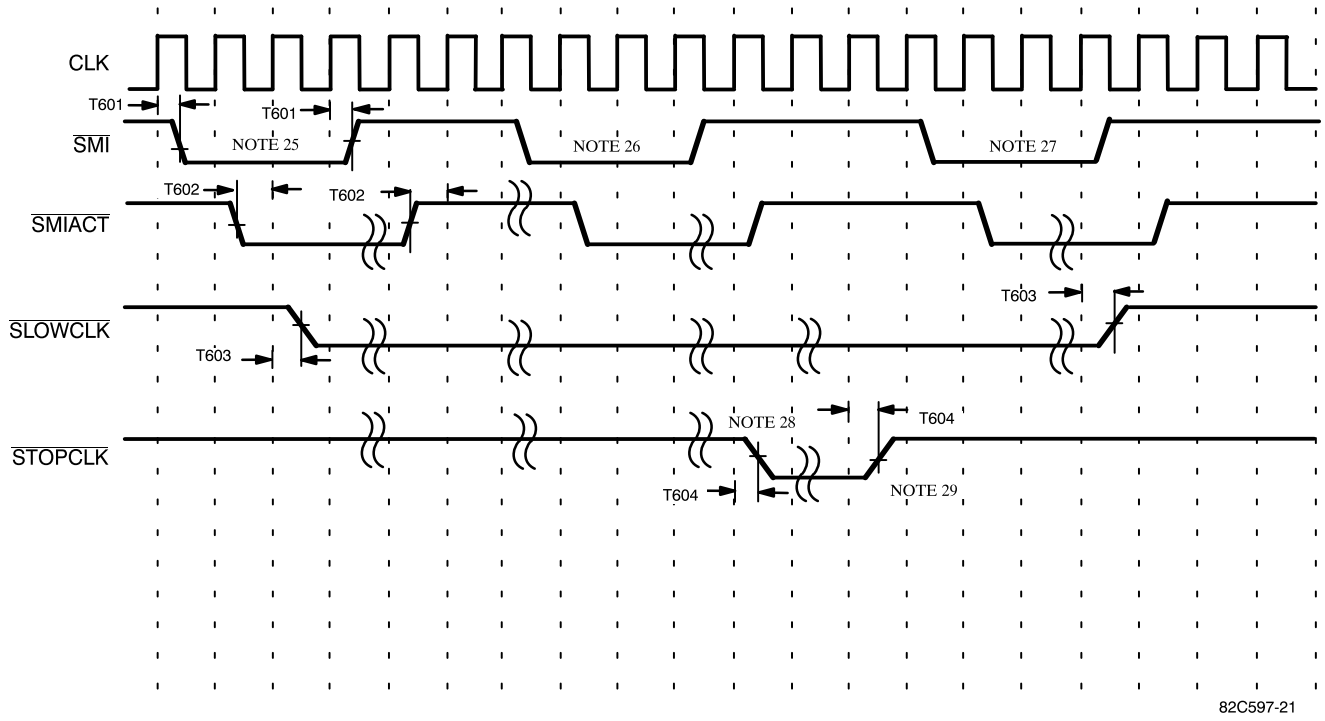
Switching Waveforms (continued)

Software Power-Down (Through $\overline{\text{SMI}}$)

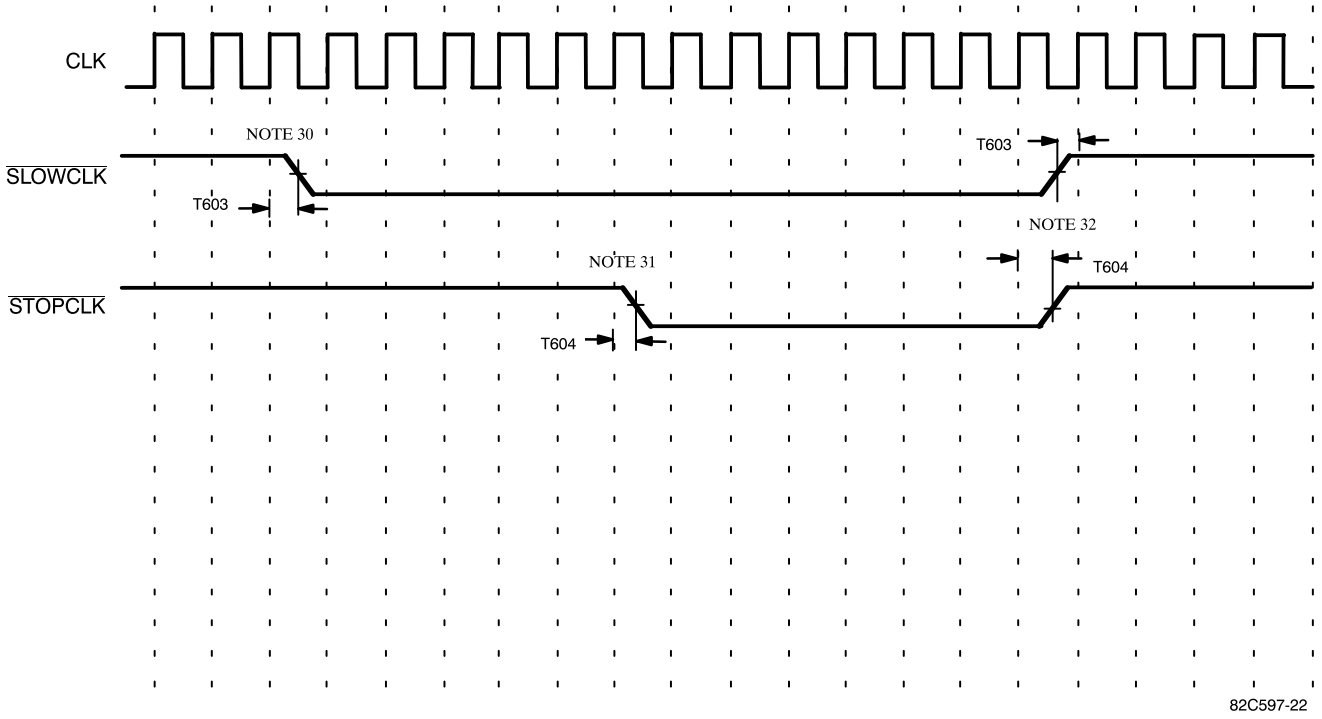


Notes:

25. $\overline{\text{SMI}}$ (System Management Interrupt) assertion caused by the stand-by timer reaching its terminal count with no detected events.
26. $\overline{\text{SMI}}$ (System Management Interrupt) assertion caused by the suspend timer reaching its terminal count with no detected events.
27. $\overline{\text{SMI}}$ (System Management Interrupt) assertion caused by the detection of one of the monitored events.
28. $\overline{\text{STOPCLK}}$ will go active when Register 64 bit 6 is set to 1 and the STOPCLK timer has expired.
29. $\overline{\text{STOPCLK}}$ will be deasserted when a monitored event is detected.

Switching Waveforms (continued)

Hardware Power-Down



Notes:

30. The assertion of $\overline{\text{SLOWCLK}}$ caused by the stand-by timer reaching its terminal count with no detected events.
31. The assertion of $\overline{\text{STOPCLK}}$ caused by the suspend timer reaching its terminal count with no detected events.
32. $\overline{\text{SLOWCLK}}$ and $\overline{\text{STOPCLK}}$ deassertion caused by the detection of one of the monitored events.

Package Diagrams

160-Lead Plastic Quad Flatpack N160