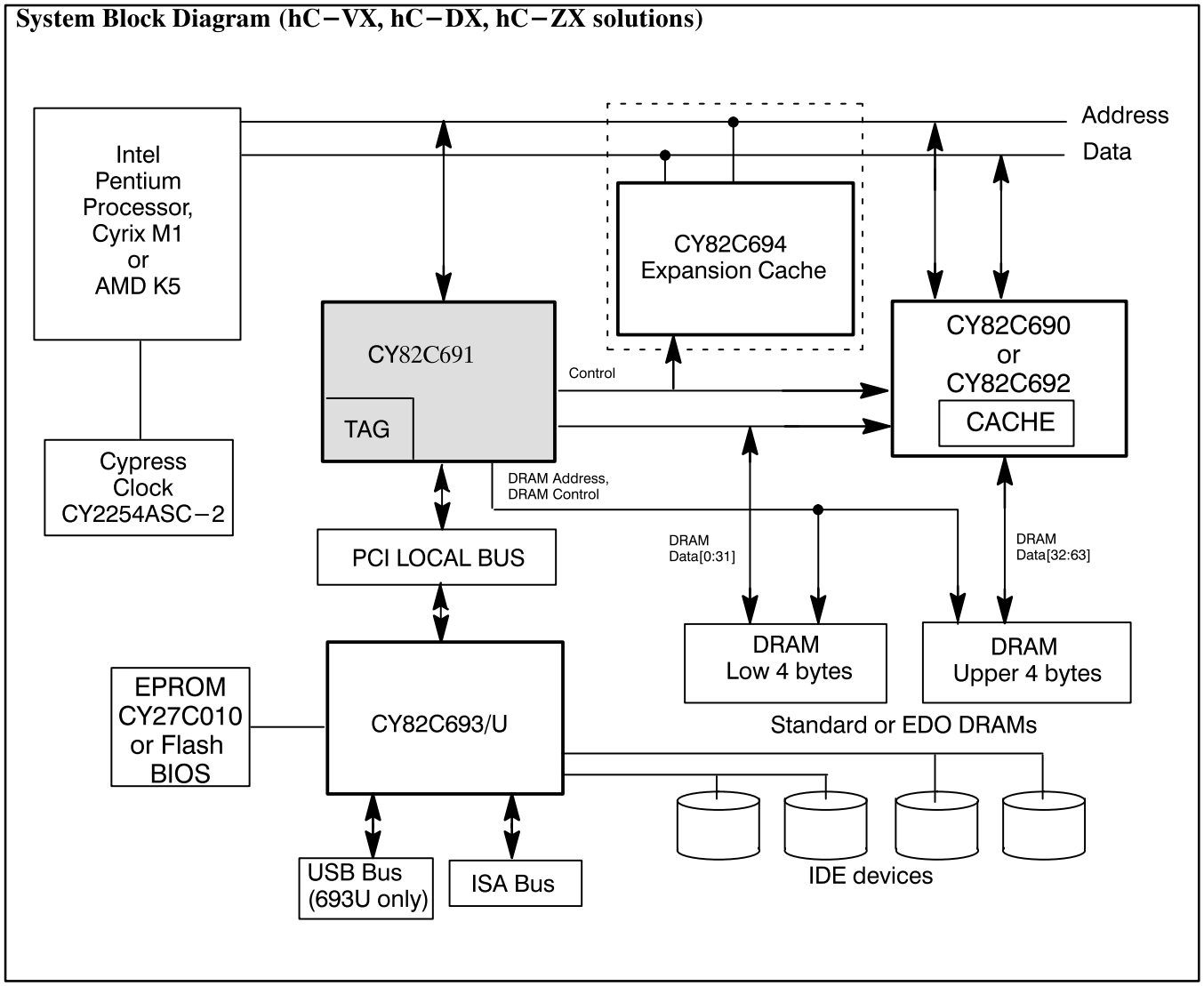
PRELIMINARY **CY82C691**

Pentium™ hyperCache™ Chipset System Controller

Features

- Provides control for the cache, system memory, and the PCI bus
- PCI Bus Rev. 2.1 compliant
- Supports 3V Pentium™, AMD K5, and Cyrix 6x86 (M1) CPUs
- Support for WB or WT L1 cache
- Supports 3-1-1-1 burst read/write operation at 66, 60, and 50 MHz bus speeds
- Supports CPU address pipelining
- Support for synchronous flow-through or pipelined BSRAMs
- Provides power management support through SMM (APM Compliant)
- Integrated 8Kx21 tag (direct mapped or two-way set associative)
- Support for cache sizes up to 1 MB
- Supports mixed standard page-mode and EDO DRAMs
- Supports the VESA Unified Memory Architecture (VUMA)
- Support for standard 72-bit-wide DRAM banks
- Supports non-symmetrical DRAM banks
- Supports six banks of DRAM (six RAS lines)
- Supports DRAM densities up to 16 Mb
- Up to 768 MB main memory
- variable drive on DRAM address and control lines (max 20mA)
- Provides glueless (0 TTL) system solution
- Support for concurrent operation among CPU, cache, DRAM, and PCI
- Byte-Merge operation
- 8 deep PCI post-write / pre-read buffers
- Packaged in a 208-pin PQFP

System Block Diagram (hC−VX, hC−DX, hC−ZX solutions)



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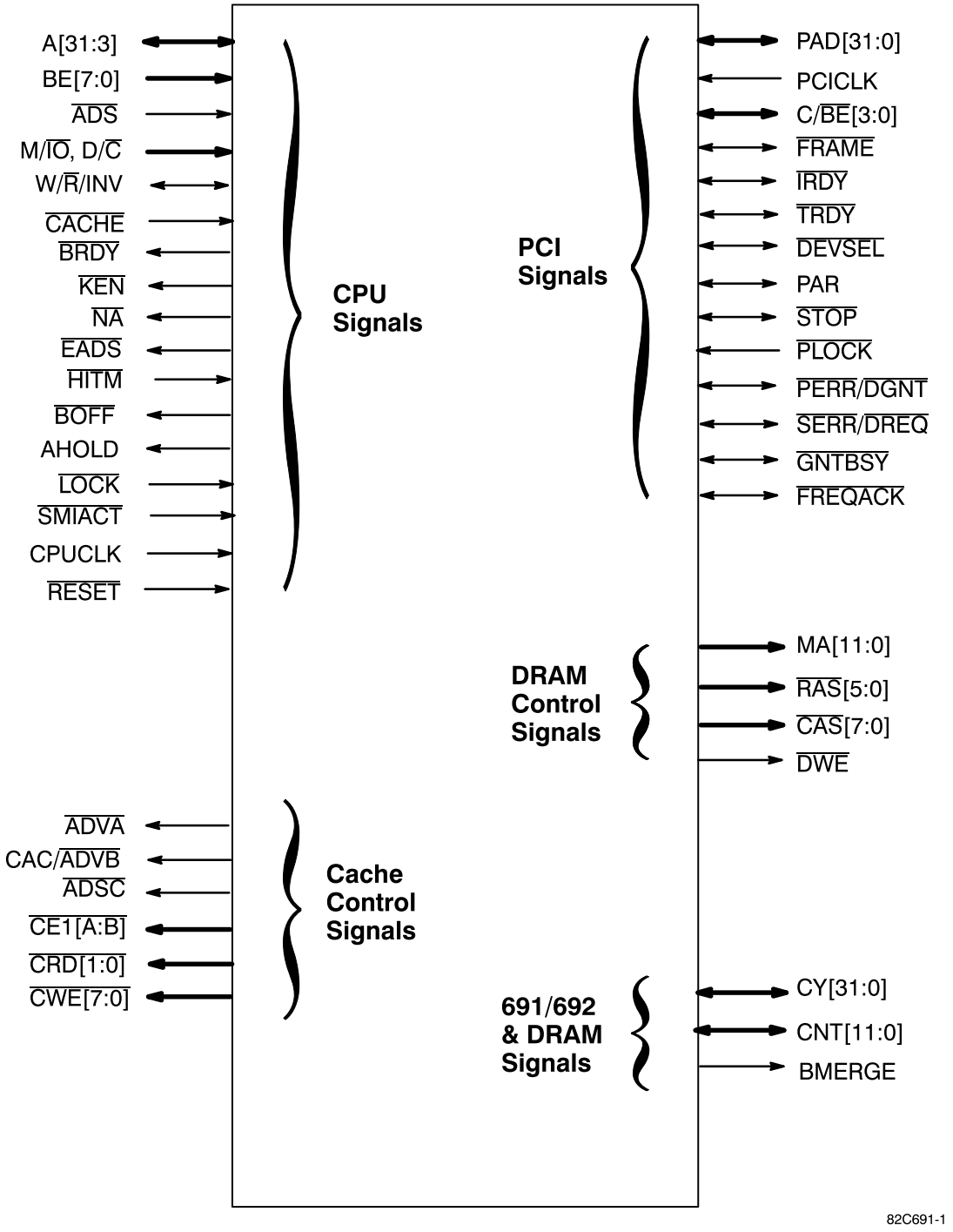
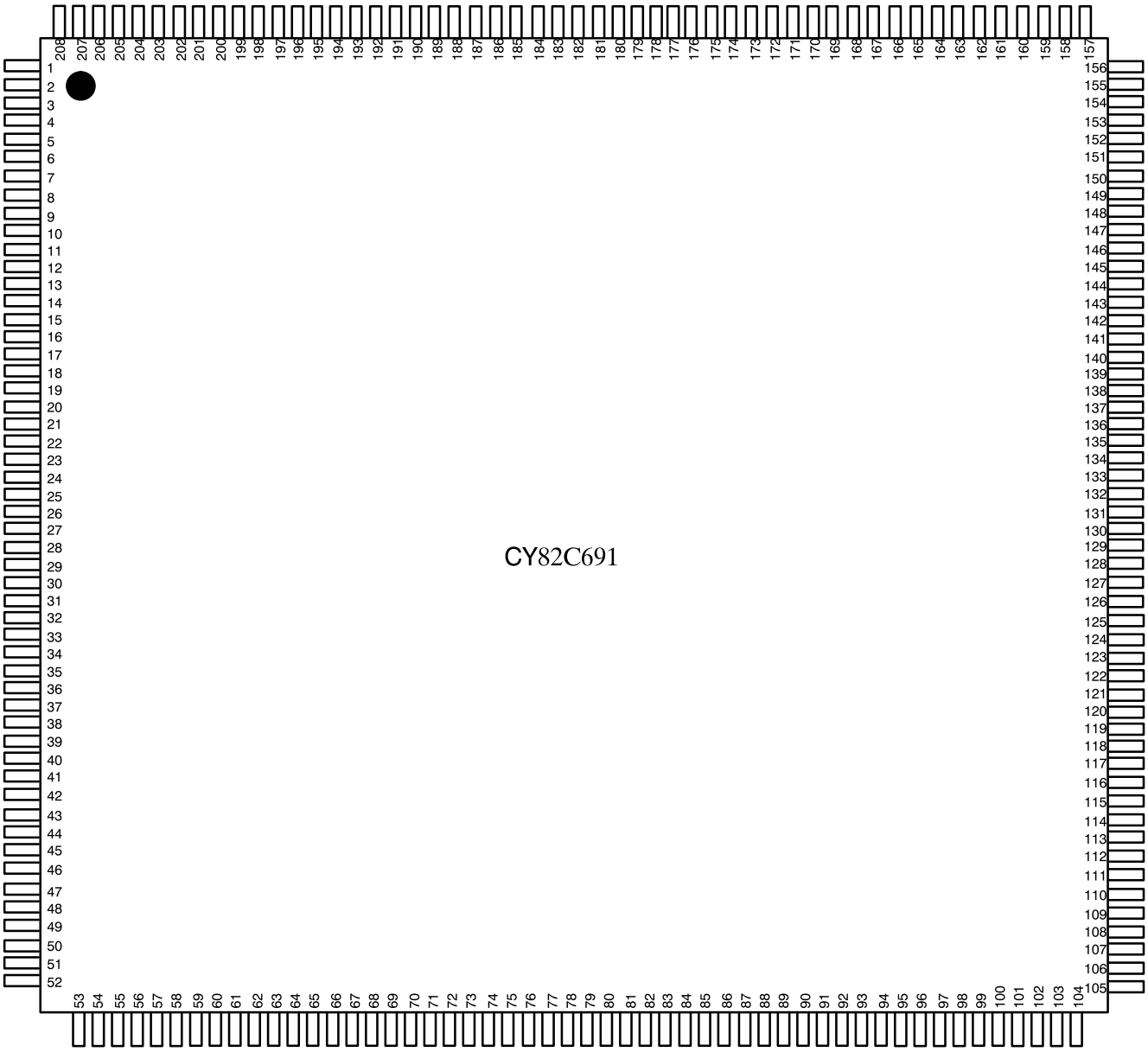
CY82C691 Signals



Pin Configuration

208-pin PQFP
Top View



82C691-2

CY82C691 Pin Reference (In Numerical Order by Pin Number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	CY13	43	A23	85	SERR/DREQ
2	CY12	44	A24	86	GNTBSY
3	CY11	45	A25	87	FREQACK
4	CY10	46	A26	88	STOP
5	CY9	47	A27	89	PAR
6	CY8	48	A28	90	DEVSEL
7	CY7	49	A29	91	+5V
8	CY6	50	A30	92	TRDY
9	CY5	51	A31	93	GND
10	CY4	52	MA11	94	IRDY
11	CY3	53	MA10	95	FRAME
12	CY2	54	MA9	96	PC/BE3
13	CY1	55	MA8	97	PC/BE2
14	CY0	56	MA7	98	PC/BE1
15	GND	57	MA6	99	PC/BE0
16	A3	58	MA5	100	PAD31
17	A4	59	MA4	101	PAD30
18	A5	60	MA3	102	PAD29
19	A6	61	MA2	103	PAD28
20	+5V	62	MA1	104	PAD27
21	GND	63	MA0	105	GND
22	A7	64	RAS5	106	PAD26
23	LOCK	65	+5V	107	PAD25
24	A8	66	RAS4	108	PAD24
25	HITM	67	GND	109	PAD23
26	A9	68	RAS3	110	PAD22
27	A10	69	RAS2	111	PAD21
28	A11	70	RAS1	112	PAD20
29	A12	71	RAS0	113	PAD19
30	A13	72	DWE	114	PAD18
31	A14	73	CAS7	115	PAD17
32	+3.3V	74	CAS6	116	PAD16
33	GND	75	CAS5	117	PAD15
34	A15	76	+5V	118	PAD14
35	A16	77	CAS4	119	PAD13
36	A17	78	CAS3	120	PAD12
37	A18	79	CAS2	121	PAD11
38	A19	80	CAS1	122	PAD10
39	A20	81	GND	123	PAD9
40	A21	82	CAS0	124	+5V
41	A22	83	BMERGE	125	GND
42	CACHE	84	PLOCK	126	PAD8

CY82C691 Pin Reference (In Numerical Order by Pin Number) (continued)

Pin No.	Pin Name		Pin No.	Pin Name
127	PAD7		169	+3.3V
128	PAD6		170	$\overline{\text{CWE5}}$
129	PAD5		171	$\overline{\text{CWE4}}$
130	PAD4		172	$\overline{\text{CWE3}}$
131	PAD3		173	$\overline{\text{CWE2}}$
132	PAD2		174	$\overline{\text{CWE1}}$
133	PAD1		175	$\overline{\text{CWE0}}$
134	PAD0		176	$\overline{\text{RESET}}$
135	PCICLK		177	CNT11
136	+5V		178	CNT10
137	GND		179	CNT9
138	CPUCLK		180	CNT8
139	$\overline{\text{PERR}}$/$\overline{\text{DGNT}}$		181	CNT7
140	$\overline{\text{ADSC}}$		182	CNT6
141	$\overline{\text{BRDY}}$		183	CNT5
142	$\overline{\text{ADVB}}$/CAC		184	CNT4
143	$\overline{\text{ADVA}}$		185	CNT3
144	D/$\overline{\text{C}}$		186	CNT2
145	M/$\overline{\text{IO}}$		187	CNT1
146	$\overline{\text{ADS}}$		188	CNT0
147	BE7		189	CY31
148	BE6		190	CY30
149	BE5		191	CY29
150	BE4		192	CY28
151	GND		193	CY27
152	BE3		194	CY26
153	BE2		195	CY25
154	BE1		196	CY24
155	BE0		197	GND
156	AHOLD		198	CY23
157	$\overline{\text{BOFF}}$		199	CY22
158	$\overline{\text{EADS}}$		200	CY21
159	$\overline{\text{NA}}$		201	CY20
160	$\overline{\text{KEN}}$		202	CY19
161	W/$\overline{\text{R}}$/INV		203	CY18
162	$\overline{\text{SMIACT}}$		204	CY17
163	$\overline{\text{CE1B}}$		205	CY16
164	$\overline{\text{CE1A}}$		206	CY15
165	$\overline{\text{CRD1}}$		207	CY14
166	$\overline{\text{CRD0}}$		208	+3.3V
167	$\overline{\text{CWE7}}$			
168	$\overline{\text{CWE6}}$			

CY82C691 Pin Reference (In Alphabetical Order by Signal Name)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A3	16	BE6	148	CY1	13
A4	17	BE7	147	CY2	12
A5	18	BMERGE	83	CY3	11
A6	19	$\overline{\text{BOFF}}$	157	CY4	10
A7	22	$\overline{\text{BRDY}}$	141	CY5	9
A8	24	$\overline{\text{CACHE}}$	42	CY6	8
A9	26	$\overline{\text{CAS0}}$	82	CY7	7
A10	27	$\overline{\text{CAS1}}$	80	CY8	6
A11	28	$\overline{\text{CAS2}}$	79	CY9	5
A12	29	$\overline{\text{CAS3}}$	78	CY10	4
A13	30	$\overline{\text{CAS4}}$	77	CY11	3
A14	31	$\overline{\text{CAS5}}$	75	CY12	2
A15	34	$\overline{\text{CAS6}}$	74	CY13	1
A16	35	$\overline{\text{CAS7}}$	73	CY14	207
A17	36	$\overline{\text{CE1A}}$	164	CY15	206
A18	37	$\overline{\text{CE1B}}$	163	CY16	205
A19	38	CNT0	188	CY17	204
A20	39	CNT1	187	CY18	203
A21	40	CNT2	186	CY19	202
A22	41	CNT3	185	CY20	201
A23	43	CNT4	184	CY21	200
A24	44	CNT5	183	CY22	199
A25	45	CNT6	182	CY23	198
A26	46	CNT7	181	CY24	196
A27	47	CNT8	180	CY25	195
A28	48	CNT9	179	CY26	194
A29	49	CNT10	178	CY27	193
A30	50	CNT11	177	CY28	192
A31	51	CPUCLK	138	CY29	191
$\overline{\text{ADS}}$	146	$\overline{\text{CRD0}}$	166	CY30	190
$\overline{\text{ADSC}}$	140	$\overline{\text{CRD1}}$	165	CY31	189
$\overline{\text{ADVA}}$	143	$\overline{\text{CWE0}}$	175	D/$\overline{\text{C}}$	144
$\overline{\text{ADVB}}$/CAC	142	$\overline{\text{CWE1}}$	174	$\overline{\text{DEVSEL}}$	90
AHOLD	156	$\overline{\text{CWE2}}$	173	$\overline{\text{DWE}}$	72
BE0	155	$\overline{\text{CWE3}}$	172	$\overline{\text{EADS}}$	158
BE1	154	$\overline{\text{CWE4}}$	171	$\overline{\text{FRAME}}$	95
BE2	153	$\overline{\text{CWE5}}$	170	$\overline{\text{FREQACK}}$	87
BE3	152	$\overline{\text{CWE6}}$	168	GND	15,21,33,67,81,93, 105,125,137,151,197
BE4	150	$\overline{\text{CWE7}}$	167	$\overline{\text{GNTBSY}}$	86
BE5	149	CY0	14	$\overline{\text{HITM}}$	25

CY82C691 Pin Reference (In Alphabetical Order by Signal Name) (continued)

Pin Name	Pin No.	Pin Name	Pin No.
$\overline{\text{IRDY}}$	94	PAD22	110
$\overline{\text{KEN}}$	160	PAD23	109
$\overline{\text{LOCK}}$	23	PAD24	108
MA0	63	PAD25	107
MA1	62	PAD26	106
MA2	61	PAD27	104
MA3	60	PAD28	103
MA4	59	PAD29	102
MA5	58	PAD30	101
MA6	57	PAD31	100
MA7	56	PAR	89
MA8	55	PC/$\overline{\text{BE0}}$	99
MA9	54	PC/$\overline{\text{BE1}}$	98
MA10	53	PC/$\overline{\text{BE2}}$	97
MA11	52	PC/$\overline{\text{BE3}}$	96
M/$\overline{\text{IO}}$	145	PCICLK	135
$\overline{\text{NA}}$	159	$\overline{\text{PERR}}$/DGNT	139
PAD0	134	$\overline{\text{PLOCK}}$	84
PAD1	133	$\overline{\text{RAS0}}$	71
PAD2	132	$\overline{\text{RAS1}}$	70
PAD3	131	$\overline{\text{RAS2}}$	69
PAD4	130	$\overline{\text{RAS3}}$	68
PAD5	129	$\overline{\text{RAS4}}$	66
PAD6	128	$\overline{\text{RAS5}}$	64
PAD7	127	$\overline{\text{RESET}}$	176
PAD8	126	$\overline{\text{SERR}}$/DREQ	85
PAD9	123	$\overline{\text{SMIACT}}$	162
PAD10	122	$\overline{\text{STOP}}$	88
PAD11	121	$\overline{\text{TRDY}}$	92
PAD11	121	W/$\overline{\text{R}}$/INV	161
PAD12	120	+3.3V	32,169,208
PAD13	119	+5V	20,65,76,91, 124,136
PAD14	118		
PAD15	117		
PAD16	116		
PAD17	115		
PAD18	114		
PAD19	113		
PAD20	112		
PAD21	111		

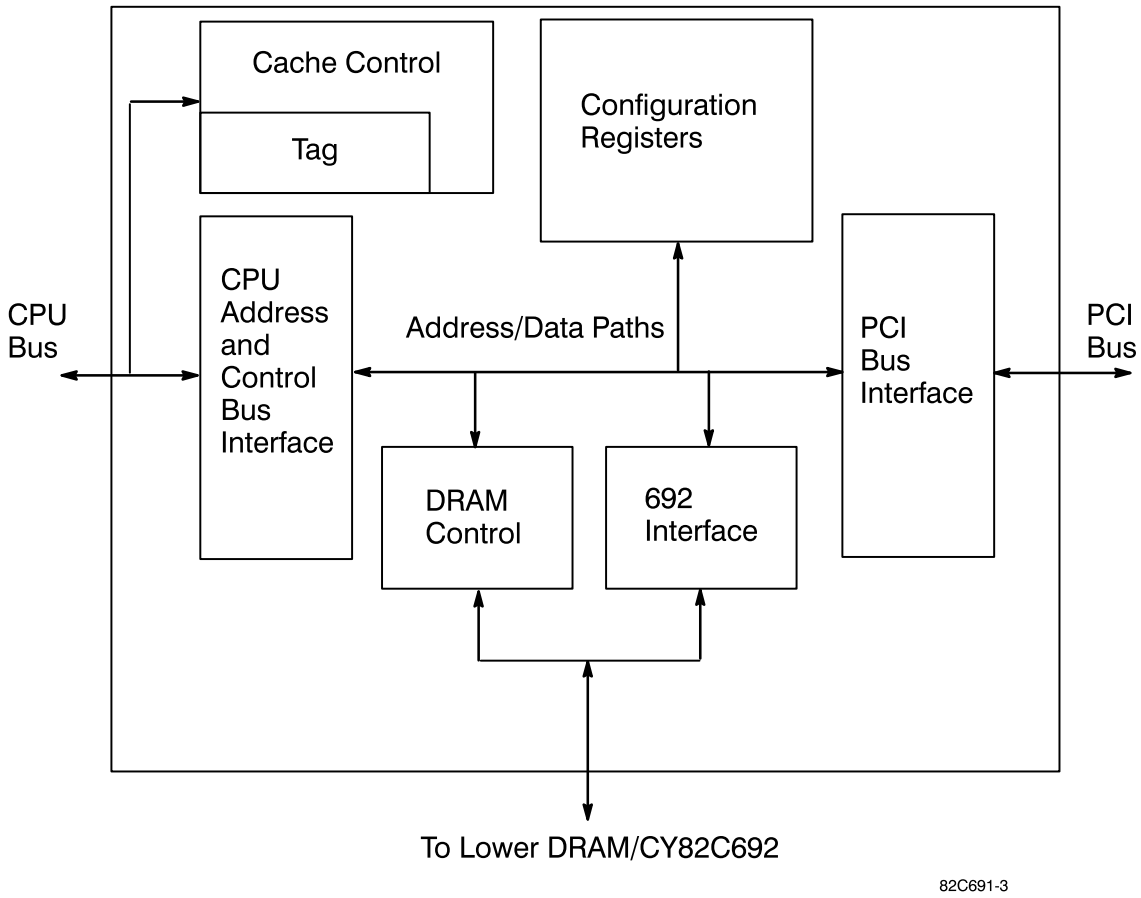


Figure 1. CY82C691 Functional Block Diagram

Introduction

System Overview

The hyperCache™ family is a family of three chipsets created to provide flexible solutions for today's PC designs. The hC-ZX, hC-VX, hC-DX Chipsets provide all the functions necessary to implement a 3.3V Pentium-class processor based system with the USB (Universal Serial Bus), PCI (Peripheral Component Interconnect), and the ISA (Industry Standard Architecture) buses. System designers can exploit the advantages of the USB and PCI buses while maintaining access to the large base of ISA cards in the marketplace.

The Cypress hyperCache family offers system designers several key advantages. With only three chips, a complete system can be implemented. Cache can be added up to 1 MB with additional CY82C694 devices in 128-KB increments All chipset solutions are pin-compatible and provide flexible upgrade paths through on-board or external cache modules. Six banks of page-mode or EDO DRAM further increase the system designer's options. The chipset also contains concurrent bus support, PCI enhanced IDE with CD-ROM support, integrated RTC, integrated peripheral control (Interrupts/ DMA), and integrated keyboard controller. This chipset is flexible enough to provide the system designer with many cost/performance/function options to provide an optimum solution for a given design.

CY82C691 Introduction

The CY82C691 System Controller provides the interfaces to the CPU, PCI, and DRAM buses. It also integrates the memory controller, cache controller, cache tag, and the CPU bus controller. *Figure 1* shows a block diagram of the CY82C691.

Functional Overview

The CY82C691 System Controller is a highly integrated device. It provides control for the CPU, cache, memory, and PCI. The memory controller supports up to 768 MB of main memory with standard page-mode DRAMs or EDO DRAMs. The cacheable range can be configured to cover the entire DRAM main system memory space. Support is provided for up to 6 banks of 72-bit wide DRAM SIMMs (parity checking/generation is provided by the CY82C692 / CY82C690). Asymmetrical DRAM banks are also supported. 20 mA outputs with programmable drive are provided on the DRAM lines, thus eliminating the need for external buffers.

The cache controller supports a look-aside (parallel) cache with synchronous flow-through or pipelined burst SRAMs. Asynchronous SRAMs are not supported. Burst reads and writes to and from the cache with 3-1-1-1 timing are maintained even at 66 MHz. The CY82C691 integrates an 8Kx21 tag-RAM to further reduce system cost. The tag can be configured to be either direct mapped or two-way set associative. Cache sizes can range from 128 KB to 1 MB in 128-KB increments. Support is provided for asymmetrical SRAM banks. For example, a 384-KB cache can be configured with the 128-KB cache in the CY82C692 and a 256-KB external expansion cache. For cache bank sizes greater than or equal to 512 KB, the cache is sectored with two lines per sector. Cache coherency with main memory is maintained at all times.

Bus concurrency is supported between the CPU, cache, DRAM, and PCI bus with the use of post-write and pre-read FIFOs. Pentium pipelined addressing and power management features (SMM) are supported. The CY82C691 also supports the Cyrix 6x86 (M1) processor and the AMD K5 processor. The CY82C691 also generates all the control for the CY82C692 /CY82C690 Data Path/Cache chip.

PCI Bus

The purpose of this section is to give an overview of PCI, the motivation behind it, and its features. Basic transfers and rules are discussed. For a detailed description of the PCI bus, all of the rules and requirements, see PCI Specification, Revision 2.1.

The PCI Bus was defined in order to satisfy the growing need for a standardized high-speed local bus that is independent of the processors, operating system, and CPU bus speed. New generations of computers incorporating I/O intensive software will require bandwidth that cannot be satisfied with the traditional I/O architectures. The PCI specification 2.1 addresses these requirements and provides an upgrade path for future requirements. Some of the PCI features include:

- Processor Independent
- Multiplexed, Burst Mode Operation
- 120 MBytes/sec usable throughput (32-bit data path)
- Three physical address spaces
  - — Memory
  - — I/O
  - — Configuration
- Hidden Arbitration

PCI is defined as a synchronous bus with a maximum clock rate of 33 MHz. All transfers take place on the rising edge of the clock (PCICLK). The basic data transfer in PCI is a burst. A burst transfer consists of an address phase, followed by one or more data phases. The address phase is defined as the first rising edge of the clock where $\overline{\text{FRAME}}$ is asserted (LOW). During the Address phase, the Master (also referred to as the initiator) asserts the appropriate address on the address/data lines (AD[31:0]) while also asserting the appropriate command on the Command/Byte Enable C/$\overline{\text{BE}}$[3:0] lines. With the information transferred during the address phase, all PCI devices, including the slave (or Target), can determine: (1) whether the transaction falls within its designated address range, (2) the kind of transfer that will take place (e.g., a read or write to memory, I/O, or configuration space), and (3) how to respond to that particular command.

Once a device recognizes that it is the target for the transaction, it claims the transactions by asserting Device Select ($\overline{\text{DEVSEL}}$) LOW. $\overline{\text{DEVSEL}}$ must be asserted LOW in order for any information to be transferred.

The address phase is followed by one or more data phases. Whether the initial data phase occurs on the subsequent clock edge is determined by the type of transaction and the ability of either agent to provide/accept the data within the appropriate time period. Since the address and data lines are multiplexed, a normal read operation requires a "turn-around" cycle to avoid bus contention. During this cycle, control of the Address/Data lines is transferred from the master to the slave, which must now use these lines to drive out the requested information. During a write operation, this "turn-around" cycle is not required since the master is providing the write data and does not have to relinquish control of the bus. PCI also allows both the master and the slave to insert wait states should either require additional cycles in order to complete the transfer. This is accomplished with the Initiator Ready signal ($\overline{\text{IRDY}}$) and the Target Ready signal ($\overline{\text{TRDY}}$). Deasserting (HIGH) either of these signals during the

data phase of the transaction will insert a wait state, thereby preventing data from being transferred during that cycle. The data presented on the AD[31:0] lines is transferred during a data phase on the rising edge of the clock when ALL of the following signals are active (LOW): DEVSEL, TRDY, IRDY, and FRAME (except during the final data phase, when FRAME is HIGH, which is explained later).

Transactions are normally terminated by the Master which deasserts FRAME (HIGH) to signal that the next data phase is the final data phase. By doing so, all of the agents on the bus, including the Target and the Arbiter, recognize that the current transaction is coming to an end. This advanced notice allows the Arbiter to grant ownership of the bus to the next requesting agent. This is referred to as Hidden Arbitration since no additional clock cycles are consumed. The new Master will not start to drive the bus until the current transaction is actually completed. The transaction is complete when the PCI bus is IDLE (FRAME and IRDY both HIGH). The Target has the ability to abort the transaction prematurely (by asserting the STOP signal) should the need arise, although this is not the typical method of termination.

Arbitration in PCI is access based instead of time-slot based. This is accomplished through a simple request-grant handshaking scheme through a central arbiter. Each agent has dedicated request and grant lines to the arbiter. A bus Master must request and be granted bus ownership each time a transaction is desired.

PCI defines three different physical address spaces: memory, I/O, and configuration space. Each of these address spaces has its own characteristics. Therefore, transactions to each space are handled differently. The memory and I/O address spaces are customary, but the configuration address space has been defined by PCI in order to support hardware configuration.

The CY82C691 functions as a high-performance PCI host bridge from the processor to the PCI bus. During PCI to main memory cycles the CY82C691 acts as a target on the PCI bus, allowing masters to read and write to main memory. For CPU cycles, the CY82C691 acts as a PCI master. The CY82C691 supports burst and single transfers, and will burst whenever possible. The CY82C691 is also parked on the PCI bus (default owner) so the CPU will have use of the bus without incurring arbitration overhead.

The CY82C691 also has a local arbiter which controls the ownership of the local memory bus. Arbitration is performed between the CPU, PCI, shared DRAM peripheral, and DRAM refresh. While one device owns the memory bus others may continue to operate without being held. See the section on concurrent bus operation.

A more detailed discussion is provided in the CY82C693 data sheet. See also PCI Spec Rev 2.1.

Address Space

The purpose of this section is to explain the memory and I/O address space mapping used by the CY82C691.

The CY82C691 recognizes two different physical address spaces: memory and I/O. Transactions to these two address spaces are handled differently, and therefore need to be distinguished from one another. The CY82C691 differentiates between these two different types of transactions by monitoring the M/IO signal from the CPU bus or the C/BE signals from the PCI bus. For CPU initiated I/O cycles, the CY82C691 decodes for accesses to its configuration registers. If the access is not to one of its registers, then the transaction is passed onto the PCI bus, including interrupt acknowledge cycles. For CPU-initiated memory cycles, the CY82C691 decodes the address based on its memory configuration registers. If the CPU address falls inside the memory range programmed in the registers, then the cycle is forwarded to memory, otherwise it is passed on to the PCI bus. As a PCI target, the CY82C691 only responds to memory cycles. CPU writes to PCI memory spaces are posted (stored in an on-chip FIFO) to improve throughput. As per the PCI specification, CPU writes to PCI I/O space are not posted in the on-chip FIFO.

I/O Address Space

Although the I/O address space can extend the full 32 bits (a possible 4 GB of I/O address space), I/O transactions are limited to the lower 64 KB (0000h-FFFFh). The remaining address locations are not valid I/O address space. In addition, the lower 1 KB (0000h-03FFh) of I/O space has been assigned as AT I/O space. The CY82C691 only decodes for I/O accesses to its on-chip configuration registers. All other I/O cycles are forwarded to PCI where the decoding is handled by the CY82C693. The CY82C693 is the subtractive decode agent on the PCI bus and it directs all unclaimed transactions to the ISA bus. See the CY82C693 data sheet for more details.

Memory Address Space

The CY82C691 supports up to 768 MB of local memory space. The full 4-GB memory space can be mapped over the local memory or PCI spaces. This mapping allows the CY82C691 to determine the destination of the transaction and respond appropriately. Memory address ranges are programmed in the CY82C691 at system startup. Address ranges can be assigned to either PCI space or main memory, cacheable or non-cacheable. All transactions not destined to main memory are forwarded to the PCI bus.

PCI Configuration Space

The CY82C691 supports the preferred PCI Configuration Mechanism #1 that allows PCI configuration cycles to be generated by software. Both Type 0 and Type 1 configurations accesses are also supported. All required fields within the Configuration Header Space are also supported.

L2 Cache Controller

The purpose of this section is to describe the basic operation of the CY82C691 L2 cache controller. The CY82C691 integrates a high performance WB/WT cache controller providing an integrated tag SRAM and a full first and second level cache coherency mechanism. Level 2 cache sizes up to 1 MB are supported through the use of the 128 KB of cache in the CY82C692 and external synchronous or pipelined burst SRAMs. The tag is two-way set associative or direct mapped and can be configured to support either WB (optional dirty bit in tag) or WT write policy. Write allocation is not supported.

The tag SRAM inside the CY82C691 is an 8Kx21 RAM organized as two 8Kx10 RAMs, TAGA and TAGB, and an 8Kx1 RAM for the LRU bit. If write-back operation is selected, one of the tag bits can optionally become the modified bit. If no modified bit is used, all cache lines are assumed dirty (modified).

The CY82C692 integrates 128 KB of BSRAM on-chip, and provides data buffering, and parity generation and checking. More information on the data BSRAMs in the CY82C692 is provided in the CY82C692 datasheet. *Table 1* shows the supported cache sizes, the tag data, the tag address, and the cacheable range.

Table 1. Cache Tag Configurations (no dirty bit)

Cache Size per bank (1 or 2 banks are allowed)	Tag Address	Tag Data	Maximum Cacheable Range
128 KB	A16–A5	A26–A17	128 MB
256 KB	A17–A5	A27–A18	256 MB
512 KB	A17–A5	A28–A19	512 MB

The cache controller supports 1 or 2 banks of SRAM, with a maximum size of 512 KB per bank. The controller also supports the mixing of pipelined and non-pipelined SRAMs to provide optimum flexibility for the system designer.

The CY82C691 provides burst read/write performance of 3-1-1-1 for direct mapped or two-way set associative two-bank configurations. The timing of the L2 controller is programmable to allow the system designer greater flexibility in the design. Wait states can be added for all cache configurations.

Cache Configurations

Below is a list of the supported cache configurations with the associated cache sizes.

Direct mapped (non-sectored) − 128KB, 256KB, 512KB
Direct mapped (sectored) − 1MB
Two-way set (non-sectored, 1 bank) − 128KB, 256KB, 512KB
Two-way set (sectored, 1 bank) − 1MB
Two-way set (non-sectored, 2 banks) − 256KB, 384KB, 512KB
Two-way set (sectored, 2 banks) − 640KB, 768KB, 896KB, 1MB

The cache configurations above can be implemented with the use of CY82C692s with CY82C694s or external BSRAMs (pipelined or synchronous).

L2 Cache Operation

Before discussing the detailed operation of the of the CY82C691 cache subsystem, it is important to define some key terms associated with caches.

Cache hit/miss cycle: These cycles occur on all CPU memory references. The CPU initiates a memory cycle by asserting the address along with $\overline{\text{ADS}}$ in the T1 cycle (first cycle of the transfer). The CY82C691 takes the high order address bits and compares them to the stored tag data in the location pointed to by the low order address bits. For direct-mapped configurations, one comparison is done and in two-way set configurations, two comparisons are done simultaneously. When a match is detected and the referenced memory location is cacheable ($\overline{\text{CACHE}}$ LOW from the CPU and $\overline{\text{KEN}}$ LOW from the memory controller) a cache hit cycle takes place and data is returned from (or written to) the data SRAMs. If there is no match found by the comparator, then the cycle is a cache miss and data is returned from (or written to) main memory. An access to non-cacheable memory is neither a hit or a miss. The cycle is just forwarded to the memory controller and the tag is not updated.

Valid bit: A mechanism for determining if the entries in the tag contain valid data. For all cache sizes except 1MB, there is no valid bit in the CY82C691. All lines are assumed and kept valid at all times. At power up, BIOS software is responsible for initializing the cache with valid data. For 1 MB cache sizes, there are two valid bits in each entry in the tag because each tag entry controls two cache lines.

Dirty bit: A mechanism for monitoring coherency between the cache and system memory when using the write-back policy. This feature is programmable in the CY82C691. A cache line is set to dirty (modified) whenever any portion of the line is written. If not used, all lines are assumed dirty. Not using a dirty bit increases the cacheable memory range.

Linefill: This type of cycle occurs on a CPU read miss to a cacheable address. It involves reading a new line from system memory and storing it in the cache.

Castout: This type of cycle occurs on a CPU read miss to a cacheable address if the line that will be replaced is dirty. In this case the dirty line is stored back to memory (or the appropriate write buffer) prior to the linefill taking place.

CPU Write Cycle

If the CY82C691 is in write-through mode and there is a cache hit, both the cache and the main memory are updated. A write hit to a cache line in write-back mode will only update the cache; however, the line will be marked dirty. If there is a cache miss, only main memory is updated. A linefill is not performed (no write allocate).

CPU Read Cycle

If there is a cache hit, the data is transferred from the cache to the CPU. Main memory is not accessed.

If there is a cache miss, the line containing the requested data is transferred from main memory to the cache and the corresponding data is returned to the CPU. In the case of write-back, if the line is dirty, a castout is performed prior to the linefill.

Cache Coherency

The snoop mechanism in the CY82C691 ensures data coherency between the L1 cache, L2 cache, and main memory. For write-back caches, the term “inquiry” is often used to describe the snooping operation.

The CY82C691 monitors all master accesses to main memory and the caches. When an external master (PCI) issues an access to the main memory, the CY82C691 will generate an inquiry cycle to the CPU by driving AHOLD, putting memory address on the CPU bus, and asserting $\overline{\text{EADS}}$. If the CPU asserts $\overline{\text{HITM}}$, in response to the inquiry, the CY82C691 will let the CPU issue the write-back cycle and hold off the master until the CPU cycle completes. The master is then allowed to proceed with the transfer.

To maintain coherency in the L2 cache, the CY82C691 also snoops the L2. If a master memory read hit occurs, data will be supplied from the SRAMs. On a memory read miss, data is supplied from the DRAMs. In the case of a cache write hit, data will be written to the SRAMs. A write miss cycle will only write data to the DRAMs. Master cycles are covered in detail in the next section.

PCI Master Read from Memory

A PCI master wins ownership of the PCI bus and initiates a read cycle. The CY82C691 detects $\overline{\text{FRAME}}$ asserted and decodes the address. If the access is targeted at main memory, the CY82C691 will drive $\overline{\text{DEVSEL}}$ active. The CY82C691 begins the memory read cycle and snoops the L1 and the L2. Several situations may occur; L1 clean hit/L2 hit, L1 dirty hit/L2 hit, L1 clean hit/L2 miss, L1 dirty hit/L2 miss, L1 miss/L2 hit, and L1 miss/L2 miss. There’s no need to differentiate between L2 dirty or clean. The data in the L2, dirty or clean, will be returned to the master on an L2 hit. The L2 data is the most current.

L1 clean hit/L2 hit: Data is returned to the master from the L2 cache. The L1 cache line is marked shared (INV deasserted). The CPU is backed off during this procedure.

L1 dirty hit/L2 hit: The master is held, the CPU is allowed to perform the castout of the dirty line, the line is written to the L2 cache and the appropriate data is returned to the master. The CPU marks the line invalid.

L1 clean hit/L2 miss: Data is returned from the DRAMs to the master.

L1 dirty hit/L2 miss: The CPU is allowed to castout the modified line and invalidate it. The data is written to the memory and returned to the master.

L1 miss/L2 hit: Data is supplied to the master from the L2 cache. The CPU is backed off.

When both snoops are misses, the memory cycle is allowed to proceed and the data is returned to the master from main memory.

PCI Master Write to Memory

A master wins ownership of the PCI bus and initiates a write cycle. The CY82C691 detects $\overline{\text{FRAME}}$ asserted, decodes the address, and drives $\overline{\text{DEVSEL}}$ active. The CY82C691 begins the memory write cycle and snoops the L1 and L2. The same snoop results can occur as in the memory read case.

L1 clean hit/L2 hit: The line in the CPU is invalidated and the master data is written to the L2 cache and main memory.

L1 dirty hit/L2 hit: The master is held, the CPU performs the castout of the line, the line is written to the L2 where it is marked dirty, and the CPU invalidates the line in the L1. The master data is then written to the L2 cache and main memory,

L1 clean hit/L2 miss: The CPU invalidates the line and the data is written to main memory.

L1 dirty hit/L2 miss: The CPU performs the castout and invalidates the line in the L1. The CPU data is written to main memory followed by the master data.

L1 miss/L2 hit: The master data is written to both the L2 cache and to main memory. If the line in the L2 was clean, it is marked dirty. If it was dirty, it remains dirty.

If both snoops miss, the memory cycle is allowed to proceed. Data is written to main memory.

PCI Clock

The PCI clock that is provided to the CY82C691 must be the CPU clock divided by two. Thus a clock phase relationship is maintained and no extra delay is incurred in the synchronization of PCI signals to the CPU clock frequency. The CY2254A−2 clock generator from Cypress provides all of the necessary PCI and CPU clocks.

DRAM Memory Controller

The DRAM controller in the CY82C691 provides the control of the memory subsystem by driving the memory address, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{DWE}}$. It interfaces main memory to the CPU bus and PCI bus. The CY82C691 provides all the DRAM control signals and the lower 32-bit data path to the DRAMs (the upper 32-bit data path is supported by the CY82C692). The data path is also used to pass data from/to PCI to/from the CPU or DRAM. For more information on the data paths see the CY82C692 data-sheet. Up to 12 single-sided or 6 double-sided 72-pin SIMMs with a maximum memory size of 768 MB are supported.

The DRAM controller is extremely flexible and is fully configurable through registers to provide optimum configuration for the given application.

The CY82C691 controls six banks of DRAM, each bank with a maximum size of 16M x 64 bits yielding 768 MB total memory. The memory controller supports standard page-mode DRAMs as well as EDO DRAMs. Different speeds are supported through programming of the DRAM controller configuration registers. EDO DRAMs provide better performance over page-mode DRAMs. DRAM sizes up to 16 Mbit are supported by providing 12 memory address lines. In addition, page size selection from 6 to 12 address bits is available independent of DRAM size. The memory address, $\overline{\text{CAS}}$, and DRAM write enable signals are driven with programmable buffers to eliminate the need for external buffering. The user can choose between 8-mA, 12-mA, and 20-mA drive strength. The $\overline{\text{RAS}}$ signals are fixed at 20mA of drive strength Parity support is provided in the CY82C691. The CY82C692 performs all the parity generation and checking. However, parity generation and checking is enabled or disabled via the CY82C691.

The CY82C691 memory controller supports asymmetrical DRAM banks. This means that each bank may be a different type (EDO or page-mode), a different variety (different page size DRAMs), different speed, or different density. The only restriction is that all DRAMs within a given bank are the same. Support for automatic EDO detection is also provided.

DRAM Performance

The CY82C691 DRAM performance can be controlled through the use of the configuration registers. Various DRAM timing parameters may be changed to adjust memory performance. Programmable timings allow the use of different DRAM types. There is also support for EDO DRAMs to further increase performance. The signals for EDO are the same for that of standard DRAM. EDO output disabling is controlled using the $\overline{\text{DWE}}$ signal.

Table 2 below shows the optimum DRAM timing. The numbers are based on 60-ns DRAMs with the system running at 66 MHz.

Table 2. DRAM Performance

Cycle Type	Burst Timing
DRAM Read page hit/row miss/page miss	6/9/12-3-3-3 Page-Mode 6/9/12-2-2-2 EDO
DRAM Writepage hit/row miss/ page miss	6/9/12-3-3-3 Page-Mode 6/9/12-3-3-3 EDO
Posted Write(write to CY82C692 FIFO)	4-1-1-1

Shadow RAM

The CY82C691 provides shadow RAM support to speed up accesses to system ROM. ROM code is copied to a reserved RAM space and write protected. All subsequent accesses to ROM will be routed to DRAM, thus improving performance.

Refresh

Refresh of the DRAM array is performed using the CAS before RAS refresh mechanism. The timing of refresh cycles is derived from the PCI clock and is totally independent of expansion bus refresh cycles. The CPU is not held during refresh cycles. Refresh

cycles will be deferred until the DRAM interface is idle, provided the DRAM refresh requirements are not violated.

Shared DRAM Bus Support

The CY82C691 supports the VESA Unified Memory Architecture (VUMA) for sharing the DRAM bus with external peripherals such as graphics adapters or digital video chips. The chipset implications involve DRAM arbitration and DRAM protection. The CY82C691 provides a DRAM request signal ($\overline{DREQ}$) and a DRAM grant signal ($\overline{DGNT}$) for arbitration. The arbitration scheme allows for low and high priority requests. When a DRAM peripheral wants access to memory, it asserts a low priority request (drives $\overline{DREQ}$ LOW). If the memory bus is idle, the low priority request will be honored. If the CY82C691 is using main memory to service the CPU, low-priority DRAM requests will not be honored. If the DRAM bus is busy, and the VUMA peripheral has a time-critical need to use the bus, it will raise the priority to high (by deasserting $\overline{DREQ}$ for one clock cycle and reasserting $\overline{DREQ}$). The CY82C691 will relinquish control of the memory bus within 35 CPU clock cycles after detecting a high-priority request. The VUMA peripheral device wins control of the bus when the CY82C691 floats all of the DRAM control signals and asserts $\overline{DGNT}$. When the VUMA peripheral sees $\overline{DGNT}$ asserted (LOW), it will take control of the DRAM memory bus. This allows the peripheral to access main memory directly. Because both the CY82C691 and the VUMA peripheral have independent DRAM controllers, the DRAM timing for the peripheral can be independent of the CY82C691 DRAM timing.

The VUMA peripheral device is allowed to "park" on the memory bus. This means that the VUMA device is not required to relinquish the bus after it finishes a transaction. It can remain on the memory bus as long as the CPU has no need to go to main memory. If the CPU wants to access system memory and the VUMA peripheral is parked on the memory bus, the CY82C691 will pre-empt the VUMA device by deasserting the $\overline{DGNT}$ signal. If the VUMA peripheral is pre-empted, it must float the the memory bus and deassert $\overline{DREQ}$ within 60 CPU clock cycles. This gives memory control back to the CY82C691.

The CY82C691 provides registers to control how the peripheral DRAM space is used. The CY82C691 can be programmed to treat the peripheral memory space as reserved. If the VUMA memory space is reserved, the CPU does not have direct access to VUMA memory. However, there are system advantages to allowing the CPU direct access to the frame buffer if the VUMA device is a graphics controller.

SMM Mode Support

The Cypress Pentium chipset provides for extensive power management, through both hardware and software. Most of the power management functions are handled by the CY82C693. For more information please refer to the CY82C693 datasheet.

The CY82C691 provides control over SMM memory space. When $\overline{SMI}$ is issued to the processor by the CY82C693, the CPU enters SMM mode where it runs out of a restricted memory space. The CY82C691 provides support by providing SMM address mapping and write protection.

Pentium Class CPU Support

The CY82C691 supports Pentium-class CPUs from multiple vendors. The CY82C691 supports the Intel Pentium processor at bus speeds up to 66 MHz, the Cyrix 6x86 (M1) processor, and the AMD K5 processors.

Concurrent Bus Support

The CY82C691 supports full bus concurrency between the CPU and the PCI bus. This is made possible through the use of the L2 cache and the extensive buffering provided by the CY82C692.

The CPU can run out of the L2 cache while a PCI master has access to main memory. The CPU can go to main memory while a PCI master is going to another PCI device. The only times where a conflict will occur are when both a PCI master and the CPU want to go to main memory or when PCI and the CPU require access to the CPU bus (for an inquiry cycle). In this case, some level of concurrent bus operation may still be possible through the use of the FIFOs in the CY82C691 and CY82C692. The CY82C691 contains 8-level-deep FIFOs for post-writing and pre-reading data from PCI. The CY82C692 contains additional FIFOs. See the CY82C692 datasheet for more details.

When it is not possible to maintain concurrent bus operation, the CY82C691 arbitrates for the use of the memory bus between the CPU and PCI. If the PCI device wins, the CPU is held off and vice versa.

Byte Merge

The CY82C691 provides byte merging to speed non-32-bit transfers to sequential PCI addresses. When writing to the on-chip FIFOs, the address of the last transfer in the FIFO is stored in a special comparison location. If the address of the next byte write matches the last FIFO entry address, the data is merged into the same FIFO entry. This allows more transfers to be queued before the on-chip write FIFOs become full.

The FIFOs also contain per-byte valid bits. *Figure 2* shows a graphical representation of one of the write FIFOs.

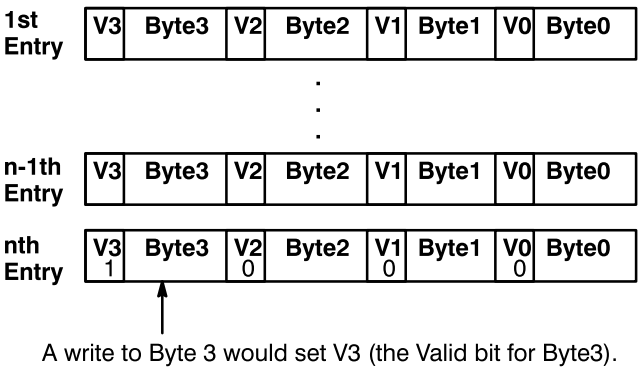


Figure 2. Byte Merge

Any byte write to a FIFO entry will set the valid bit associated with the modified byte. This ensures that only the modified bytes (valid within the write FIFOs) get written to main memory.

During byte merge operations, the cache SRAMs will be deselected. This prevents the cache write enable signals ($\overline{CWE}$'s), which are used to convey the valid bytes to be merged, from falsely writing to the cache.

CY82C691 Signal Description

The CY82C691 signals are divided into four functional areas: PCI Interface signals, CPU Interface signals, DRAM interface signals, and Miscellaneous signals.

PCI Interface

Name	I/O	Description
PAD[31:0]	I/O	PCI Address/Data Bus: Multiplexed bidirectional address/data lines on the PCI bus. The CY82C691 either drives or samples these lines during PCI cycles.
PCICLK	I	PCI Clock: PCI Clock Input. All PCI transactions are referenced to the rising edge of PCICLK.
PC/$\overline{BE}$[3:0]	I/O	PCI Command & Byte Enables: PC/$\overline{BE}$[3:0] are driven by the current bus master during the address phase to define the transaction and during the data phase as the byte enables.
$\overline{FRAME}$	I/O	Cycle Frame: Driven by the current bus master to indicate the start and duration of a transaction.
$\overline{IRDY}$	I/O	Initiator Ready: The assertion of $\overline{IRDY}$ indicates the current bus master's ability to complete the current data phase of the transaction. Used in conjunction with $\overline{TRDY}$ from the target.
$\overline{TRDY}$	I/O	Target Ready: The assertion of $\overline{TRDY}$ indicates the current target's ability to complete the current data phase of the transaction. Works in conjunction with $\overline{IRDY}$ from the master.
$\overline{DEVSEL}$	I/O	Device Select: Indicates that a PCI device has decoded that it is the target of the transaction. The target has three options for decoding: fast decoding, medium decoding, or slow decoding.
PAR	I/O	Parity: An even parity bit across PAD[31:0] and PC/$\overline{BE}$[3:0]. As a master the CY82C691 generates even parity on PCI write cycles. On read cycles the CY82C691 checks parity by sampling PAR.
$\overline{STOP}$	I/O	Stop: Indicates that the current target is requesting the master to stop the current transaction. STOP is used in conjunction with $\overline{DEVSEL}$ and $\overline{TRDY}$ to indicate a disconnect, target abort, and retry cycles.
$\overline{PLOCK}$	I	PCI Lock: Used to indicate that an atomic operation is taking place and may require multiple cycles to complete without another master interfering.
$\overline{PERR}$/$\overline{DGNT}$	I/O	Parity Error/ DRAM Bus Grant: Parity Error may be asserted by any agent that detects a parity error during the data phase of a transaction. Address parity errors are reported on $\overline{SERR}$. Also, the DRAM bus grant signal for shared DRAM bus operation.
$\overline{SERR}$/$\overline{DREQ}$	I/O	System Error/ DRAM Bus Request: System error may be asserted by any agent for reporting address parity errors or any other types of errors beside data parity. Also, the DRAM bus request signal for shared DRAM bus operation.
$\overline{GNTBSY}$	I/O	C691 Busy/ Granted: The CY82C693 asserts this signal for one clock cycle to indicate to the CY82C691 that it has been granted the PCI bus and is allowed to initiate a transaction. It is also asserted by the CY82C691 to show that the CY82C691 owns the PCI bus. If the CY82C693 owns the PCI bus, it will deassert this signal to tell the CY82C691 that the bus is not free. When not asserted the PCI bus is free to be granted to other masters.
$\overline{FREQACK}$	I/O	C691 FIFO Flush Request/Acknowledge: When asserted for one clock by the CY82C693, this signal indicates that the CY82C691 must flush its internal FIFOs. Then the CY82C691 will assert this signal to acknowledge that the FIFOs have been flushed and the CY82C693 is free to take ownership of the PCI bus for a DMA transfer.

CPU Interface

Name	I/O	Description
A[31:5]	I/O	CPU Address Bus: A[31:5] are connected to the CPU A[31:5] lines. They are inputs to the CY82C691 during CPU initiated cycles and are outputs during cache inquiry cycles.
A[4:3]	I/O	CPU Address 4 and 3: Same as above except they are not used by the processor in the Level 1 hit/miss decision during inquire cycles.
BE[7:0]	I	CPU Byte enables: The byte enables indicate which byte lanes on the CPU data bus carry valid data. The also define the type of special cycle when M/$\overline{IO}$ = D/$\overline{C}$ = 0.
$\overline{ADS}$	I	CPU Address Strobe: Used to indicate the start of a new bus cycle. Driven in the same clock as the address, byte enables, and cycle definition signals.
M/$\overline{IO}$	I	CPU Memory/IO: Driven by the CPU during the T1 to indicate a memory or I/O space access. Along with D/$\overline{C}$ and W/$\overline{R}$ make up the cycle definition signals.
D/$\overline{C}$	I	CPU Data/Code: Used by the CPU to differentiate accesses for data and instructions. Used as a cycle definition signal.
W/$\overline{R}$/INV	I/O	CPU Write/Read: Used by the CPU to define write and read cycles. Along with M/$\overline{IO}$ and D/$\overline{C}$ makes up the cycle definition signals. Also used as the invalidate signal when running in Level 1 write-back mode.
$\overline{CACHE}$	I	Cacheability: The Pentium asserts $\overline{CACHE}$ to indicate the internal cacheability of a read cycle or that a write cycle is a burst write-back. It is driven along with the cycle definition signals.
$\overline{BRDY}$	O	Burst Ready: $\overline{BRDY}$ indicates to the Pentium that the data is available in the current clock cycle.
$\overline{KEN}$	O	Cache Enable: Driven by the CY82C691 to tell the processor that the current memory cycle is cacheable. $\overline{KEN}$ is asserted for all memory accesses that are to cacheable memory as determined by the address registers in the CY82C691. These registers are fully programmable.
$\overline{NA}$	O	Next Address: Used to support CPU address pipelining. The CY82C691 asserts $\overline{NA}$ for one clock when it is ready to accept a new address from the processor, even if the current transaction hasn't completed. The CPU may drive $\overline{ADS}$ two clocks after $\overline{NA}$ is asserted.
$\overline{EADS}$	O	External $\overline{ADS}$: The CY82C691 drives $\overline{EADS}$ to indicate to the processor that a valid snoop address has been placed on the address bus.
$\overline{HITM}$	I	Hit Modified: The CPU asserts $\overline{HITM}$ to inform the CY82C691 that the inquiry cycle hit a modified line in the L1 cache. It is asserted two clocks after $\overline{EADS}$ if the hit line was in the modified state.
$\overline{BOFF}$	O	Backoff: The CY82C691 asserts $\overline{BOFF}$ to force the CPU to float the bus in the next clock cycle. The bus is floated until backoff is sampled deasserted. Outstanding bus cycles are restarted.
AHOLD	O	Bus Address Hold: AHOLD tells the CPU to float its address bus.
$\overline{LOCK}$	I	Bus Lock: CPU $\overline{LOCK}$ is used by the CPU for atomic operations.
$\overline{SMIACT}$	I	System Management Interrupt Active: Output from the processor that tells the CY82C691 that the processor is operating in SMM (System Management Mode).
CPUCLK	I	CPU Clock: External Clock. All CY82C691 timing is based off CPU clock.
BMERGE	O	Byte Merge: This signal is used to facilitate byte merging into the PCI FIFO. This pin should be tied to the $\overline{BWE}$ signal of the CY82C692.
$\overline{RESET}$	I	System Reset: The CY82C691 uses this signal to initialize the chip to a known state after system power-up.

Cache Interface Signals

Name	I/O	Description
$\overline{\text{ADVB}}$/CAC	O	Cache Sectored Address Control/Set Selector/Bank B SRAM Advance Signal: Controls the cache address line for sectoring and 2-way set, single-bank operation. Chooses whether set0 or set1 will be accessed. Also, the $\overline{\text{ADV}}$ input for Bank B when two banks of BSRAMs are used.
$\overline{\text{ADVA}}$	O	Bank A Advance Address: Tells Bank A BSRAMs to increment their internal address counters for the next clock cycle.
$\overline{\text{ADSC}}$	O	Controller $\overline{\text{ADS}}$: $\overline{\text{ADS}}$ driven by the cache controller to initiate cache accesses independent from the CPU. Driven by the CY82C691 when doing line replacements and castouts, or returning data to an external master.
$\overline{\text{CE1}}$[A:B]	O	Burst SRAM Cache Chip Select: Used with the CY82C692 and external BSRAMs for selecting the RAM. Also serves as the cache set selection for two-way set associative L2 organizations during writes.
$\overline{\text{CRD}}$[1:0]	O	Cache SRAM Output Enable: These signals are asserted by the CY82C691 when data is to be read from the L2 cache. Functions as the read set selection for two way set organizations.
$\overline{\text{CWE}}$[7:0]	O	Cache SRAM Write Enable: $\overline{\text{CWE}}$[7:0] are asserted by the CY82C691 to write data to the L2 cache BSRAMs or CY82C692 on a byte-by-byte basis.

Memory Interface

Name	I/O	Description
MA[11:0]	O	DRAM Multiplexed Address: Provide the row and column address to the DRAM array. Up to 20 mA drive (programmable) to eliminate external buffering.
$\overline{\text{RAS}}$[5:0]	O	Row Address Strobe: Used by the DRAMs to latch the row address on the DRAM address lines. Each RAS line corresponds to one bank of DRAM.
$\overline{\text{CAS}}$[7:0]	O	Column Address Strobe: Used to latch the column address on the DRAM address lines. Each CAS signal corresponds to one byte of data in the DRAM array.
$\overline{\text{DWE}}$	O	DRAM Write Enable: The signal used to initiate a write into the DRAM array.

CY82C692 Interface Signals

Name	I/O	Description
CNT[11:0]	O	692 Control: These twelve signals are used to control the CY82C692 BSRAMs and FIFOs. The CY82C691 keeps complete track of all CY82C692 transitions. CNT11 is also called ENNMIN (DRAM Parity Error NMI Enable). CNT10 is also called SELCYDH (Selects which FIFO CY or DRAM to access). CNT9 is also called SELDHDL (Selects between High Data or Low Data FIFO). CNT8 is also called ADVCYFN (Advance CY FIFO pointer). CNT7 is also called ADVMDFN (Advance MD FIFO pointer). CNT6 is also called ADVCPUF (Advance CPU FIFO pointer). CNT5 is also called SECLATN (Secondary Latch Control). CNT4 is also called PRILATN (Primary Latch Control). CNT3:0 are control state bits.
CY[31:0]	O	CY Bus: This 32-bit bus functions as the data path between the CY82C691 and the CY82C692 for PCI transfers. It also functions as the DRAM lower (bits 31 through 0) data bus.

CY82C691 PCI Configuration Registers

The PCI configuration registers for the CY82C691 are defined in this section. The registers can be accessed using a PCI configuration mechanism #1, type 0 access (See PCI Specification) with the device number field equal to 00H.

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PCI Configuration Register 00: PCI Device/Vendor Register (Read Only) — Bits 7:0 of the CONFIG_ADDRESS register=00H

Bit	Function	Default
31:16	CY82C691 Device ID	C691H
15:0	Cypress Semiconductor Vendor ID	1080H

PCI Configuration Register 04: PCI Status/Command Register — Bits 7:0 of the CONFIG_ADDRESS register=04H

Bit	Function	Default
31	(R/W) Parity Error Status: 0: No Parity Error Detected 1: Parity Error Detected Set when 691 detects a data parity error as a target or an address parity error	0
30	(R/W) System Error (PCI $\overline{\text{SERR}}$ Signal) Status: 0: No System Error Detected 1: System Error Detected	0
29	(R/W) Master Abort Status: 0: No Master Abort Occurred 1: Master Abort Occurred	0
28	(R/W) Target Abort Termination of CY82C691 Transaction Status: 0: No Target Abort Terminated CY82C691 Transaction 1: Target Abort Terminated CY82C691 Transaction	0
27	(R/W) Target Abort Termination Generated by CY82C691 Status: 0: No Target Abort Generated by CY82C691 1: Target Abort Generated by CY82C691	0
26:25	(RO) $\overline{\text{DEVSEL}}$ Assertion Timing Status: 01: Medium Decode ($\overline{\text{DEVSEL}}$ will be asserted on clock edge #3)	01
24	(R/W) Conditional Parity Error (PCI $\overline{\text{PERR}}$ Signal) Status: 0: No Parity Error Detected 1: Parity Error Detected, the CY82C691 either asserted $\overline{\text{PERR}}$ or was the master when $\overline{\text{PERR}}$ was asserted, and the PARITY ERROR RESPONSE BIT is set in the Command Register.	0
23	(RO) Fast Back-to-Back Capability Status: 0: The CY82C691 is incapable of accepting fast back-to-back transactions as a target.	0
22	(RO) User Definable Features Implementation Status: 0: The CY82C691 does not implement User Definable Features.	0
21	(RO) 66-MHz Capability Status: 0: The CY82C691 is incapable of 66-MHz PCI operation.	0
20:10	Reserved	00000000000
9	(R/W) Fast Back-to-Back Allowed: 0: One or more of the targets does not support fast back-to-back transactions. 1: All of the targets support fast back-to-back transactions. The CY82C691 can only do fast back-to-back transfers to different targets if all targets support fast back-to-back transfers. If this bit is a zero, fast back-to-back transfers are only allowed to the same target.	0
8	(R/W) System Error (PCI $\overline{\text{SERR}}$ Signal) Drive Control: 0: The CY82C691 cannot drive $\overline{\text{SERR}}$. 1: $\overline{\text{SERR}}$ driver enabled.	0

7	(R/W) Address/Data Stepping Status: 0: Address/Data Stepping Disabled 1: Address/Data Stepping Enabled (Add an additional wait state).	1
6	(R/W) Parity Error Reporting Control: 0: Ignore PCI Parity Errors. 1: PCI Parity Error Detection Enabled..	0
5	(RO) VGA Palette Snooping Status: 0: VGA Palette Accesses are Treated Like Normal Transactions (Palette Snooping Disabled).	0
4	(RO) Memory Write and Invalidate Status: 0: The CY82C691 will not generate PCI Memory Write and Invalidate cycles.	0
3	(R/W) Special Cycle Response: 0: The CY82C691 will ignore Special Cycles. 1: The CY82C691 will monitor Special Cycles.	0
2	(R/W) PCI Bus Mastering Control: 0: CY82C691 PCI bus mastering disabled. 1: CY82C691 PCI bus mastering enabled.	0
1	(R/W) PCI Bus Memory Space Control: 0: CY82C691 will not respond to memory space accesses. 1: CY82C691 will respond to memory space accesses.	0
0	(R/W) PCI Bus I/O Space Control: 0: CY82C691 will not respond to I/O space accesses. 1: CY82C691 will respond to I/O space accesses.	0

PCI Configuration Register 08: (Read Only) PCI Class/Revision Register — Bits 7:0 of the CONFIG_ADDRESS register=08H

Bit	Function	Default
31:8	Class Code= Bridge Device	060000H
7:0	Revision ID	00H

PCI Configuration Register 80: (Read/Write) DRAM Row Boundary Register for Banks 1 and 0— Bits 7:0 of the CONFIG_ADDRESS register=80H

Bit	Function	Default
31:23	Bank 1 Upper Address Limit A[29:21].	000000000
22:20	Reserved	000
19	Bank 1 Page Size Control: 0: Page Sizing Disabled 1: Page Size is set to 2 KB for DRAMs with 12 row and 8 column addresses. Page Size is set to 4 KB for all other DRAMs.	0
18:17	Bank 1 Row/Column Address Split Control: 00: R12/C12, R11/C11, R11/C10, R10/C10, R10/C9, and R9/C9 Combinations 01: R12/C10 10: R12/C9 11: R12/C8	00
16	Reserved	0
15:7	Bank 0 Upper Address Limit A[29:21].	000000001
6:4	Reserved	000
3	Bank 0 Page Size Control: 0: Page Sizing Disabled 1: Page Size is set to 2 KB for DRAMs with 12 row and 8 column addresses. Page Size is set to 4 KB for all other DRAMs.	0
2:1	Bank 0 Row/Column Address Split Control: 00: R12/C12, R11/C11, R11/C10, R10/C10, R10/C9, and R9/C9 Combinations 01: R12/C10 10: R12/C9 11: R12/C8	00
0	Reserved	0

PCI Configuration Register 84: (Read/Write) DRAM Row Boundary Register for Banks 3 and 2 — Bits 7:0 of the CONFIG_ADDRESS register=84H

Bit	Function	Default
31:23	Bank 3 Upper Address Limit A[29:21].	000000000
22:20	Reserved	000
19	Bank 3 Page Size Control: 0: Page Sizing Disabled 1: Page Size is set to 2 KB for DRAMs with 12 row and 8 column addresses. Page Size is set to 4 KB for all other DRAMs.	0
18:17	Bank 3 Row/Column Address Split Control: 00: R12/C12, R11/C11, R11/C10, R10/C10, R10/C9, and R9/C9 Combinations 01: R12/C10 10: R12/C9 11: R12/C8	00
16	Reserved	0
15:7	Bank 2 Upper Address Limit A[29:21].	000000000
6:4	Reserved	000
3	Bank 2 Page Size Control: 0: Page Sizing Disabled 1: Page Size is set to 2 KB for DRAMs with 12 row and 8 column addresses. Page Size is set to 4 KB for all other DRAMs.	0
2:1	Bank 2 Row/Column Address Split Control: 00: R12/C12, R11/C11, R11/C10, R10/C10, R10/C9, and R9/C9 Combinations 01: R12/C10 10: R12/C9 11: R12/C8	00
0	Reserved	0

PCI Configuration Register 88: (Read/Write) DRAM Row Boundary Register for Banks 5 and 4— Bits 7:0 of the CONFIG_ADDRESS register=88H

Bit	Function	Default
31:23	Bank 5 Upper Address Limit A[29:21].	000000000
22:20	Reserved	000
19	Bank 5 Page Size Control: 0: Page Sizing Disabled 1: Page Size is set to 2 KB for DRAMs with 12 row and 8 column addresses. Page Size is set to 4 KB for all other DRAMs.	0
18:17	Bank 5 Row/Column Address Split Control: 00: R12/C12, R11/C11, R11/C10, R10/C10, R10/C9, and R9/C9 Combinations 01: R12/C10 10: R12/C9 11: R12/C8	00
16	Reserved	0
15:7	Bank 4 Upper Address Limit A[29:21].	000000000
6:4	Reserved	000
3	Bank 4 Page Size Control: 0: Page Sizing Disabled 1: Page Size is set to 2 KB for DRAMs with 12 row and 8 column addresses. Page Size is set to 4 KB for all other DRAMs.	0
2:1	Bank 4 Row/Column Address Split Control: 00: R12/C12, R11/C11, R11/C10, R10/C10, R10/C9, and R9/C9 Combinations 01: R12/C10 10: R12/C9 11: R12/C8	00
0	Reserved	0

PCI Configuration Register 8C: (Read/Write) Byte Merge Control Register— Bits 7:0 of the CONFIG_ADDRESS register=8CH

Bit	Function	Default
31	Reserved	0
30:16	Byte Merge Start Address bits A[31:17] Byte accesses between the start and end address are capable of being byte merged into internal FIFO.	000000000000000
15	Byte Merge Control: 0: Byte Merge Disabled. 1: Byte Merge Enabled.	0
14:0	Byte Merge End Address bits A[31:17] Byte accesses between the start and end address are capable of being byte merged into internal FIFO.	000000000000000

PCI Configuration Register 90: Memory Control Register #1 (Read/Write) − Bits 7:0 of the CONFIG_ADDRESS register=90H

Bit	Function	Default
31	Address Block D0000H−D3FFFH Cacheable Control 0: This address block is not cacheable in the level 2 cache. 1: This address block is cacheable in the level 2 cache.	0
30	Address Block D0000H−D3FFFH DRAM Write Control 0: This address block is not writeable to DRAM Memory 1: This address block is writeable to DRAM Memory	0
29	Address Block D0000H−D3FFFH DRAM Read Control 0: This address block is not readable from DRAM Memory 1: This address block is readable from DRAM Memory	0

2	Address Block D4000H−D7FFFH Cacheable Control 0: This address block is not cacheable in the level 2 cache. 1: This address block is cacheable in the level 2 cache.	0
27	Address Block D4000H−D7FFFH DRAM Write Control 0: This address block is not writeable to DRAM Memory 1: This address block is writeable to DRAM Memory	0
26	Address Block D4000H−D7FFFH DRAM Read Control 0: This address block is not readable from DRAM Memory 1: This address block is readable from DRAM Memory	0
25	Address Block D8000H−DBFFFH Cacheable Control 0: This address block is not cacheable in the level 2 cache. 1: This address block is cacheable in the level 2 cache.	0
24	Address Block D8000H−DBFFFH DRAM Write Control 0: This address block is not writeable to DRAM Memory 1: This address block is writeable to DRAM Memory	0
23	Address Block D8000H−DBFFFH DRAM Read Control 0: This address block is not readable from DRAM Memory 1: This address block is readable from DRAM Memory	0
22	Address Block DC000H−DFFFFH Cacheable Control 0: This address block is not cacheable in the level 2 cache. 1: This address block is cacheable in the level 2 cache.	0
21	Address Block DC000H−DFFFFH DRAM Write Control 0: This address block is not writeable to DRAM Memory 1: This address block is writeable to DRAM Memory	0
20	Address Block DC000H−DFFFFH DRAM Read Control 0: This address block is not readable from DRAM Memory 1: This address block is readable from DRAM Memory	0
19	Address Block E0000H−EFFFFH Cacheable Control 0: This address block is not cacheable in the level 2 cache. 1: This address block is cacheable in the level 2 cache.	0
18	Address Block E0000H−EFFFFH DRAM Write Control 0: This address block is not writeable to DRAM Memory 1: This address block is writeable to DRAM Memory	0
17	Address Block E0000H−EFFFFH DRAM Read Control 0: This address block is not readable from DRAM Memory 1: This address block is readable from DRAM Memory	0
16	Address Block F0000H−FFFFFH Cacheable Control 0: This address block is not cacheable in the level 2 cache. 1: This address block is cacheable in the level 2 cache.	0
15	Address Block F0000H−FFFFFH DRAM Write Control 0: This address block is not writeable to DRAM Memory 1: This address block is writeable to DRAM Memory	0
14	Address Block F0000H−FFFFFH DRAM Read Control 0: This address block is not readable from DRAM Memory 1: This address block is readable from DRAM Memory	0
13:0	End of Local Memory (with 64 KB granularity): $\overline{A29}$, $\overline{A28}$, $\overline{A27}$, $\overline{A26}$, $\overline{A25}$, $\overline{A24}$, $\overline{A23}$, $\overline{A22}$, $\overline{A21}$, $\overline{A20}$, $\overline{A19}$, $\overline{A18}$, $\overline{A17}$, $\overline{A16}$ Note: This register programs the upper address of local DRAM memory. Any accesses above the address range programmed in this register will be passed to the PCI bus. The address bits in this register are inverted (so the default 00000000000000 will set the maximum memory address to 1 Gigabyte or 3FFFFFFFH)	00000000000000

PCI Configuration Register 94: Memory Control Register #2 (Read/Write) — Bits 7:0 of the CONFIG_ADDRESS register=94H

Bit	Function	Default
31:30	Reserved	00
29	DRAM Bank 5 EDO Control: 0: This bank is populated with Fast-Page-Mode (Not EDO) DRAMs 1: This bank is populated with EDO DRAMs	0
28	DRAM Bank 4 EDO Control: 0: This bank is populated with Fast-Page-Mode (Not EDO) DRAMs 1: This bank is populated with EDO DRAMs	0
27	DRAM Bank 3 EDO Control: 0: This bank is populated with Fast-Page-Mode (Not EDO) DRAMs 1: This bank is populated with EDO DRAMs	0
26	DRAM Bank 2 EDO Control: 0: This bank is populated with Fast-Page-Mode (Not EDO) DRAMs 1: This bank is populated with EDO DRAMs	0
25	DRAM Bank 1 EDO Control: 0: This bank is populated with Fast-Page-Mode (Not EDO) DRAMs 1: This bank is populated with EDO DRAMs	0
24	DRAM Bank 0 EDO Control: 0: This bank is populated with Fast-Page-Mode (Not EDO) DRAMs 1: This bank is populated with EDO DRAMs	0
23	Address Block A0000H−A7FFFH Cacheable Control 0: This address block is not cacheable in the level 2 cache. 1: This address block is cacheable in the level 2 cache.	0
22	Address Block A0000H−A7FFFH DRAM Write Control 0: This address block is not writeable to DRAM Memory 1: This address block is writeable to DRAM Memory	0
21	Address Block A0000H−A7FFFH DRAM Read Control 0: This address block is not readable from DRAM Memory 1: This address block is readable from DRAM Memory	0
20	Address Block A8000H−AFFFFH Cacheable Control 0: This address block is not cacheable in the level 2 cache. 1: This address block is cacheable in the level 2 cache.	0
19	Address Block A8000H−AFFFFH DRAM Write Control 0: This address block is not writeable to DRAM Memory 1: This address block is writeable to DRAM Memory	0
18	Address Block A8000H−AFFFFH DRAM Read Control 0: This address block is not readable from DRAM Memory 1: This address block is readable from DRAM Memory	0
17	Address Block B0000H−B7FFFH Cacheable Control 0: This address block is not cacheable in the level 2 cache. 1: This address block is cacheable in the level 2 cache.	0
16	Address Block B0000H−B7FFFH DRAM Write Control 0: This address block is not writeable to DRAM Memory 1: This address block is writeable to DRAM Memory	0
15	Address Block B0000H−B7FFFH DRAM Read Control 0: This address block is not readable from DRAM Memory 1: This address block is readable from DRAM Memory	0
14	Address Block B8000H−BFFFFH Cacheable Control 0: This address block is not cacheable in the level 2 cache. 1: This address block is cacheable in the level 2 cache.	0

13	Address Block B8000H−BFFFFH DRAM Write Control 0: This address block is not writeable to DRAM Memory 1: This address block is writeable to DRAM Memory	0
12	Address Block B8000H−BFFFFH DRAM Read Control 0: This address block is not readable from DRAM Memory 1: This address block is readable from DRAM Memory	0
11	Address Block C0000H−C3FFFH Cacheable Control 0: This address block is not cacheable in the level 2 cache. 1: This address block is cacheable in the level 2 cache.	0
10	Address Block C0000H−C3FFFH DRAM Write Control 0: This address block is not writeable to DRAM Memory 1: This address block is writeable to DRAM Memory	0
9	Address Block C0000H−C3FFFH DRAM Read Control 0: This address block is not readable from DRAM Memory 1: This address block is readable from DRAM Memory	0
8	Address Block C4000H−C7FFFH Cacheable Control 0: This address block is not cacheable in the level 2 cache. 1: This address block is cacheable in the level 2 cache.	0
7	Address Block C4000H−C7FFFH DRAM Write Control 0: This address block is not writeable to DRAM Memory 1: This address block is writeable to DRAM Memory	0
6	Address Block C4000H−C7FFFH DRAM Read Control 0: This address block is not readable from DRAM Memory 1: This address block is readable from DRAM Memory	0
5	Address Block C8000H−CBFFFH Cacheable Control 0: This address block is not cacheable in the level 2 cache. 1: This address block is cacheable in the level 2 cache.	0
4	Address Block C8000H−CBFFFH DRAM Write Control 0: This address block is not writeable to DRAM Memory 1: This address block is writeable to DRAM Memory	0
3	Address Block C8000H−CBFFFH DRAM Read Control 0: This address block is not readable from DRAM Memory 1: This address block is readable from DRAM Memory	0
2	Address Block CC000H−CFFFFH Cacheable Control 0: This address block is not cacheable in the level 2 cache. 1: This address block is cacheable in the level 2 cache.	0
1	Address Block CC000H−CFFFFH DRAM Write Control 0: This address block is not writeable to DRAM Memory 1: This address block is writeable to DRAM Memory	0
0	Address Block CC000H−CFFFFH DRAM Read Control 0: This address block is not readable from DRAM Memory 1: This address block is readable from DRAM Memory	0

PCI Configuration Register 98: Memory Block 0 Control Register (Read/Write) — Bits 7:0 of the CONFIG_ADDRESS register=98H

Bit	Function	Default
31	Block 0 Non-Cacheable Control 0: Block 0 is cacheable in the level 2 cache 1: Block 0 is not cacheable in the level 2 cache	0
30:16	Ending Address of Memory Block 0 (with 32-KB granularity): A29, A28, A27, A26, A25, A24, A23, A22, A21, A20, A19, A18, A17, A16, A15	0000H
15	Block 0 Non-Local Control 0: Block 0 is contained in local memory 1: Block 0 is not contained in local memory (It resides on peripheral cards)	0
14:0	Starting Address of Memory Block 0 (with 32-KB granularity): A29, A28, A27, A26, A25, A24, A23, A22, A21, A20, A19, A18, A17, A16, A15	0000H

PCI Configuration Register 9C: Memory Block 1 Control Register (Read/Write) — Bits 7:0 of the CONFIG_ADDRESS register=9CH

Bit	Function	Default
31	Block 1 Control Bit Zero Bit 15 / Bit 31 / Function 0 / 0 / Block 1 Disabled 0 / 1 / Block 1 Non-Cacheable 1 / 0 / Block 1 is Non-Local 1 / 1 / Invalid	0
30:16	Ending Address of Memory Block 1 (with 32-KB granularity): A29, A28, A27, A26, A25, A24, A23, A22, A21, A20, A19, A18, A17, A16, A15	0000H
15	Block 1 Control Bit One See Bit 31 for functionality of this bit.	0
14:0	Starting Address of Memory Block 1 (with 32-KB granularity): A29, A28, A27, A26, A25, A24, A23, A22, A21, A20, A19, A18, A17, A16, A15	0000H

PCI Configuration Register A0: Cache Control Register (Read/Write) — Bits 7:0 of the CONFIG_ADDRESS register=A0H

Bit	Function	Default
31:26	Reserved	000000
25	PCI to Level 2 Cache Write Mode: 0: PCI writes to cache will operate with x-2-2-2 cycles. 1: PCI writes to cache will operate with x-1-1-1 cycles.	0
24	PCI to Level 2 Cache Read Mode: 0: PCI reads from cache will operate with x-2-2-2 cycles. 1: PCI reads from cache will operate with x-1-1-1 cycles.	0
23	Level 1 (CPU's Internal) Cache Mode: 0: Level 1 Cache is Write-Through 1: Level 1 Cache is Write-Back	0
22	Internal Tag SRAM Control: 0: Disable Internal Tag SRAM 1: Enable Internal Tag SRAM	0
21	Pipelined SRAM back-to-back cycle control: 0: Do not force a wait state in between back-to-back pipelined accesses. 1: Force a wait state in between back-to-back pipelined accesses. A wait state must be forced in between pipelined accesses if addresses are used to expand the depth of the cache when pipelined BSRAMs are used.	0

20	Reserved	0
19	Pseudo 2-Way Set, Way Miss Control: 0: Two extra wait states penalty for way miss (3/5-1-1-1; This bit is only used for two-way set systems with 1 Bank if 3-1-1-1 Reads or Writes are selected; See Bits 11:10 and 18:15) 1: Extra wait state penalty for way miss (3/4-1-1-1; This bit is only used for two-way set systems with 1 Bank if 3-1-1-1 Reads or Writes are selected; See Bits 11:10 and 18:15)	0
18:17	Cache Read Control: 00: 4-2-2-2 read cycles 01: 4-1-1-1 read cycles 10: 3-2-2-2 read cycles 11: 3-1-1-1 read cycles	00
16:15	Cache Write Control: 00: 4-2-2-2 write cycles 01: 4-1-1-1 write cycles 10: 3-2-2-2 write cycles 11: 3-1-1-1 write cycles	00
14	Level 2 Cache Mode: 0: Level 2 Cache is Write-Through 1: Level 2 Cache is Write-Back	0
13	Level 2 Cache Bank B Control: 0: Bank B Contains Synchronous, Pipelined Burst SRAMs 1: Bank B Contains Synchronous, Flow-through Burst SRAMs	0
12	Level 2 Cache Bank A Control: 0: Bank A Contains Synchronous, Pipelined Burst SRAMs 1: Bank A Contains Synchronous, Flow-through Burst SRAMs	0
11:10	Level 2 Cache Type Control: 00: Level 2 Cache Disabled 01: Direct-Mapped 10: Two-Way Set with 2 Banks 11: Two-Way Set with 1 Bank	00
9	Level 2 Cache Dirty Bit Control: 0: Dirty Bit is not used; cacheable range is doubled; All cache lines are assumed dirty 1: Dirty Bit is used	0
8	Level 2 Cache Sectoring Control: 0: Cache tag is not sectored (One level 1 cache line maps to one level 2 cache line) 1: Cache tag is sectored (Two level 1 cache lines map to one level 2 cache line: Level 2 Line size is effectively doubled: This mode must be used for cache sizes larger than 512 KB)	1
7:5	Level 2 Cache Bank B Size Control (This Range is ignored if level 2 cache is chosen to be Direct-Mapped or Single-Bank, 2-Way Set Associative): 000: Reserved 001: Reserved 010: Reserved 011: 64 KBytes 100: 128 KBytes 101: 256 KBytes 110: 512 KBytes 111: Invalid	111
4:2	Level 2 Cache Bank A Size Control : 000: Reserved 001: Reserved 010: Reserved 011: 64 KBytes 100: 128 KBytes 101: 256 KBytes 110: 512 KBytes 111: 1 MBytes (1 MByte bank size is only valid for Direct-Mapped or Single-bank, 2-Way Set Associative Level 2 Cache configurations)	111

1	Level 2 Cache Bank Test Control: 0: When Cache is organized as two-way set associative and the cache is in test mode, force a hit in bank A. 1: When Cache is organized as two-way set associative and the cache is in test mode, force a hit in bank B.	0
0	Level 2 Cache Test Control: 0: Level 2 Cache is in Normal Operating Mode 1: Level 2 Cache is in Test Mode In Cache Test Mode, any CPU access with address between 100000H and 200000H will force a cache hit.	0

PCI Configuration Register A8: System DRAM Memory Control Register (Read/Write) — Bits 7:0 of the CONFIG_ADDRESS register=A8H

Bit	Function	Default
31	VUMA control 0: VUMA interface disabled 1: VUMA interface enabled	0
30	Access Above Physical DRAM Memory Cacheability Control: 0: Memory Accesses Outside of Physical Memory Range Not Cached 1: Memory Accesses Outside of Physical Memory Range Cached	0
29:28	DRAM Write Enable ($\overline{DWE}$) and MA[11:0] Drive Strength: 00: 20 mA 01: 12 mA 10: 8 mA 11: Reserved	00
27:26	DRAM Column Address Strobe ($\overline{CAS}$) Drive Strength: 00: 20 mA 01: 12 mA 10: 8 mA 11: Reserved	00
25	CPU to DRAM Post-Write Buffer Control: 0: Disable CPU-to-DRAM Post-Write Buffers 1: Enable CPU-to-DRAM Post-Write Buffers	0
24	CPU Type: 0: Intel/AMD CPU 1: Cyrix CPU	0
23	DRAM Parity Error NMI Control: 0: Disable Error Reporting Through the NMI signal 1: Enable Error Reporting Through the NMI signal	0
22	$\overline{CAS}$ PCI-to-DRAM Precharge Control: 0: 3 CPU clock cycles of $\overline{CAS}$ precharge for PCI-to-DRAM Accesses 1: 2 CPU clock cycle of $\overline{CAS}$ precharge for PCI-to-DRAM Accesses	0
21:19	DRAM Refresh Request Rate Control (for 256 Rows): 000: Disable DRAM Refresh (Do NOT Use in Normal Operation) 001: Reserved 010: Reserved 011: Reserved 100: 4 ms 101: 16 ms 110: 64 ms 111: 128 ms	000
18	EDO DRAM Autodetection Control: 0: Disable EDO DRAM Autodetection 1: Enable EDO DRAM Autodetection	0

17	DRAM Buffer Wait State Control: 0: 1 CPU clock cycle wait state for write data through the DRAM buffers 1: 0 CPU clock cycle wait states for write data through the DRAM buffers	0
16:15	DRAM Refresh $\overline{RAS}$ Assertion Time Control: 00: 6 CPU clock cycles of $\overline{RAS}$ assertion on a DRAM refresh 01: 5 CPU clock cycles of $\overline{RAS}$ assertion on a DRAM refresh 10: 4 CPU clock cycles of $\overline{RAS}$ assertion on a DRAM refresh 11: 3 CPU clock cycles of $\overline{RAS}$ assertion on a DRAM refresh	00
14	Row Address Set-up Control: 0: 2 CPU clock cycles of row address set-up 1: 1 CPU clock cycle of row address set-up	0
13	Page Decode Time Control: 0: 2 CPU clock cycles for page decoding 1: 1 CPU clock cycle for page decoding	0
12	Write Data Setup to $\overline{CAS}$ Time Control: 0: 1 CPU clock cycle of write data set-up to $\overline{CAS}$ 1: 0 CPU clock cycles of write data set-up to $\overline{CAS}$	0
11:10	$\overline{RAS}$ to $\overline{CAS}$ Delay Control: 00: 4 CPU clock cycles of $\overline{RAS}$ to $\overline{CAS}$ delay 01: 3 CPU clock cycles of $\overline{RAS}$ to $\overline{CAS}$ delay 10: 2 CPU clock cycles of $\overline{RAS}$ to $\overline{CAS}$ delay 11: Reserved	00
9:8	$\overline{RAS}$ Precharge Control: 00: 5 CPU clock cycles of $\overline{RAS}$ precharge 01: 4 CPU clock cycles of $\overline{RAS}$ precharge 10: 3 CPU clock cycles of $\overline{RAS}$ precharge 11: 2 CPU clock cycles of $\overline{RAS}$ precharge	00
7	$\overline{CAS}$ EDO DRAM Precharge Control 0 2 CPU clock cycles of $\overline{CAS}$ precharge 1 1 CPU clock cycles of $\overline{CAS}$ precharge	0
6	Reserved	0
5:4	$\overline{CAS}$ EDO DRAM Read Width Control: 00: 3 CPU clock cycles of $\overline{CAS}$ width on a read 01: 2 CPU clock cycles of $\overline{CAS}$ width on a read 10: 1 CPU clock cycle of $\overline{CAS}$ width on a read 11: Reserved	00
3	$\overline{CAS}$ Fast Page Mode DRAM Precharge Control: 0: 2 CPU clock cycles of $\overline{CAS}$ precharge 1: 1 CPU clock cycle of $\overline{CAS}$ precharge	0
2	$\overline{CAS}$ Fast Page Mode DRAM Write Width Control: 0: 2 CPU clock cycles of $\overline{CAS}$ width on a write 1: 1 CPU clock cycle of $\overline{CAS}$ width on a write	0
1:0	$\overline{CAS}$ Fast Page Mode DRAM Read Width Control: 00: 3 CPU clock cycles of $\overline{CAS}$ width on a read 01: 2 CPU clock cycles of $\overline{CAS}$ width on a read 10: Reserved 11: Reserved	00

PCI Configuration Register B0: CPU to PCI Control Register (Read/Write) — Bits 7:0 of the CONFIG_ADDRESS register=B0H

Bit	Function	Default
31:29	PCI Retry Attempts Control: 000: Retry until transaction is successful 001: 6 Retries 010: 5 Retries 011: 4 Retries 100: 3 Retries 101: 2 Retries 110: 1 Retry 111: Retry Disabled	000
28:27	$\overline{\text{DEVSEL}}$ Latency Timer: 00: Timeout and Abort After 7 PCI Clocks with no $\overline{\text{DEVSEL}}$ returned 01: Timeout and Abort After 6 PCI Clocks with no $\overline{\text{DEVSEL}}$ returned 10: Timeout and Abort After 5 PCI Clocks with no $\overline{\text{DEVSEL}}$ returned 11: Timeout and Abort After 4 PCI Clocks with no $\overline{\text{DEVSEL}}$ returned	00
26:25	Reserved	00
24	Reserved	0
23	Reserved	0
22	Target Abort Control: 0: Disable Target Abort 1: Enable Target Abort	0
21	Initiator (Master) Abort Control: 0: Disable Initiator Abort 1: Enable Initiator Abort	0
20	Parity Check Control: 0: Disable PCI Parity Checking for Read Data 1: Enable PCI Parity Checking for Read Data	0
19	Reserved	0
18	Reserved	0
17	PCI I/O Write Data Wait State Control: 0: One Additional I/O Write Data Wait State Inserted 1: No Additional I/O Write Data Wait States Inserted	0
16	PCI Memory Write Data Wait State Control: 0: One Additional Memory Write Data Wait State Inserted 1: No Additional Memory Write Data Wait States Inserted	0
15	Reserved	0
14	PCI Read Data Wait State Control: 0: One Additional Read Data Wait State Inserted 1: No Additional Read Data Wait States Inserted	0
13	Address Setup Wait State Control: 0: One Additional Address Setup Wait State Inserted 1: No Additional Address Setup Wait States Inserted	0
12	Reserved	0
11	CPU to PCI Idle Control: 0: When CPU to PCI is Idle, Float drivers off of the PCI bus 1: When CPU to PCI is Idle, Drive onto the PCI bus	0
10	Special Cycle Control: 0: Normal Operation 1: Force PCI Special Cycle	0
9:6	Reserved	0000

5	CPU to 692 Read Transfer Control: 0: One Wait State is inserted 1: No Wait States are inserted	0
4	Reserved	0
3	CPU to 692 Post-Write Transfer Control: 0: One Wait State is inserted 1: No Wait States are inserted	0
2	CPU to PCI Post-Write Control: 0: Disable Post-Write buffers 1: Enable Post-Write buffers	0
1	Pipeline Dead Cycle Control: 0: Force Wait States for Dead Cycles 1: Will not Force Wait States for Dead Cycles	0
0	Address Decode Control: 0: Will add one Additional Wait State for Address Decode 1: Will not add Additional Wait States for Address Decode	0

PCI Configuration Register B4: PCI Master Control Register (Read/Write) — Bits 7:0 of the CONFIG_ADDRESS register=B4H

Bit	Function	Default
31:14	Reserved	000000
13	0: Disable SMM memory (all access to SMM memory goes to PCI bus) 1: Enable SMM memory	0
12	0: Enable CPU to initialize the SMM memory when Bit[13]=1 1: Disable CPU from initialize the SMM memory. This is a sticky bit and is sticked to 1	0
11	0: Forward all CPU cycles with address A0000h−BFFFFh to DRAM 1: Forward all CPU cycles with address A0000h−BFFFFh to DRAM, except CPU data cycle which goes to PCI	0
10	0: Disable 1: Enable dpfreqackn test mode (drive on bmerge)	0
9	0: Disable 1: Enable dpgntbsyn test mode (drive on bmerge)	0
8	Reserved, and must be kept at 0	0
7	Reserved	0
6	0: Enable caching E00000h−FFFFFFh (15M−16M hole) 1: Disable caching E00000h−FFFFFFh (15M−16M hole)	0
5	0: Enable E00000h−FFFFFFh (15M−16M hole) as local memory 1: Disable E00000h−FFFFFFh (15M−16M hole) as local memory (cycles redirect to PCI bus)	0
4	0: Enable caching 80000h−9FFFFh (512k−640k hole) 1: Disable caching 80000h−9FFFFh (512k−640k hole)	0
3	0: Enable 80000h−9FFFFh (512k−640k hole) as local memory 1: Disable 80000h−9FFFFh (512k−640k hole) as local memory (cycles redirect to PCI bus)	0
2	Reserved	0
1	Shared DRAM (VUMA) Control: 0: Disable VUMA 1: Enable VUMA	0
0	Write Burst Enable for CPU-to-PCI FIFO Control: 0: Disable Write Burst 1: Enable Write Burst	0

PCI Configuration Register B8: PCI Slave Control Register (Read/Write) — Bits 7:0 of the CONFIG_ADDRESS register=B8H

Bit	Function	Default
31:25	Reserved	0000000
24	High Doubleword Transfer from 691 to 692 Control during PCI write to L2 cache: 0: One Wait State is inserted 1: No Wait States are inserted	0
23	PCI to L2 cache read data transfer from C692 to C691 control: 0: One Wait State is inserted 1: No Wait States are inserted	0
22	PCI to Cache Memory Burst Write Control: 0: Enable Burst Write 1: Disable Burst Write	0
21	Cache Write Low Doubleword (Transfer from 691 to the 692) Wait State Control: 0: One Wait State is inserted 1: No Wait States are inserted	0
20	DRAM Read High Double Word Wait State Control: 0: One Wait State is inserted 1: No Wait States are inserted	0
19	DRAM Write High Double Word Wait State Control: 0: One Wait State is inserted 1: No Wait States are inserted	0
18	DRAM Write Low Double Word Wait State Control: 0: One Wait State is inserted 1: No Wait States are inserted	0
17:16	Reserved	00
15	Target Pre-Read Control: 0: Disable Target Pre-Read 1: Enable Target Pre-Read	0
14	Target Burst Read Control: 0: Disable Target Burst Read 1: Enable Target Burst Read	0
13	Target 0 Wait State Read Control: 0: Disable Zero Wait State Target Reads 1: Enable Zero Wait State Target Reads	0
12	Target Burst Write Control: 0: Disable Target Burst Write 1: Enable Target Burst Write	0
11	Target 0 Wait State Write Control: 0: Disable Zero Wait State Target Writes 1: Enable Zero Wait State Target Writes	0
10	Target $\overline{\text{PERR}}$ and $\overline{\text{SERR}}$ Generation Control: 0: Disable Target $\overline{\text{PERR}}$ and $\overline{\text{SERR}}$ Generation 1: Enable Target $\overline{\text{PERR}}$ and $\overline{\text{SERR}}$ Generation	0
9	Target Lock Control: 0: Disable Target Lock 1: Enable Target Lock	0
8	Target Delayed Read Control: 0: Disable Target Delayed Read 1: Enable Target Delayed Read	0

7:6	Target Flush After Delayed Read Retry Cycle Control: 00: Flush Data After 1 Retry 01: Flush Data After 4 Retries 10: Flush Data After 8 Retries 11: Never Flush Data Until Transaction Is Completed.	00
5:4	Address Space Compare Size Boundary Control: 00: 64 KBytes 01: 32 KBytes 10: 256 KBytes 11: 1 MByte	00
3:2	Subsequent Data Transfer Latency Control: 00: Disabled 01: Retry On 8th PCI Clock 10: Retry On 16th PCI Clock 11: Retry On 32nd PCI Clock	00
1:0	Initial Data Transfer Latency Control: 00: Disabled 01: Retry On 16th PCI Clock 10: Retry On 32nd PCI Clock 11: Retry On 64th PCI Clock	00

PCI Configuration Register BC: Reserved for CY82C691(Read Only) — Bits 7:0 of the CONFIG_ADDRESS register=BCH

Bit	Function	Default
31:26	Reserved	XXXXXX
25:0	Reserved	000000H

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage (V_{CC}) ..... +7 V

Ambient Operating Temperature ..... −25°C to +70°C

Ambient Storage Temperature ..... −40°C to 125°C

DC Voltage Applied to Outputs ..... −0.5V to V_{DD}

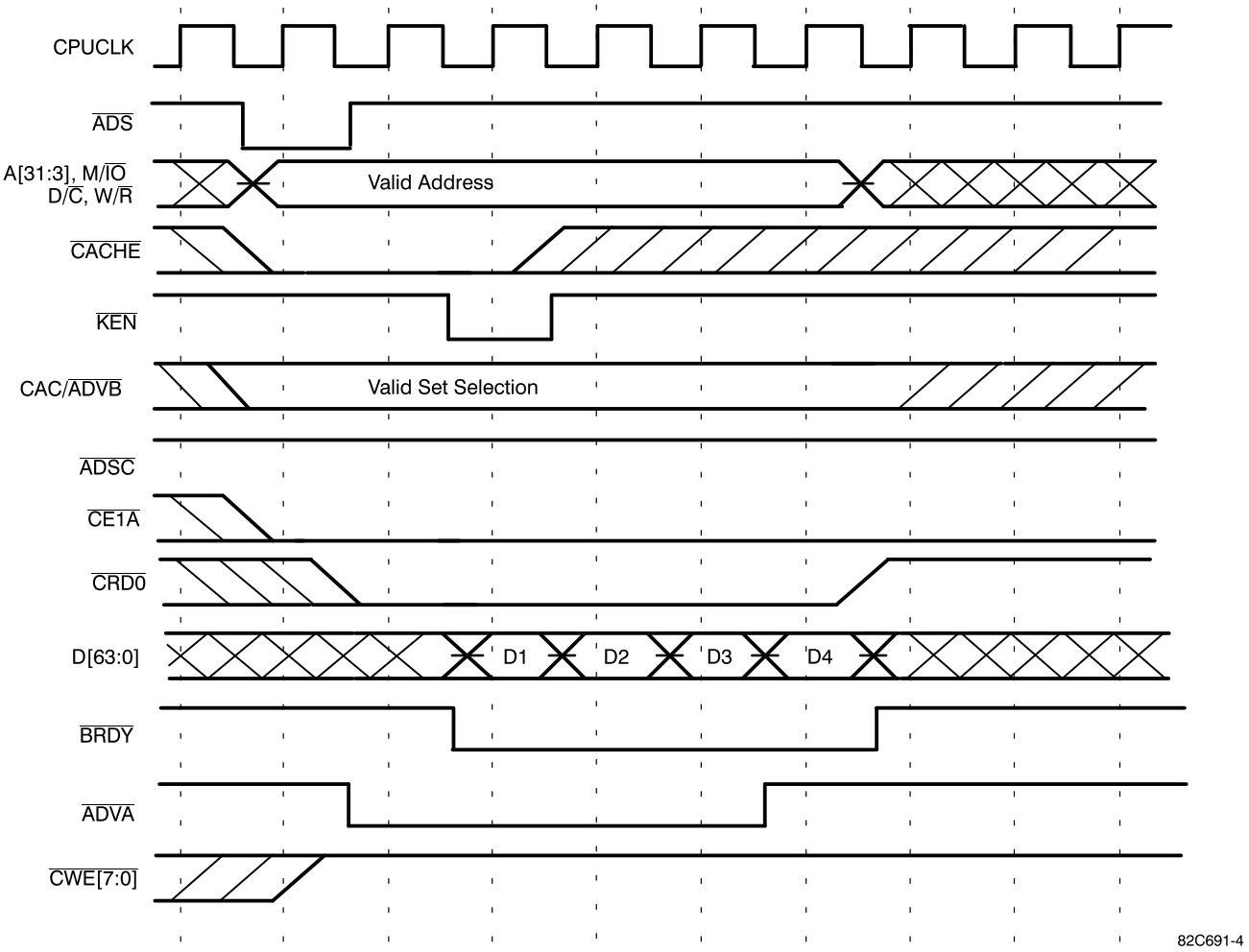
DC Input Voltage ..... −0.5V to V_{DD}

Electrical Characteristics Over the Operating Range (T_A=0°C to 70°C)

Parameter	Description		Min.	Max.	Unit
V_{CC}	Core Supply Voltage		4.5	5.5	V
V_{DD}	3.3V I/O Supply Voltage		3.0	Vcc	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD}+0.5	V
V_{OL}	Output LOW Voltage			0.4	V
V_{OH3}	Output HIGH Voltage (3.3V Outputs)		2.4	V_{OUT}+0.3	V
V_{OH5}	Output HIGH Voltage (5V Outputs)		2.4	V_{CC}+0.5	V
I_{IL}	Input Leakage Current			10	µA
I_{OL}	Output Leakage			10	µA
C_{IN}	Input Capacitance			10	pF
C_{OUT}	Output Capacitance			10	pF
I_{CC}	Power Supply Current	66 MHz		TBD	mA

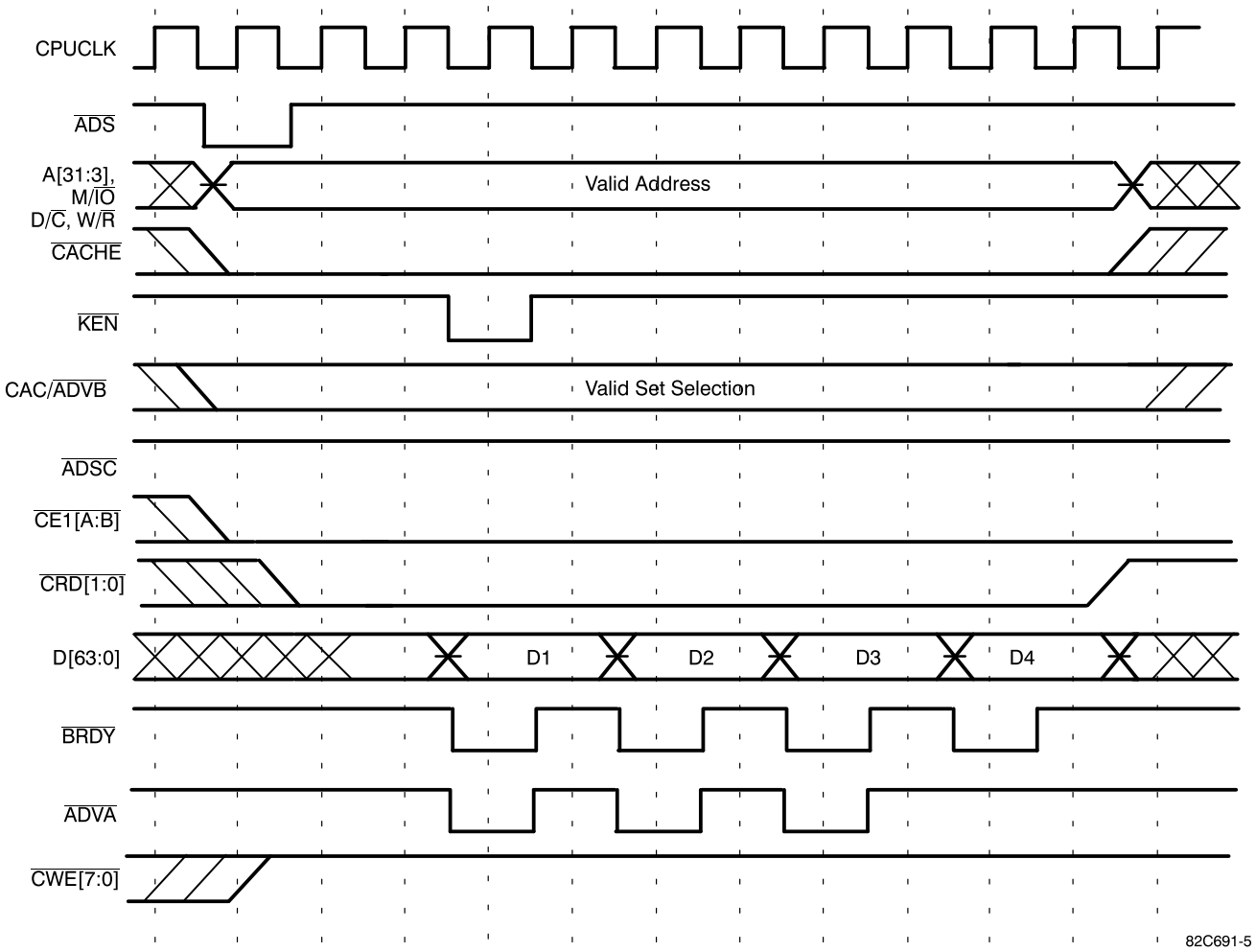
Switching Waveforms

Pipelined Cache Read (Two-way Set, Bank Hit or Direct -mapped)



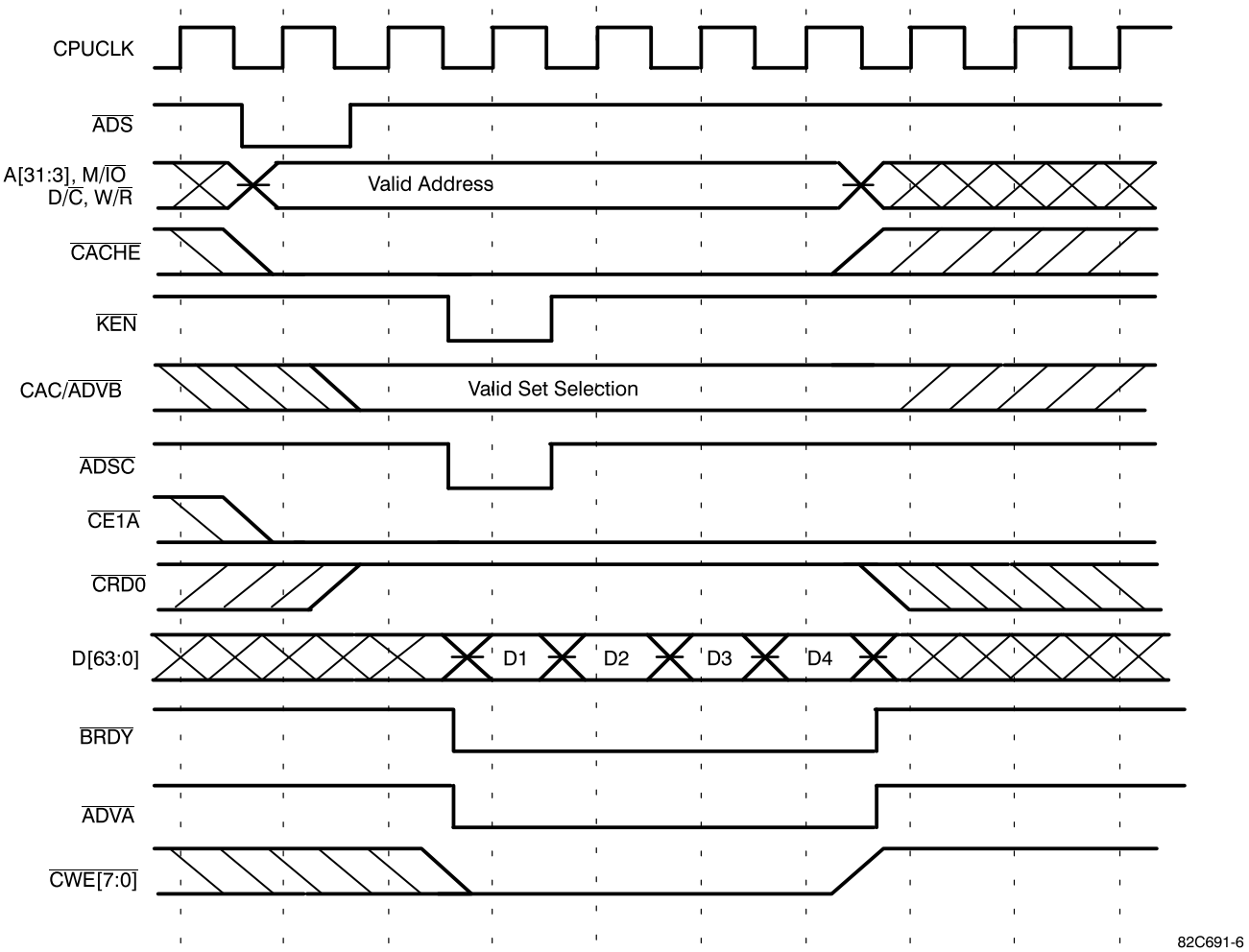
Switching Waveforms (continued)

Pipelined Cache Read (2-way set, bank hit,4-2-2-2 Programmed Operation)



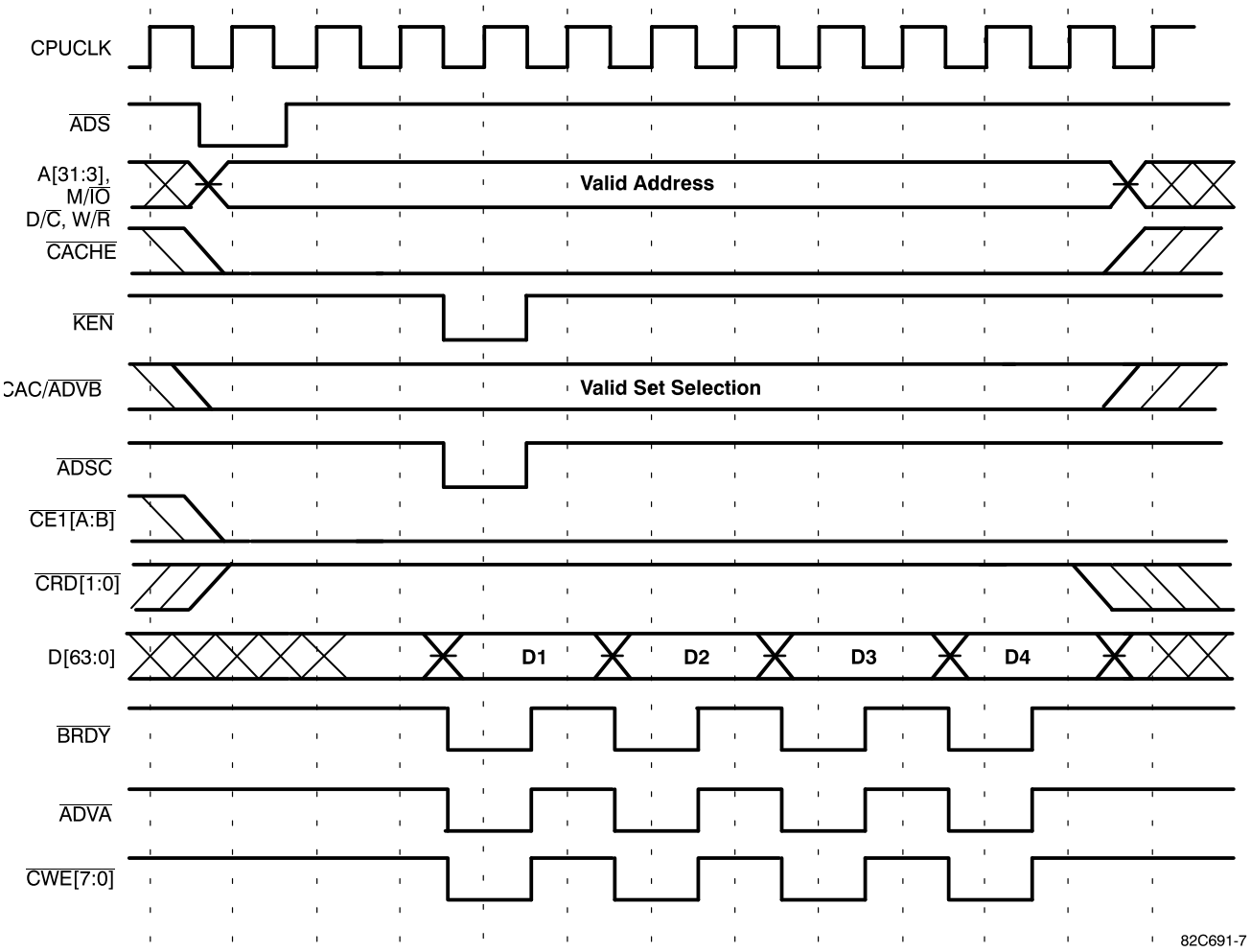
Switching Waveforms (continued)

Cache Line Write (1 Bank)



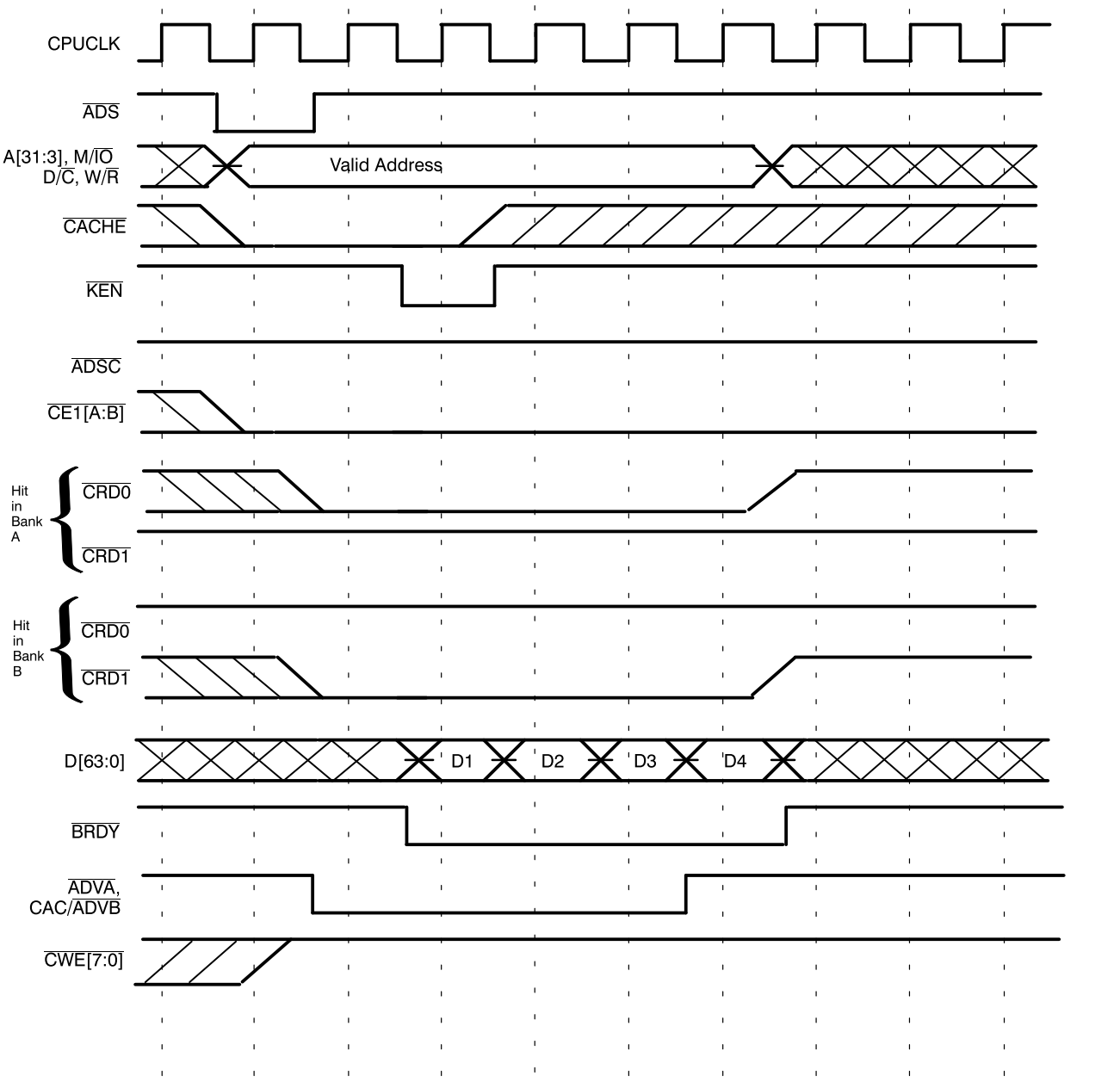
Switching Waveforms (continued)

Line Write (1 Bank,4-2-2-2 Programmed Operation)



Switching Waveforms (continued)

Pipelined Cache Read (2-way set, 2 Banks)



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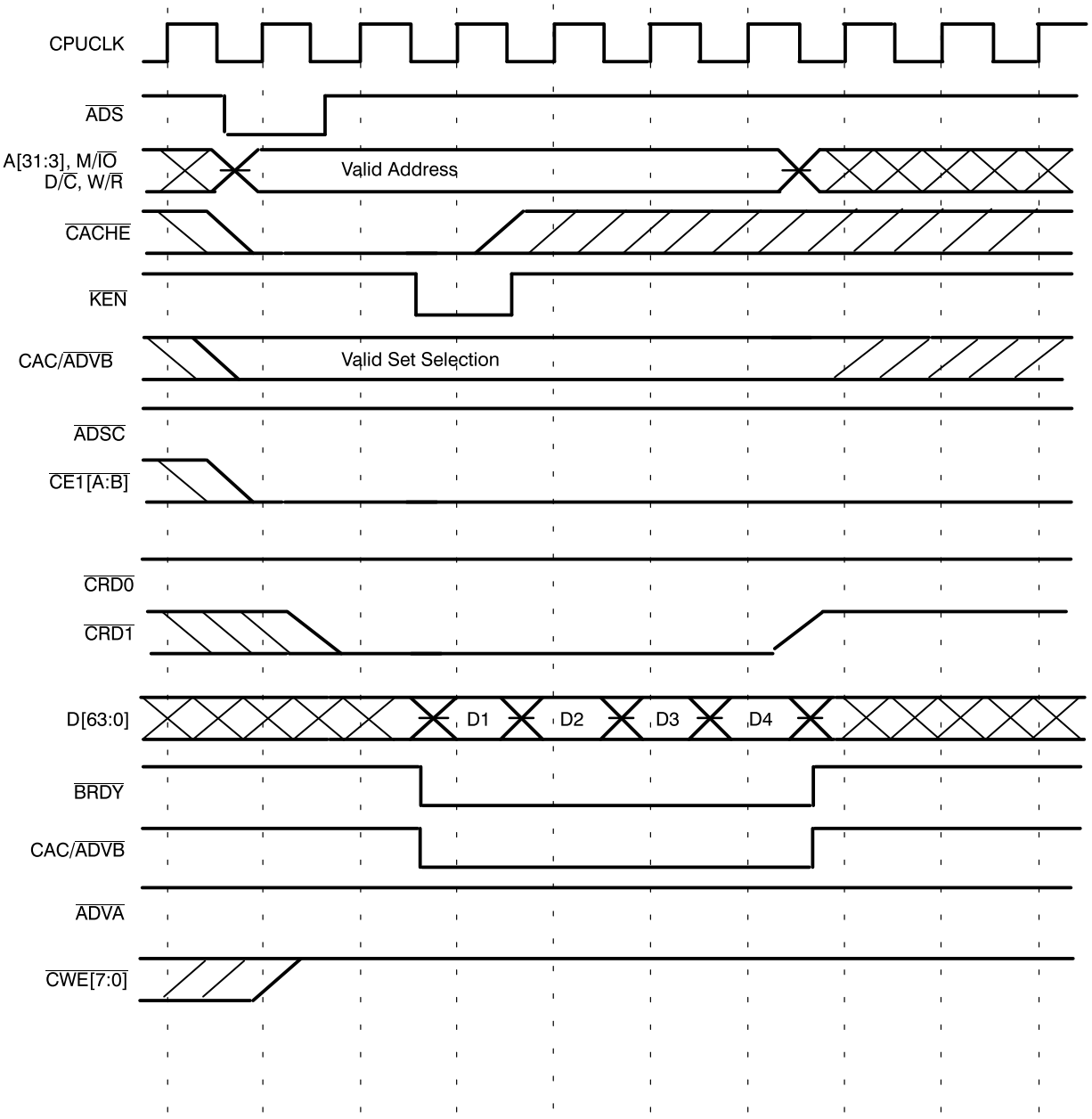
Switching Waveforms (continued)

CPU Cache Read (2 Banks, Bank 2 Contains Synchronous Flow-through RAMs, Hit in Bank 2)



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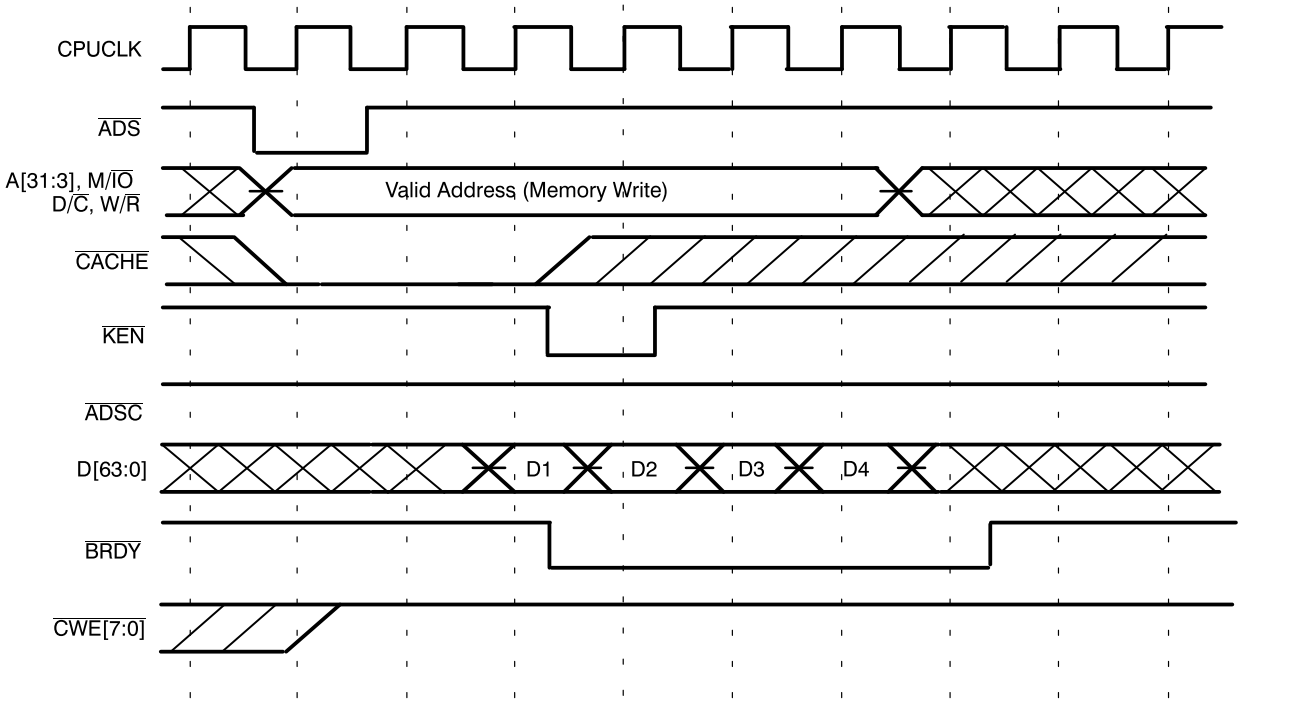
Switching Waveforms (continued)

CPU Memory Write to Post Write Buffer (Destination PCI or DRAM)



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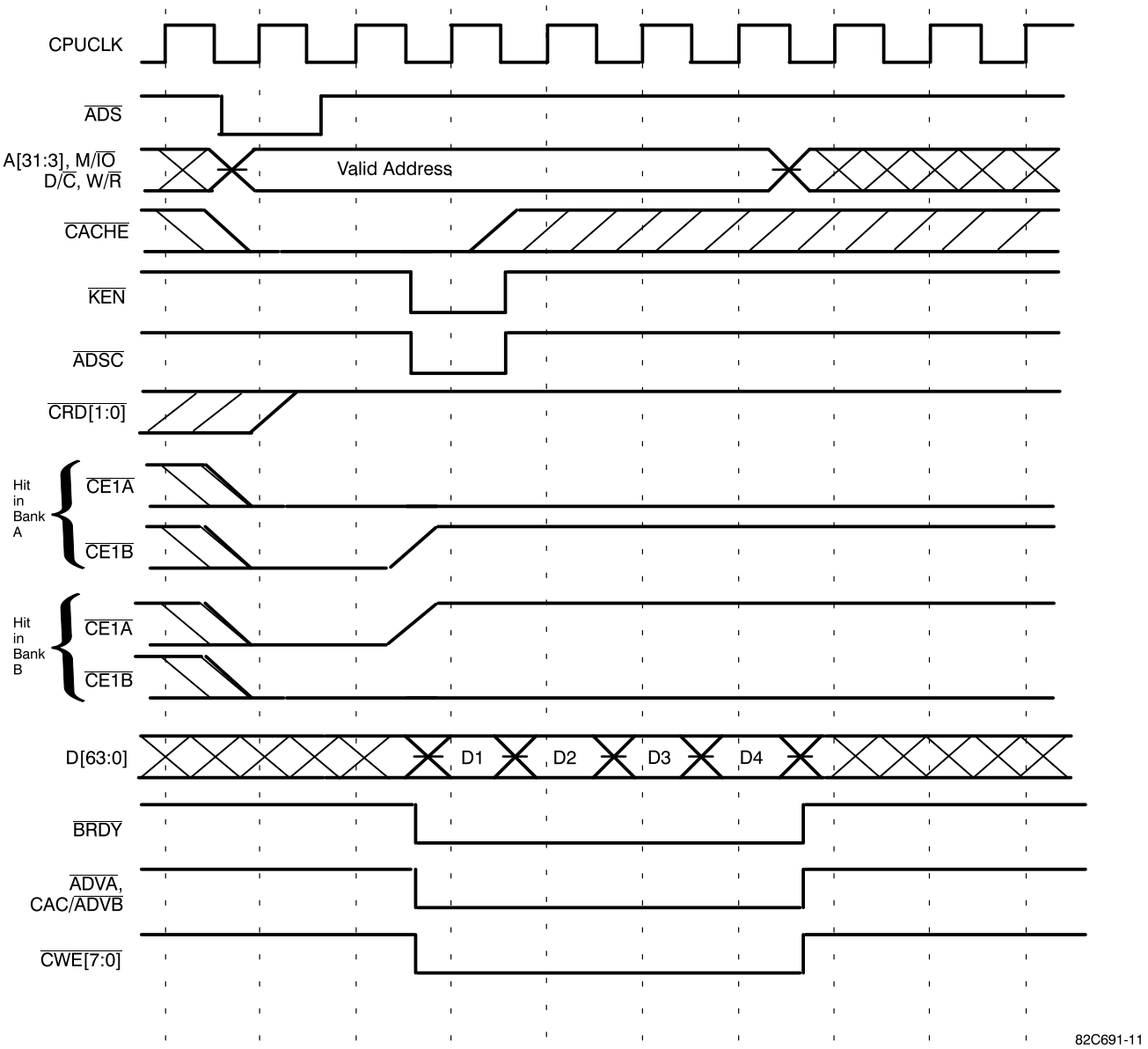
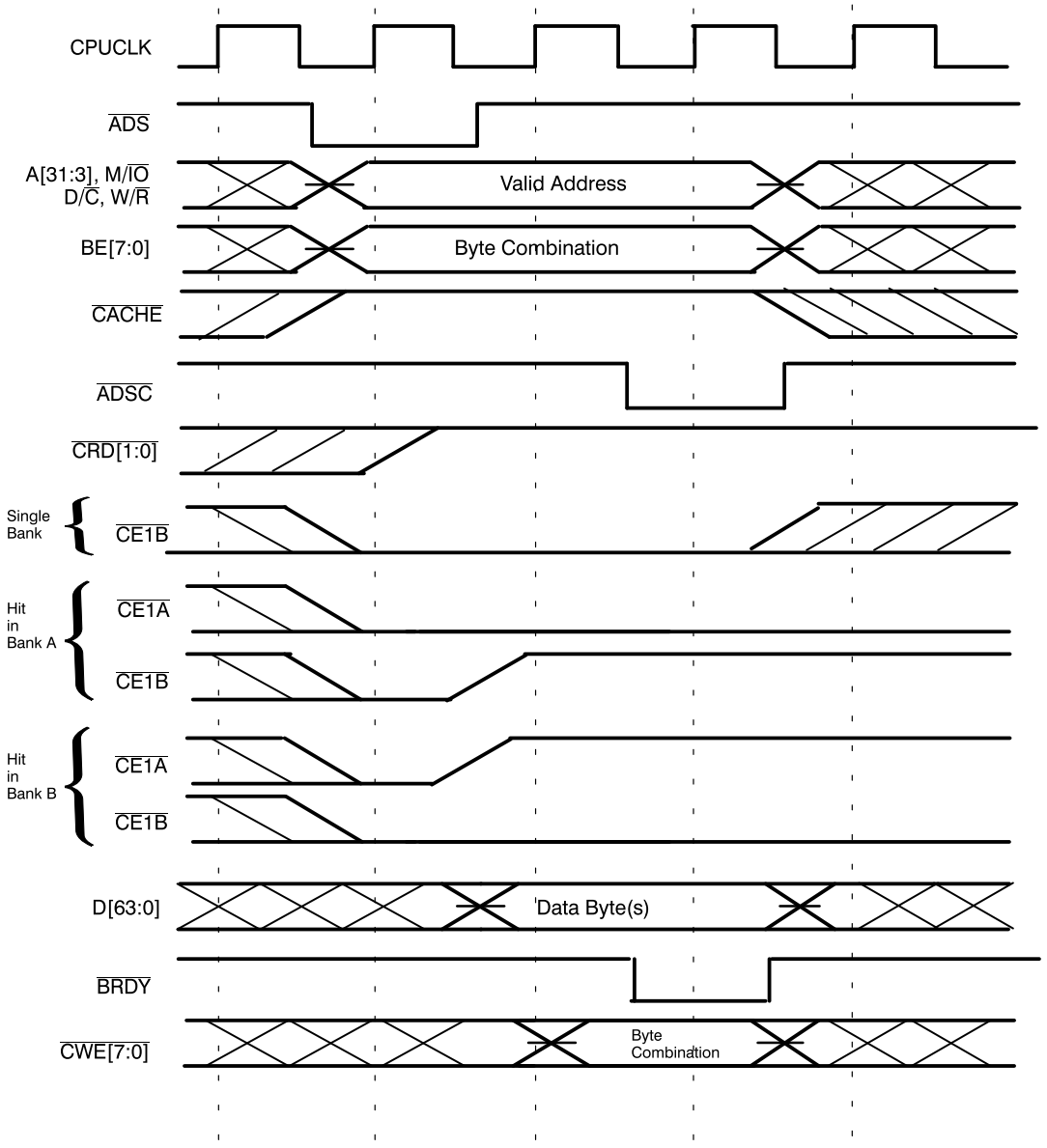
Switching Waveforms (continued)

Cache Line Write (2 Banks)



Switching Waveforms (continued)

CPU Cache Byte Write



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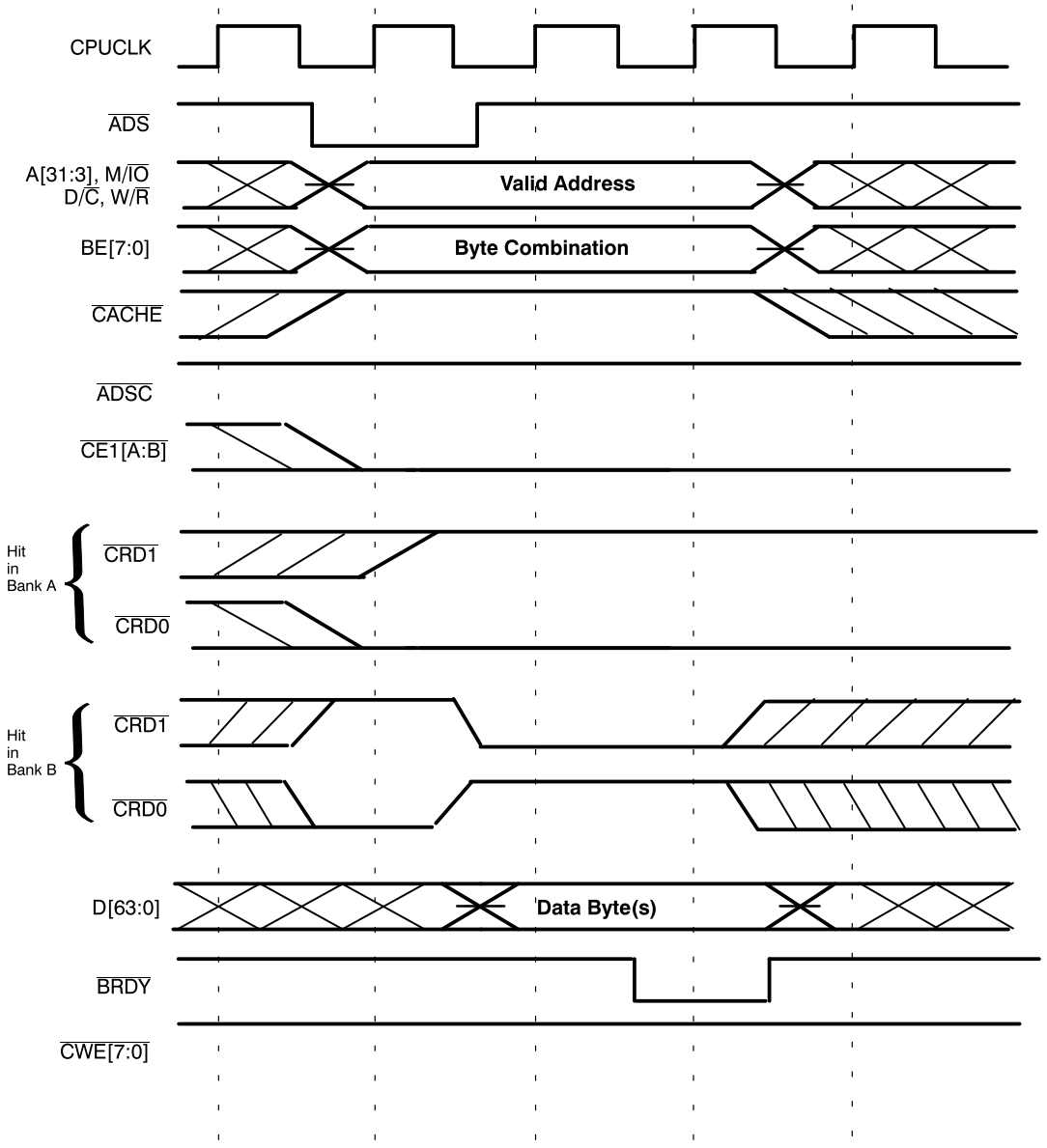
Switching Waveforms (continued)

CPU Cache Single (Non-burst) Read



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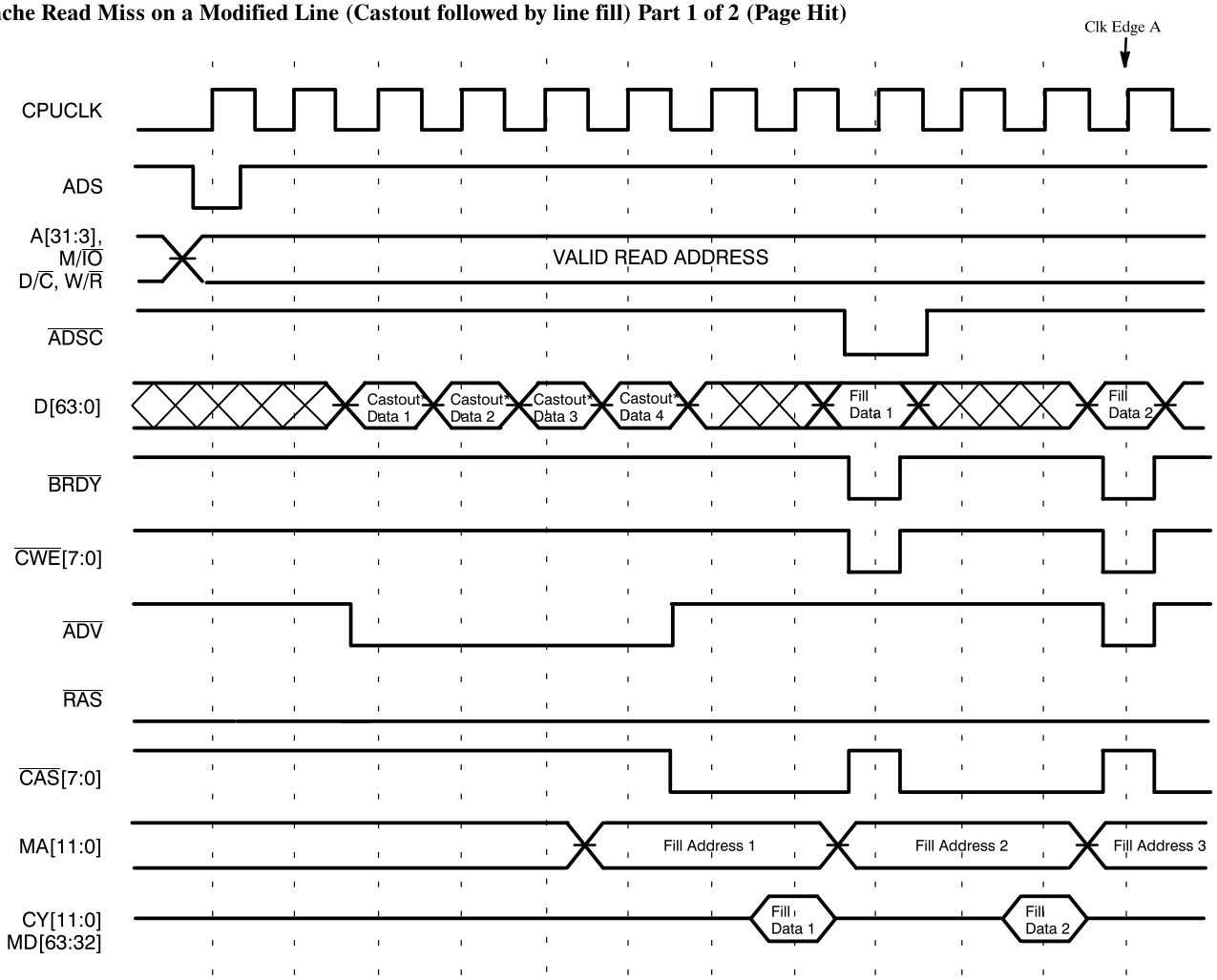
Switching Characteristics
Switching Waveforms (continued)

Cache Read Miss on a Modified Line (Castout followed by line fill) Part 1 of 2 (Page Hit)

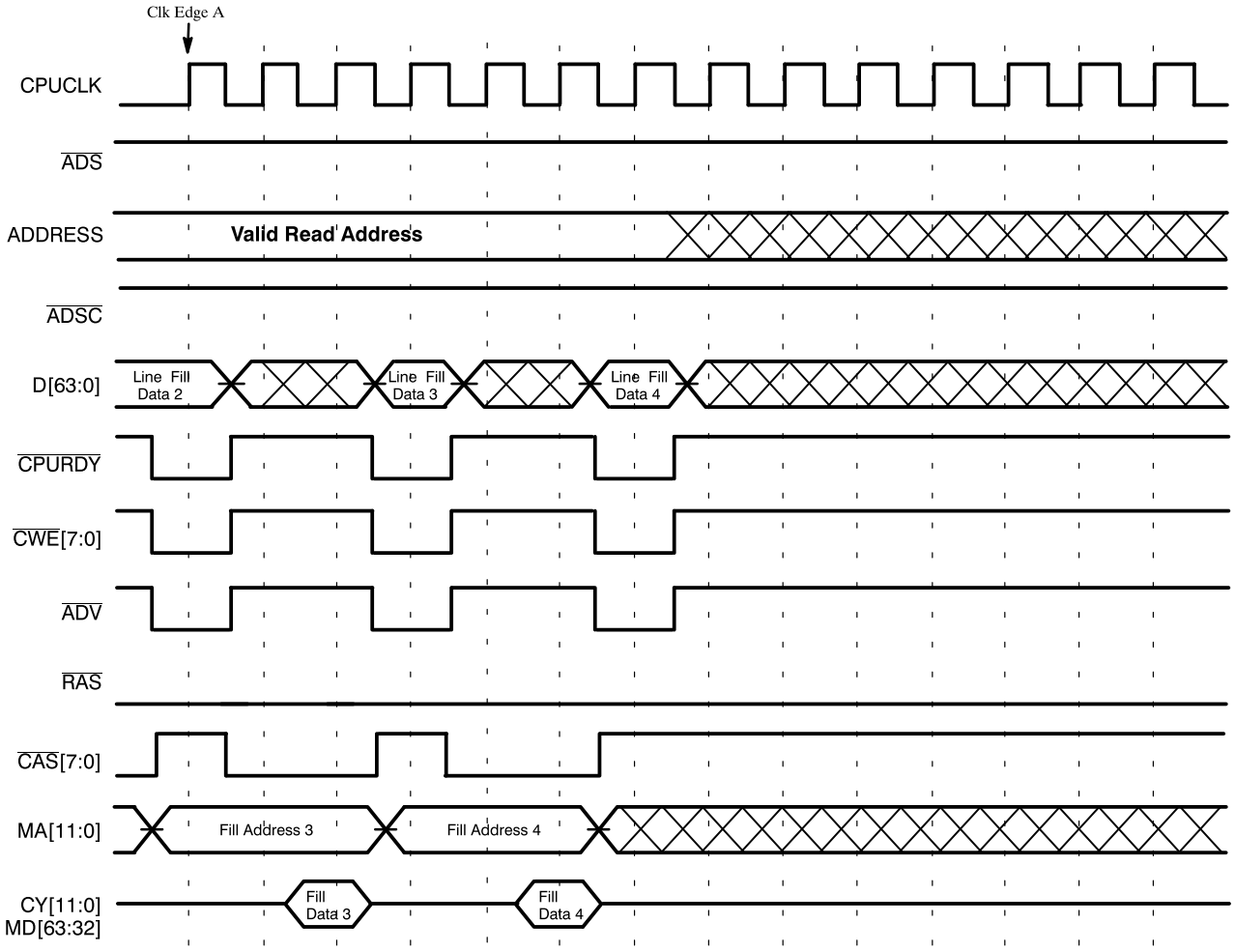


* Note: The castout data is written into DRAM FIFOS.

Switching Characteristics

Switching Waveforms (continued)

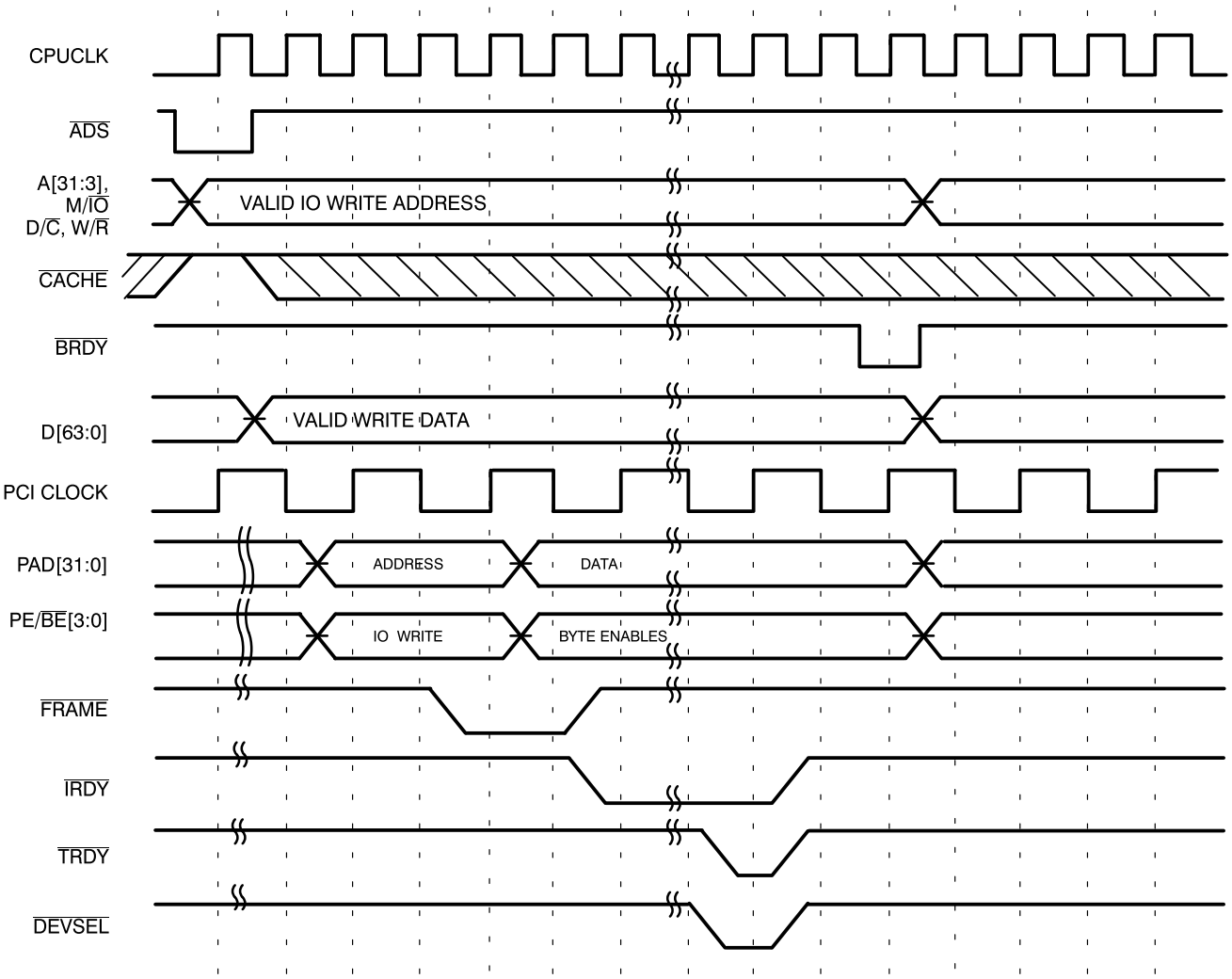
Cache Read Miss on a Modified Line (Page Hit) Part 2 of 2



Switching Characteristics

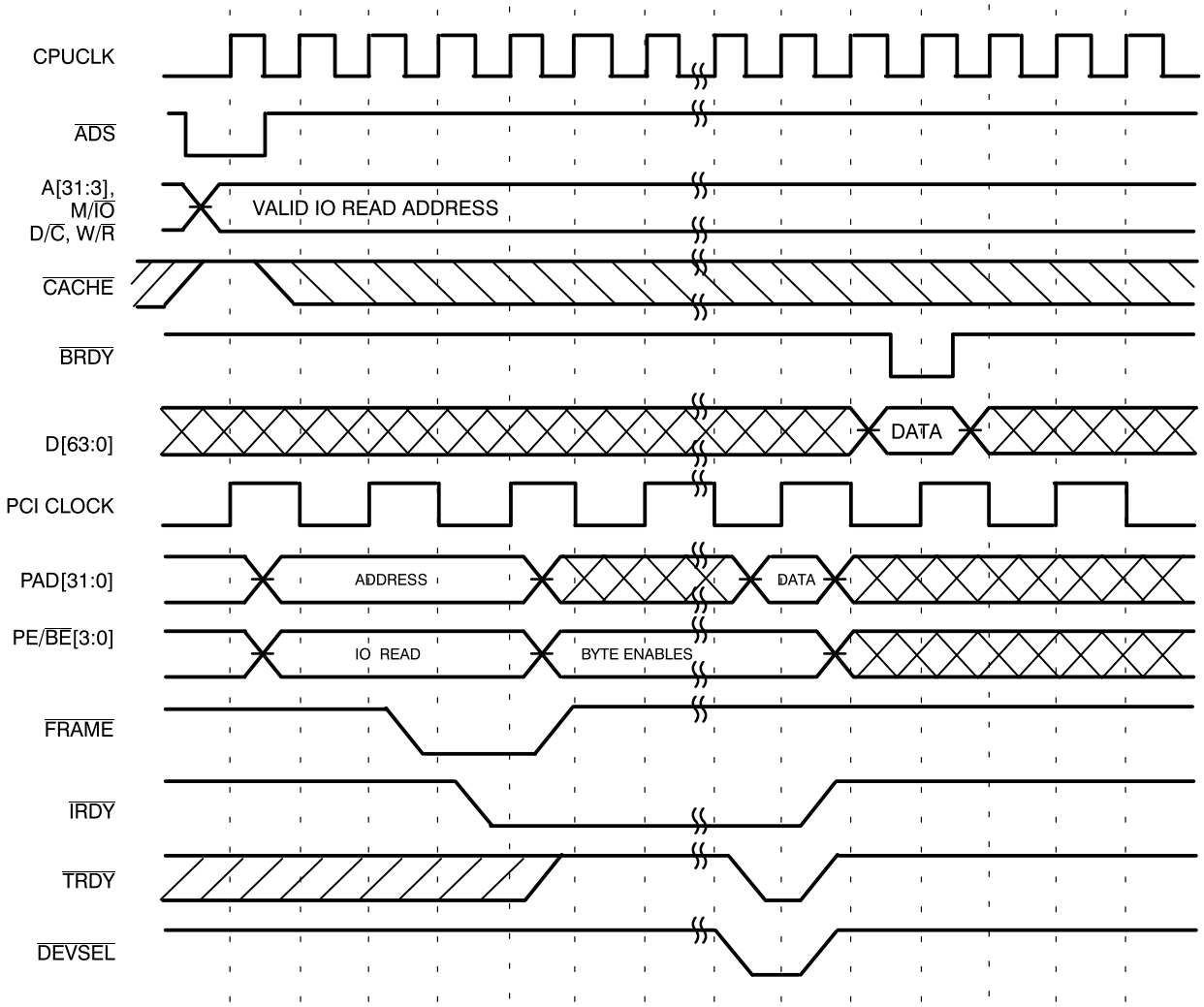
Switching Waveforms (continued)

IO Write to PCI Slave



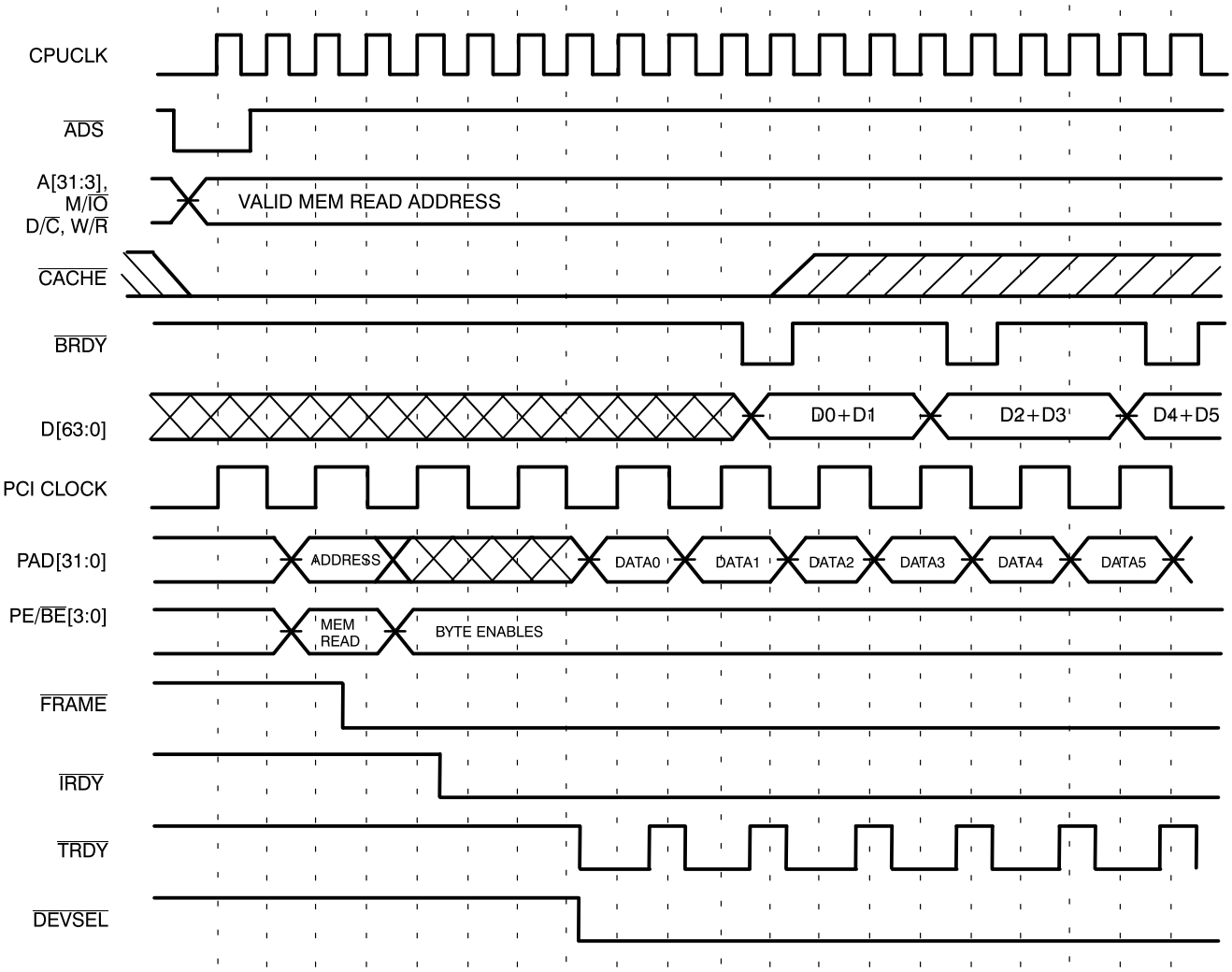
Switching Waveforms (continued)

IO Read from PCI Slave



Switching Waveforms (continued)

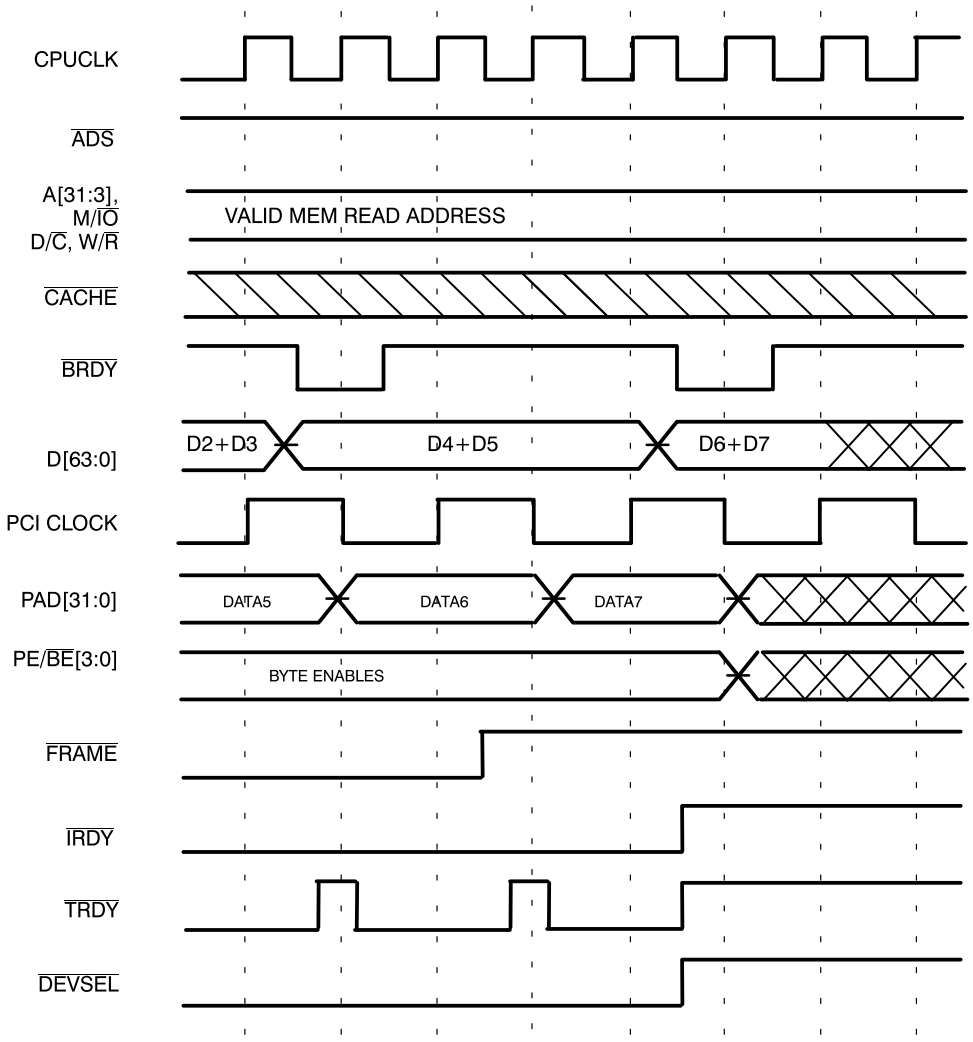
Memory Read (Cache Line Fill) from PCI Slave (Part 1 of 2)



Switching Characteristics

Switching Waveforms (continued)

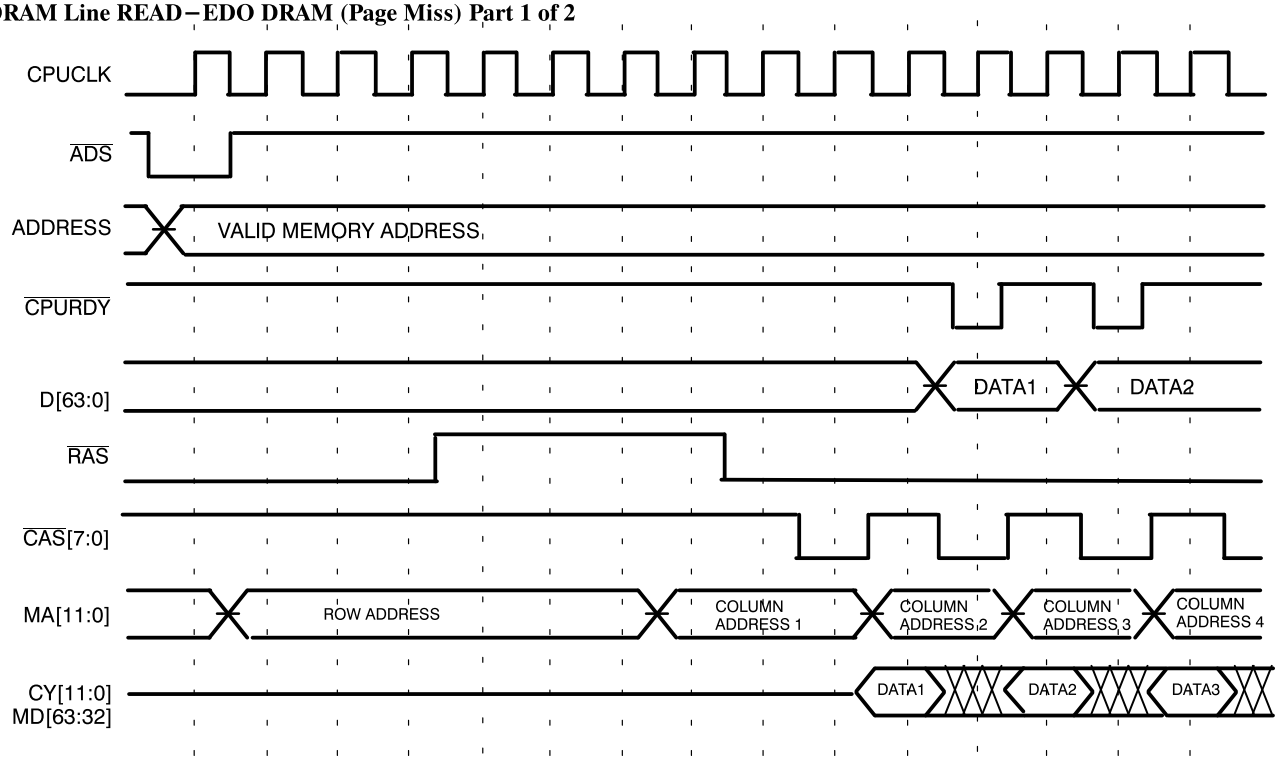
Memory Read (Cache Line Fill) Form PCI Slave (Part 2 of 2)



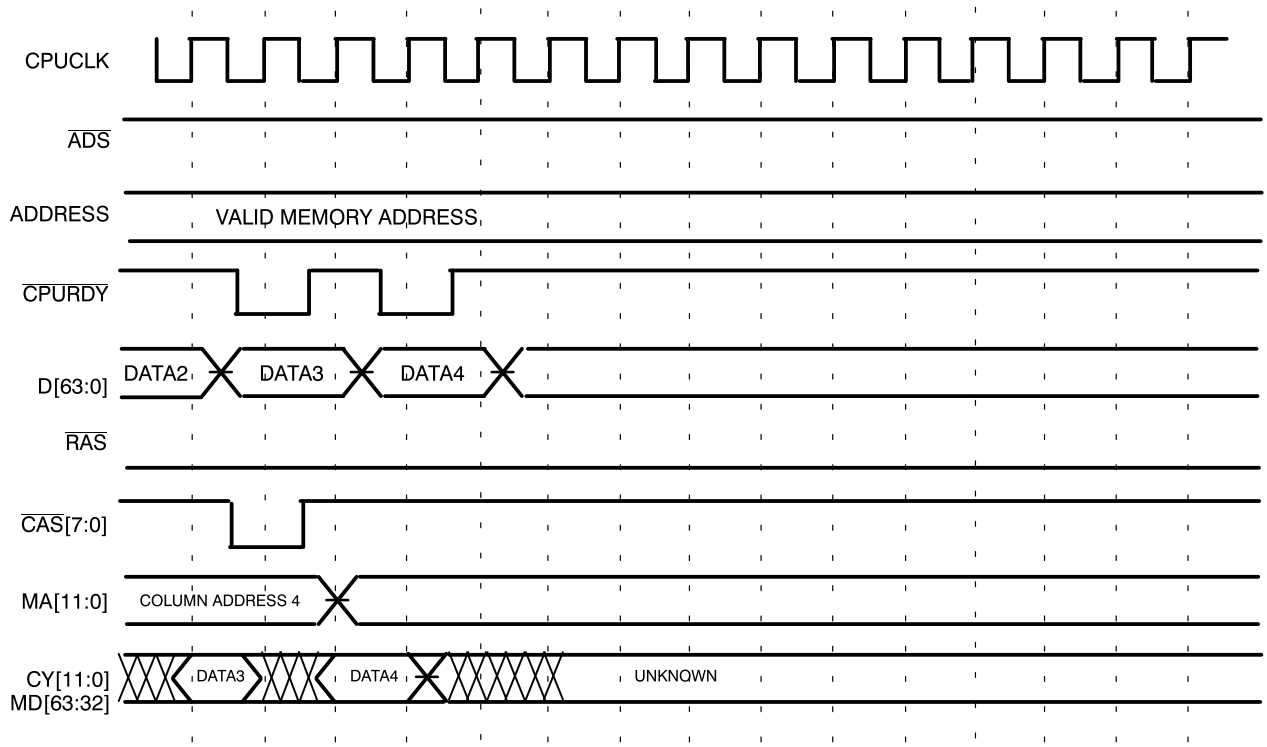
Switching Characteristics

Switching Waveforms (continued)

DRAM Line READ−EDO DRAM (Page Miss) Part 1 of 2



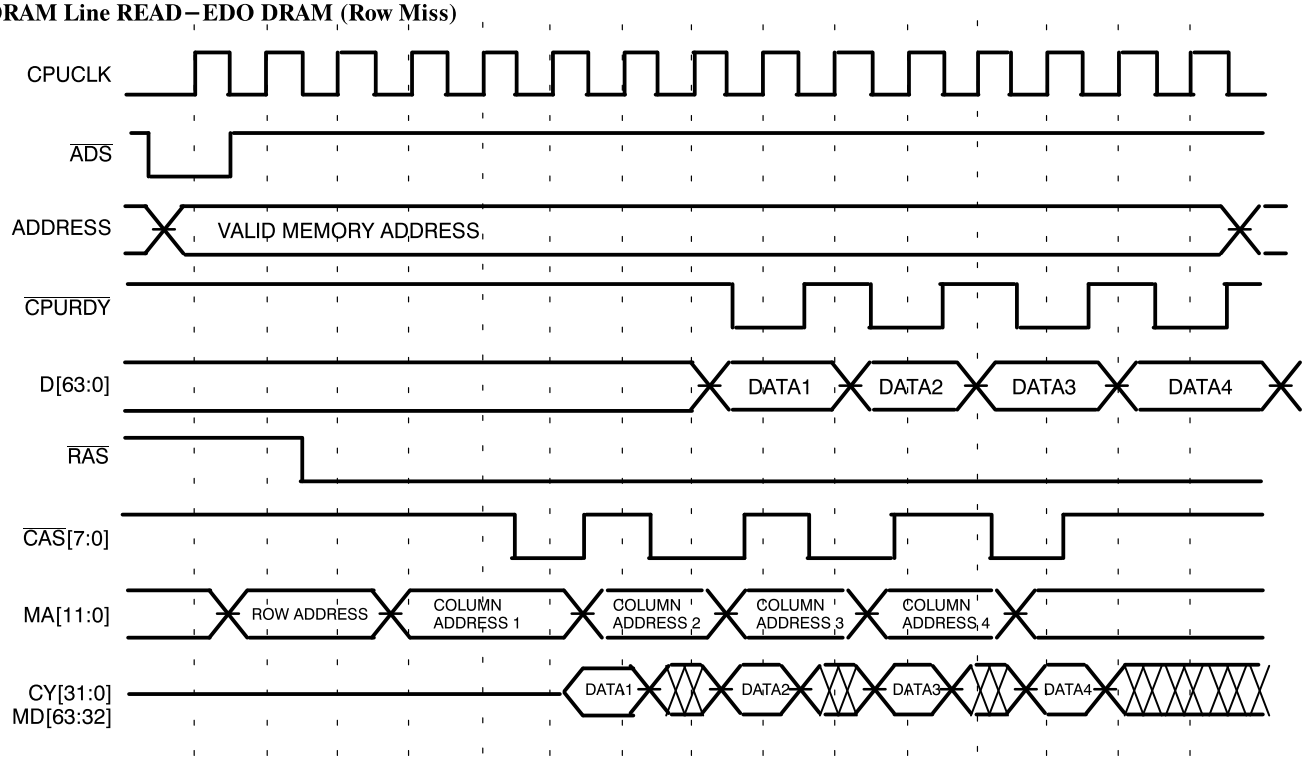
DRAM Line READ−EDO DRAM (Page Miss) Part 2 of 2



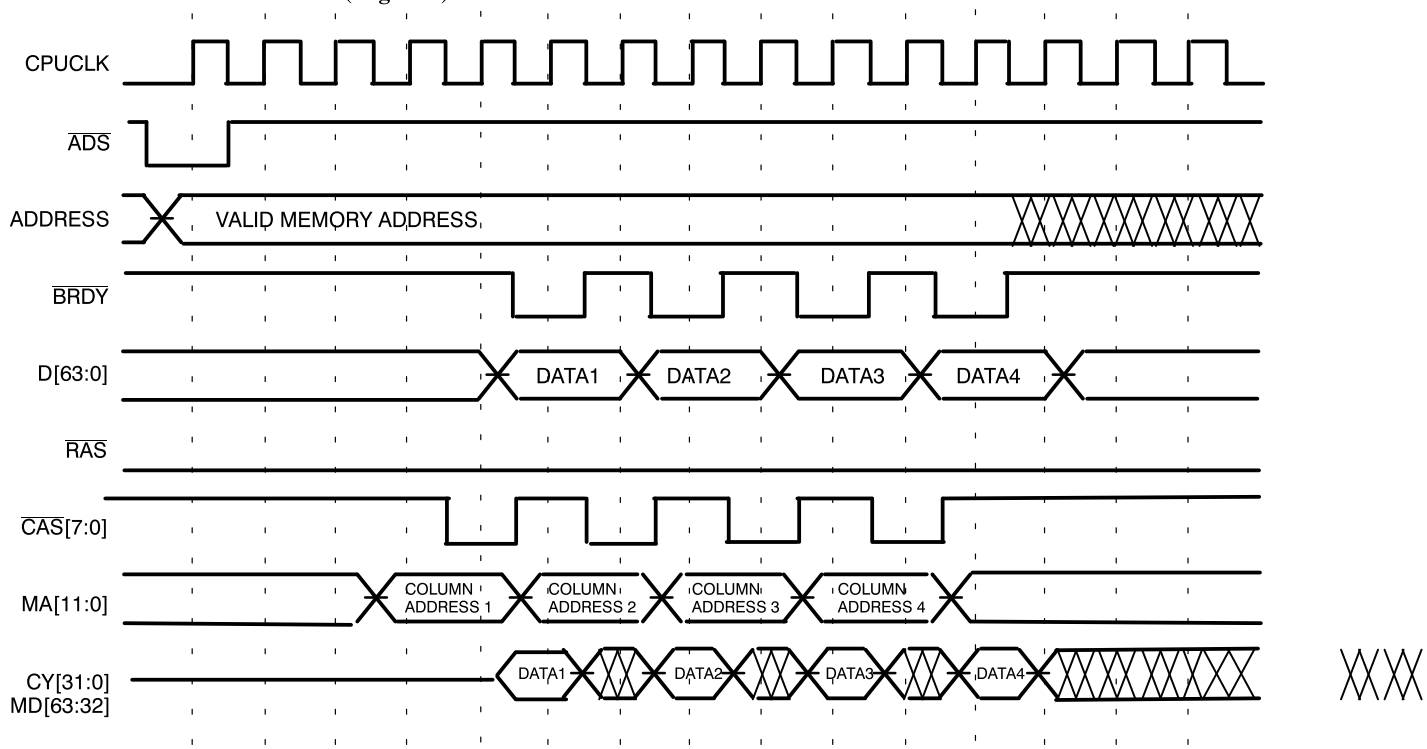
Switching Characteristics

Switching Waveforms (continued)

DRAM Line READ−EDO DRAM (Row Miss)



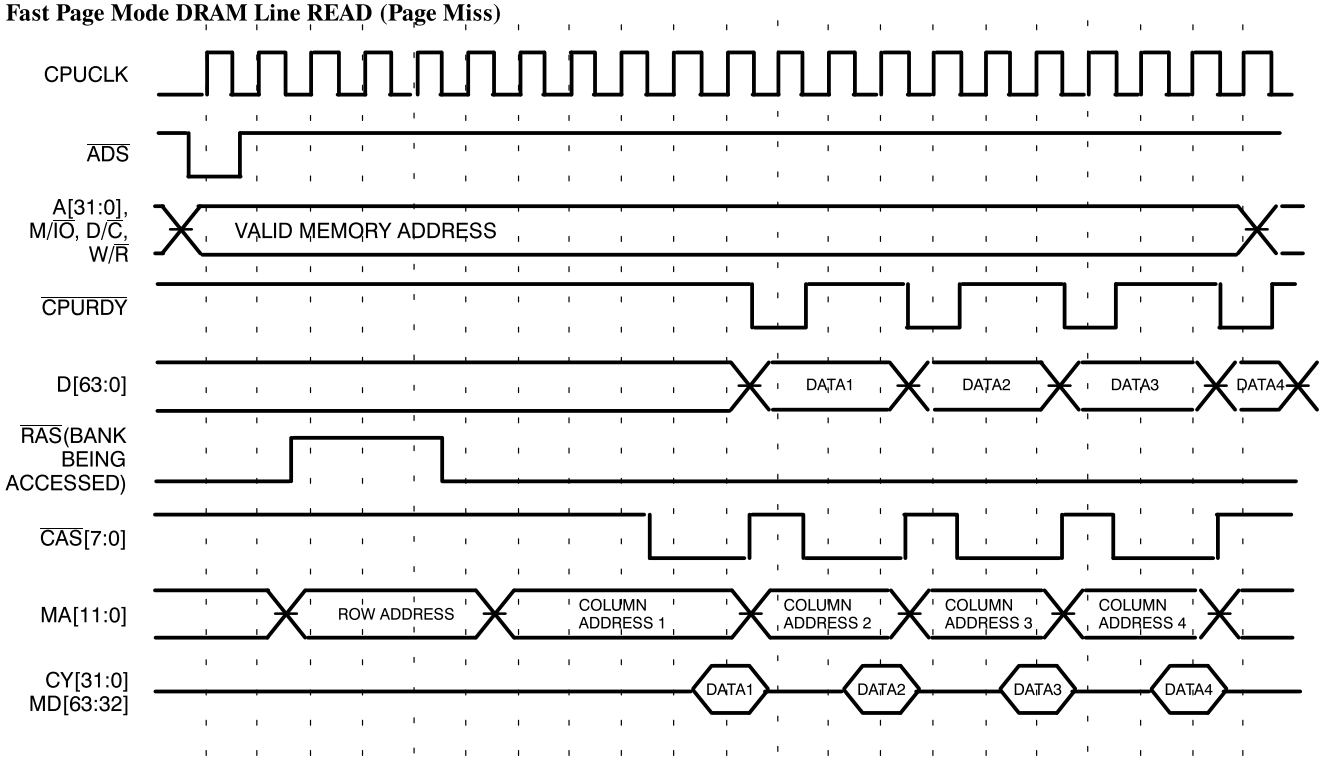
DRAM Line READ−EDO DRAM (Page Hit)



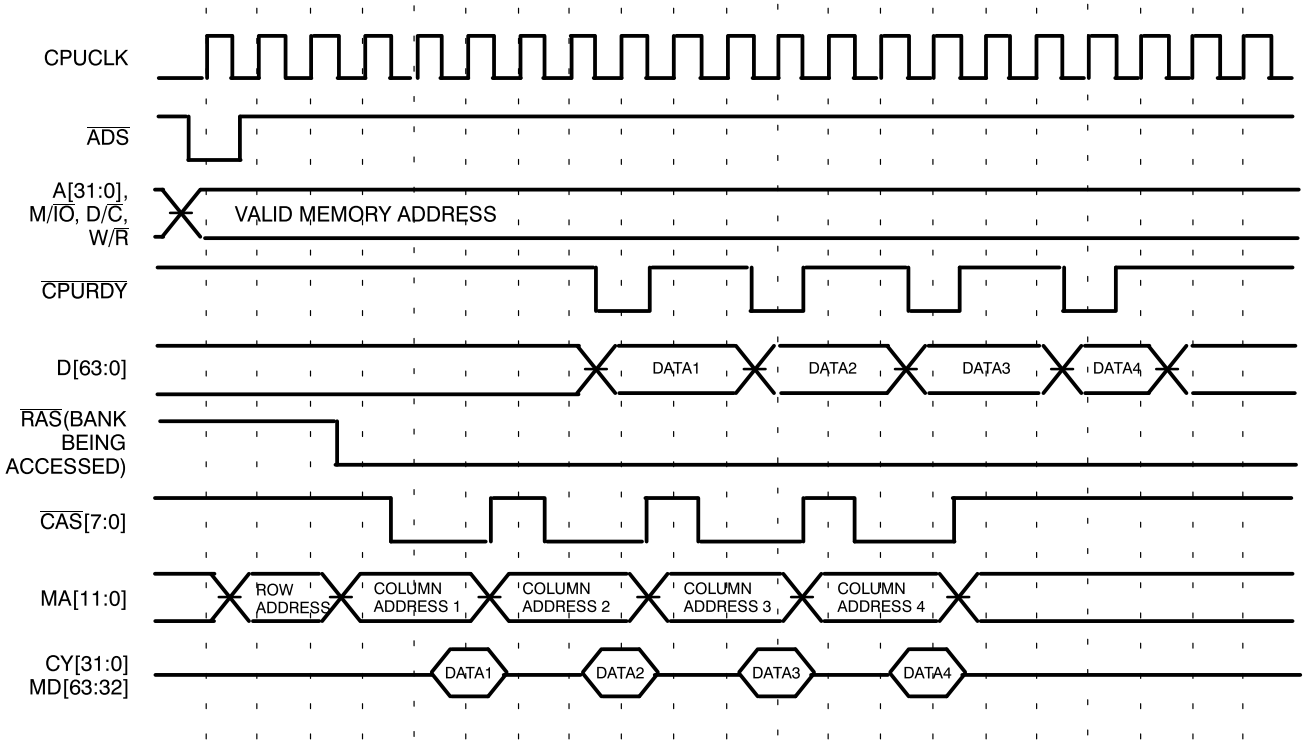
Switching Characteristics

Switching Waveforms (continued)

Fast Page Mode DRAM Line READ (Page Miss)



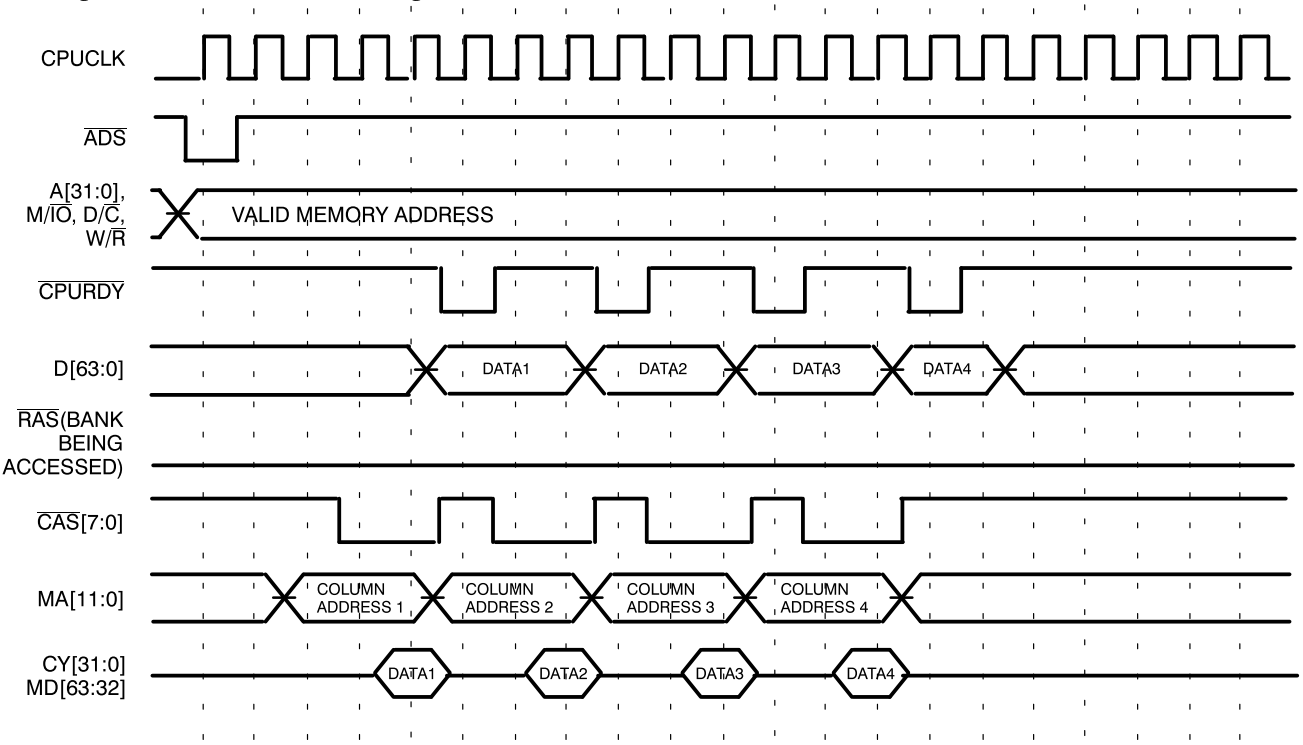
Fast Page Mode DRAM Line READ (Row Miss)



Switching Characteristics

Switching Waveforms (continued)

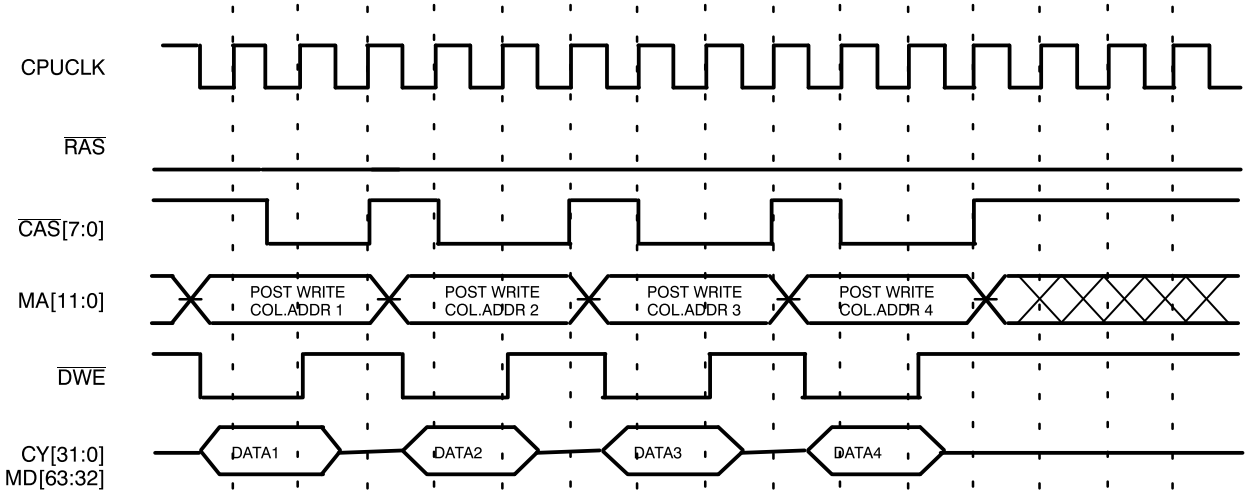
Fast Page Mode DRAM Line READ (Page Hit)



Switching Characteristics

Switching Waveforms (continued)

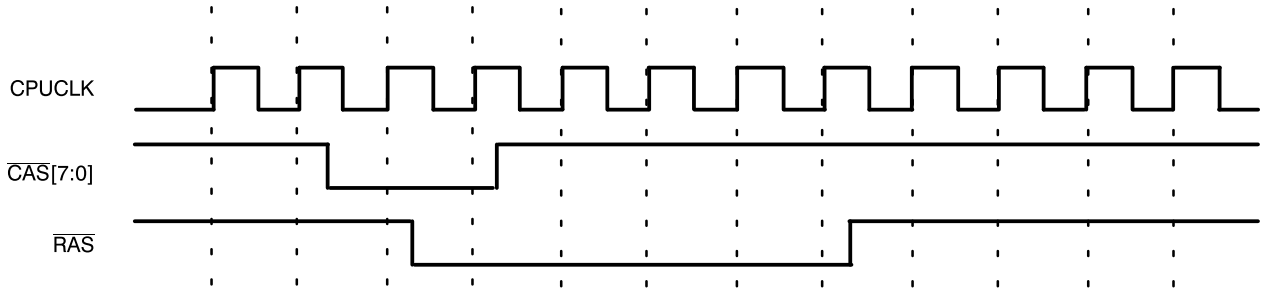
POST-WRITE FIFO WRITE TO FAST PAGE MODE/EDO DRAM (Page Hit)



Switching Characteristics

Switching Waveforms (continued)

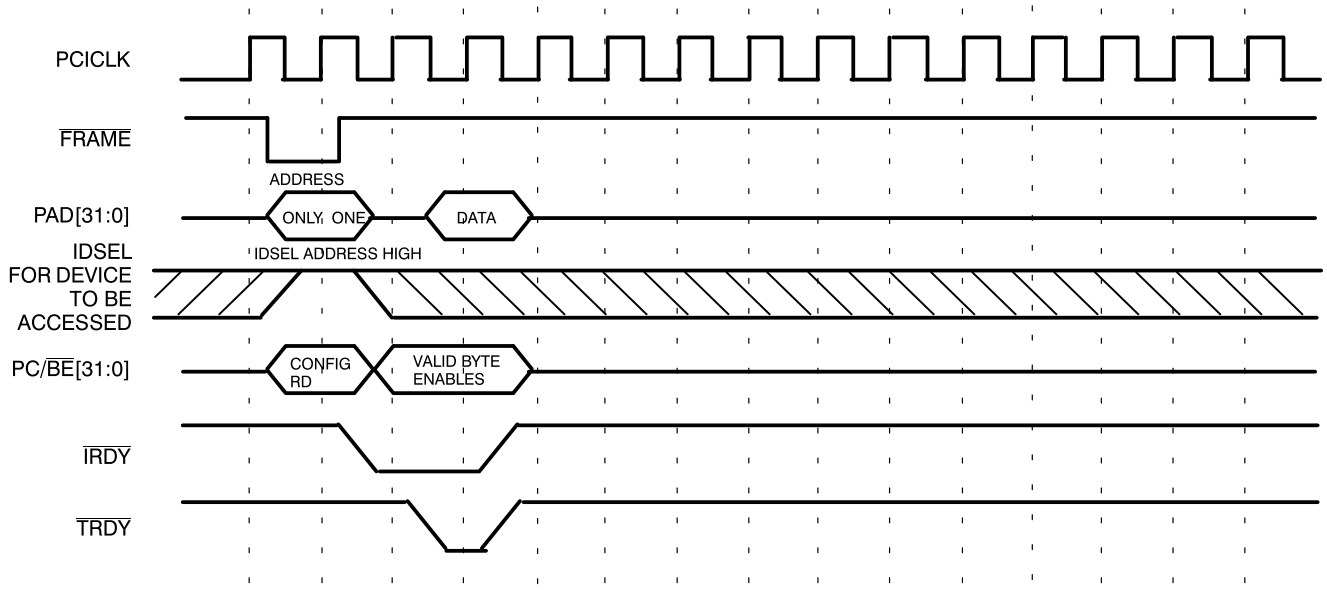
DRAM REFRESH



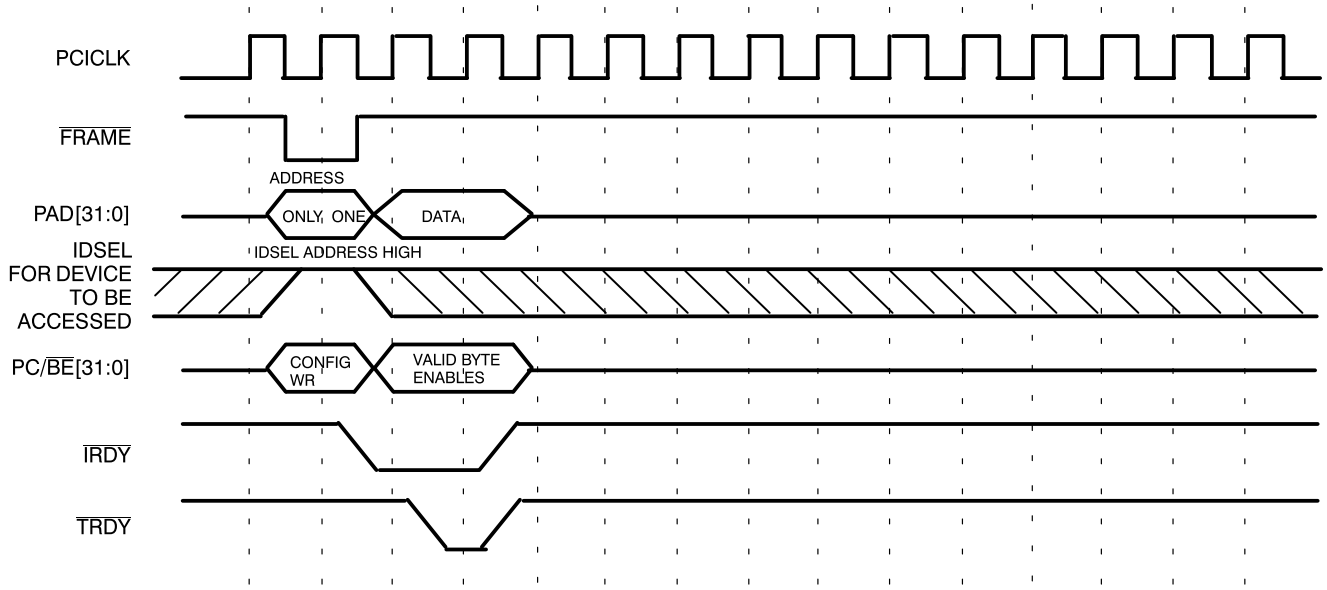
Switching Characteristics

Switching Waveforms (continued)

PCI Configuration READ Cycle (generated by Config Mechanism 1 Accesses)



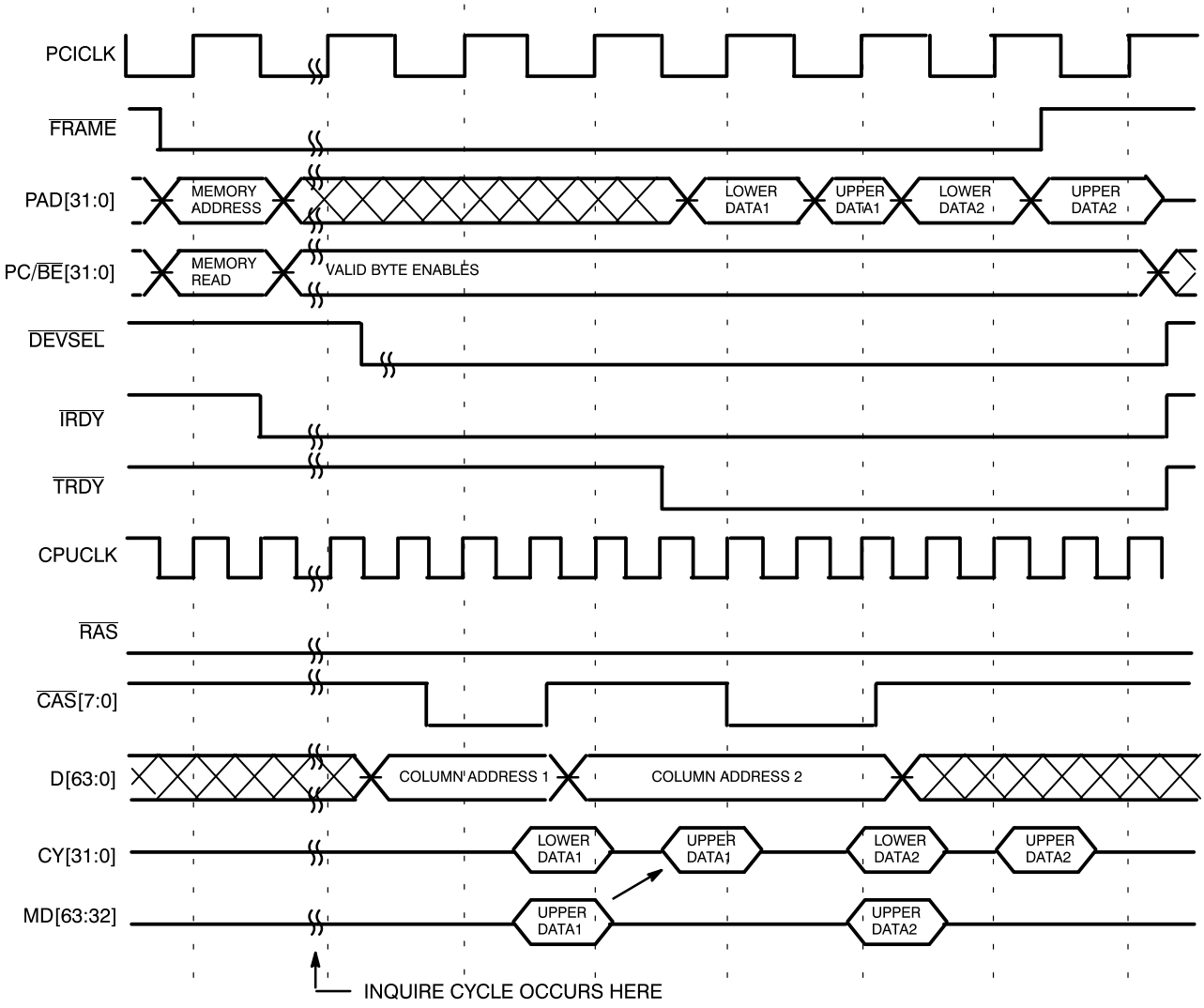
PCI Configuration WRITE Cycle (generated by Config Mechanism 1 Accesses)



Switching Characteristics

Switching Waveforms (continued)

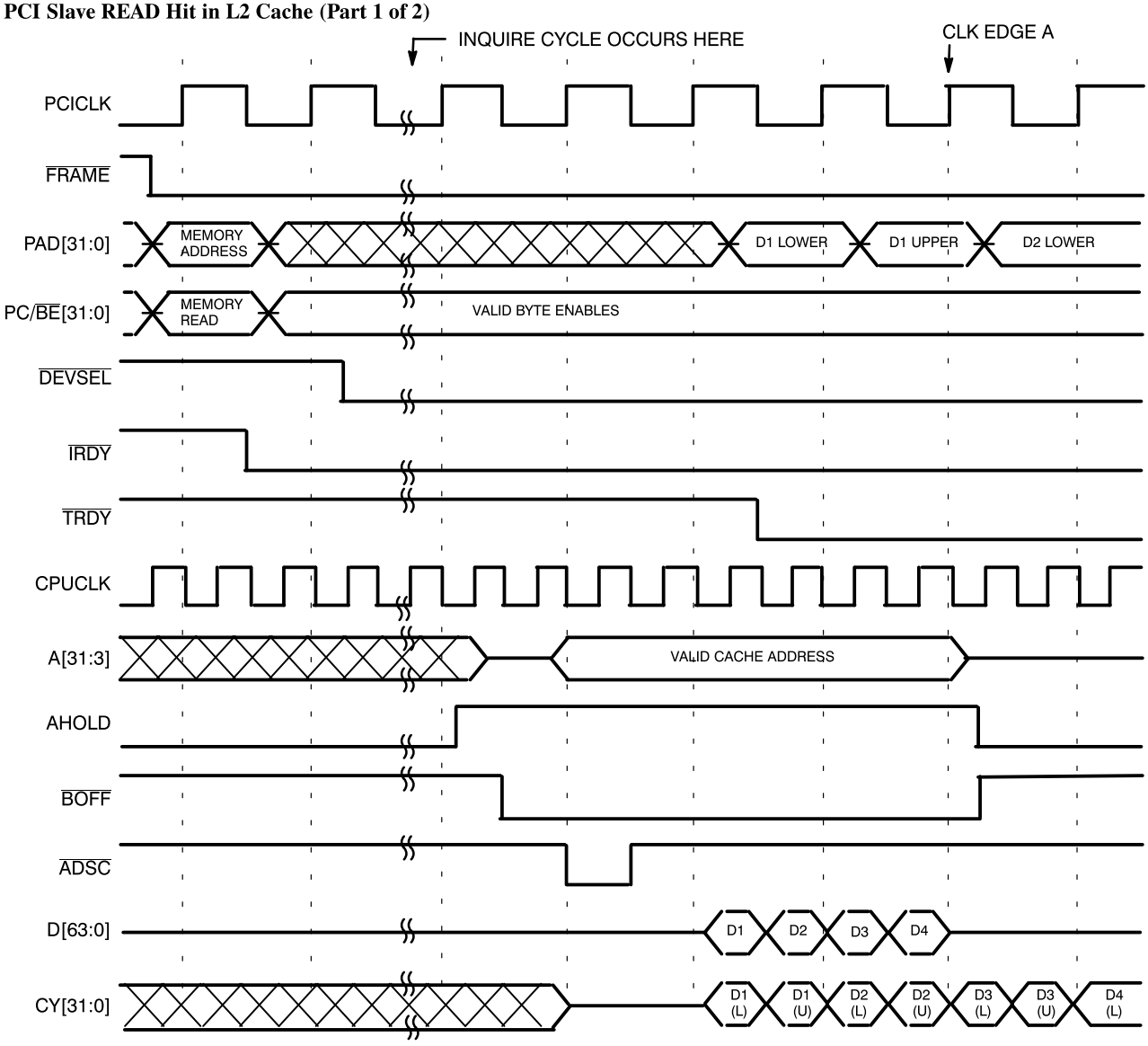
691 PCI Slave to FPM DRAM READ (Page Hit)



Switching Characteristics

Switching Waveforms (continued)

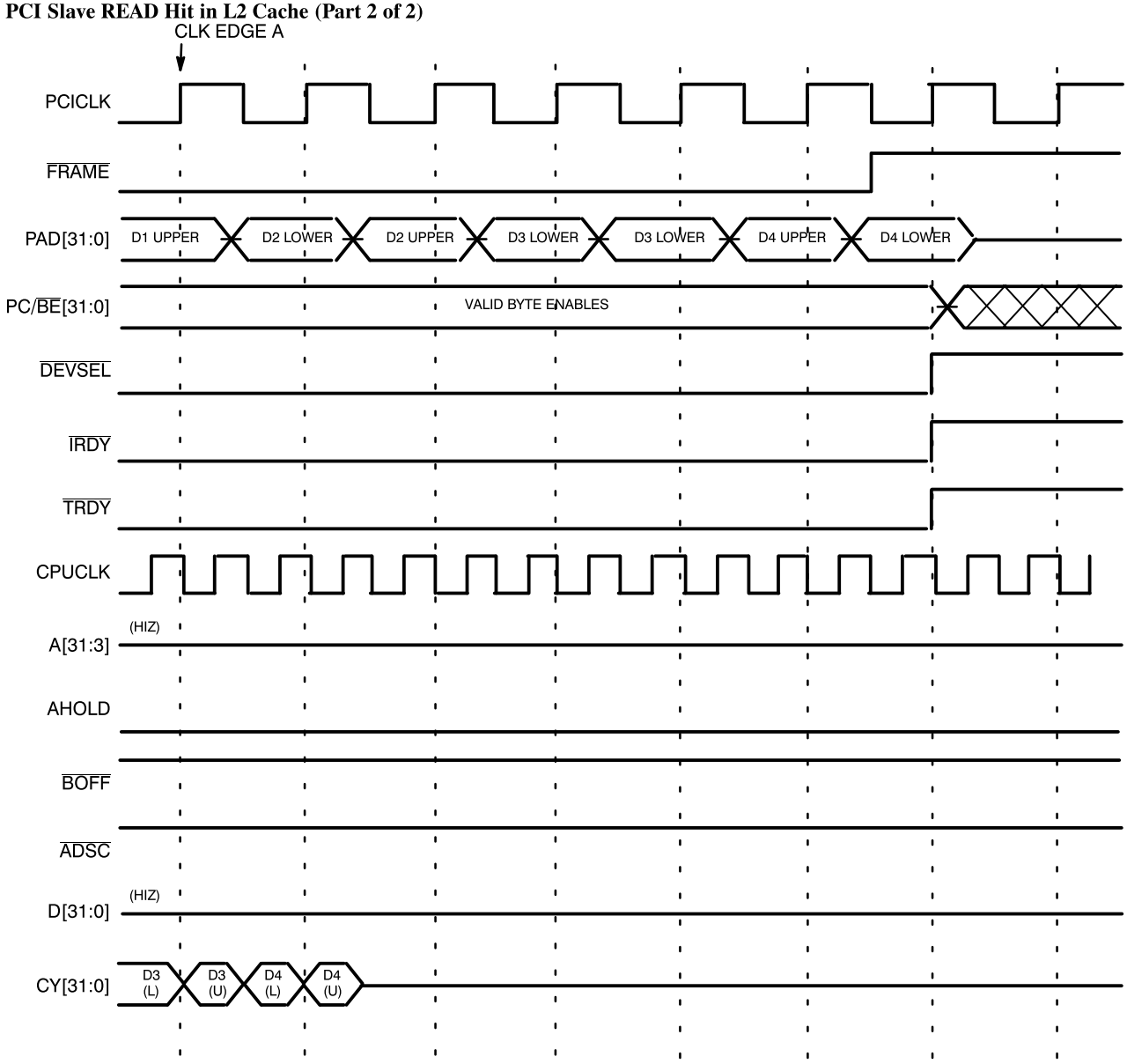
PCI Slave READ Hit in L2 Cache (Part 1 of 2)



Switching Characteristics

Switching Waveforms (continued)

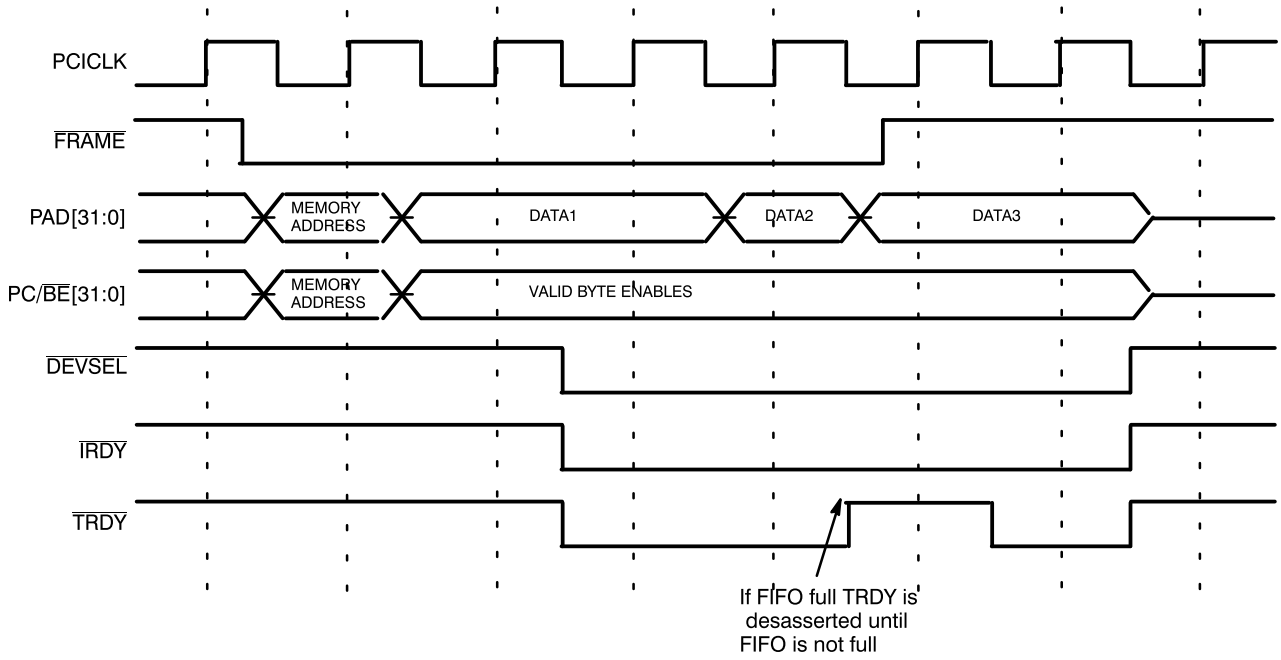
PCI Slave READ Hit in L2 Cache (Part 2 of 2)



Switching Characteristics

Switching Waveforms (continued)

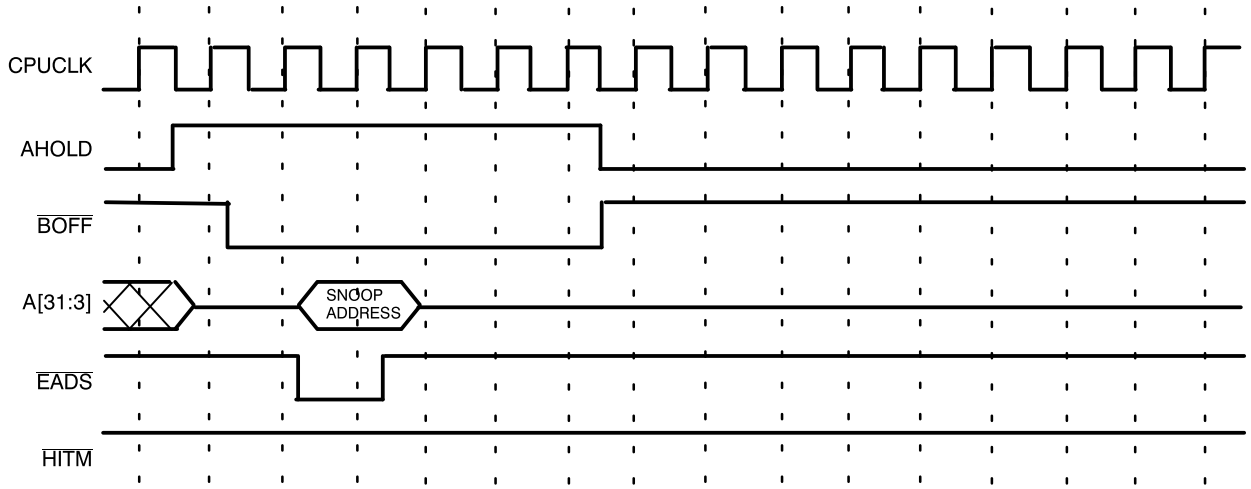
PCI Slave WRITE to Memory post write FIFOS



Switching Characteristics

Switching Waveforms (continued)

Inquire Cycle (Miss in L1 Cache or Hit on Clean L1 Line)



Inquire Cycle (Hit in L1 Cache on a Modified Line)