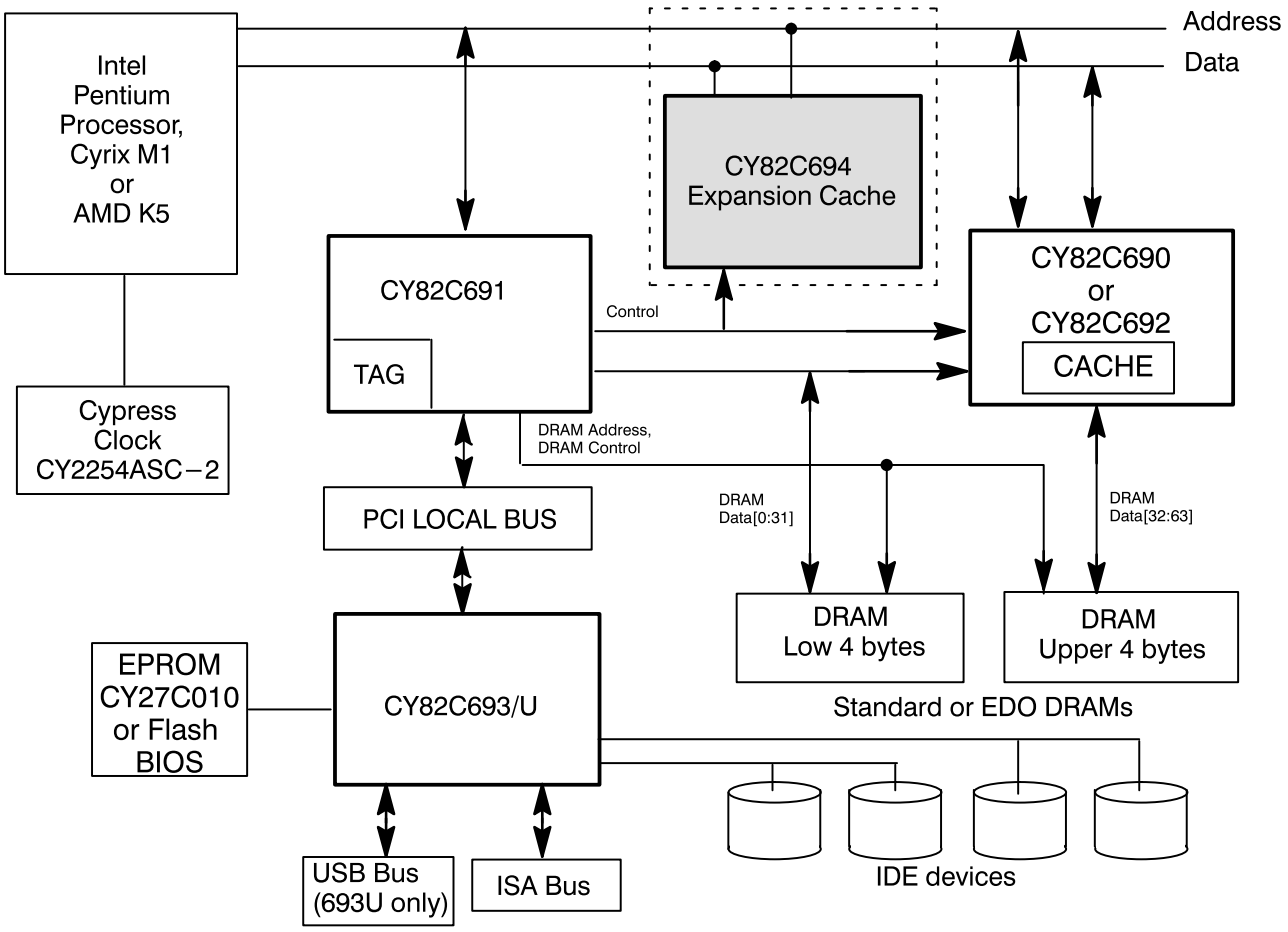
*ADVANCED INFORMATION* **CY82C694**

# Pentium™ hyperCache™ Chipset 128KB Expansion RAM

## Features

- **Interfaces directly to hyperCache™ Chipset at 66 MHz with 0 wait states**
- **Fully registered inputs and outputs in Pipelined mode operation**
- **16K x 64 common I/O architecture**
- **I/Os capable of 3.3V operation**
- **Fast Clock-to-output times**
  - **— $T_{CO}$=8.5 ns (for 66-MHz systems)**
- **User selectable Two-bit wraparound burst counter supporting Intel™ interleaved or linear bust sequences**
- **Separate processor and controller address strobes**
- **Synchronous self-timed writes**
- **Asynchronous output enable**
- **14 mm x 20 mm 128-pin TQFP package**

**System Block Diagram (hC−VX, hC−DX, hC−ZX solutions)**

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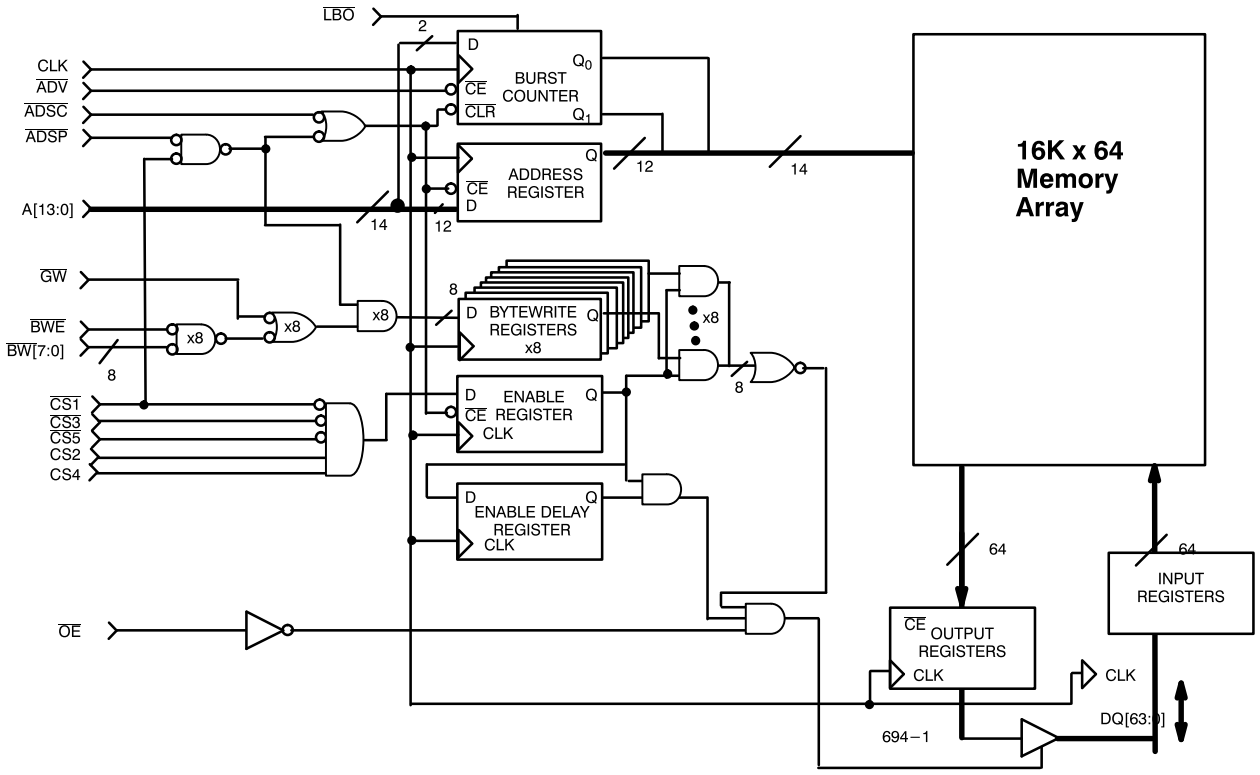
## Logic Block Diagram

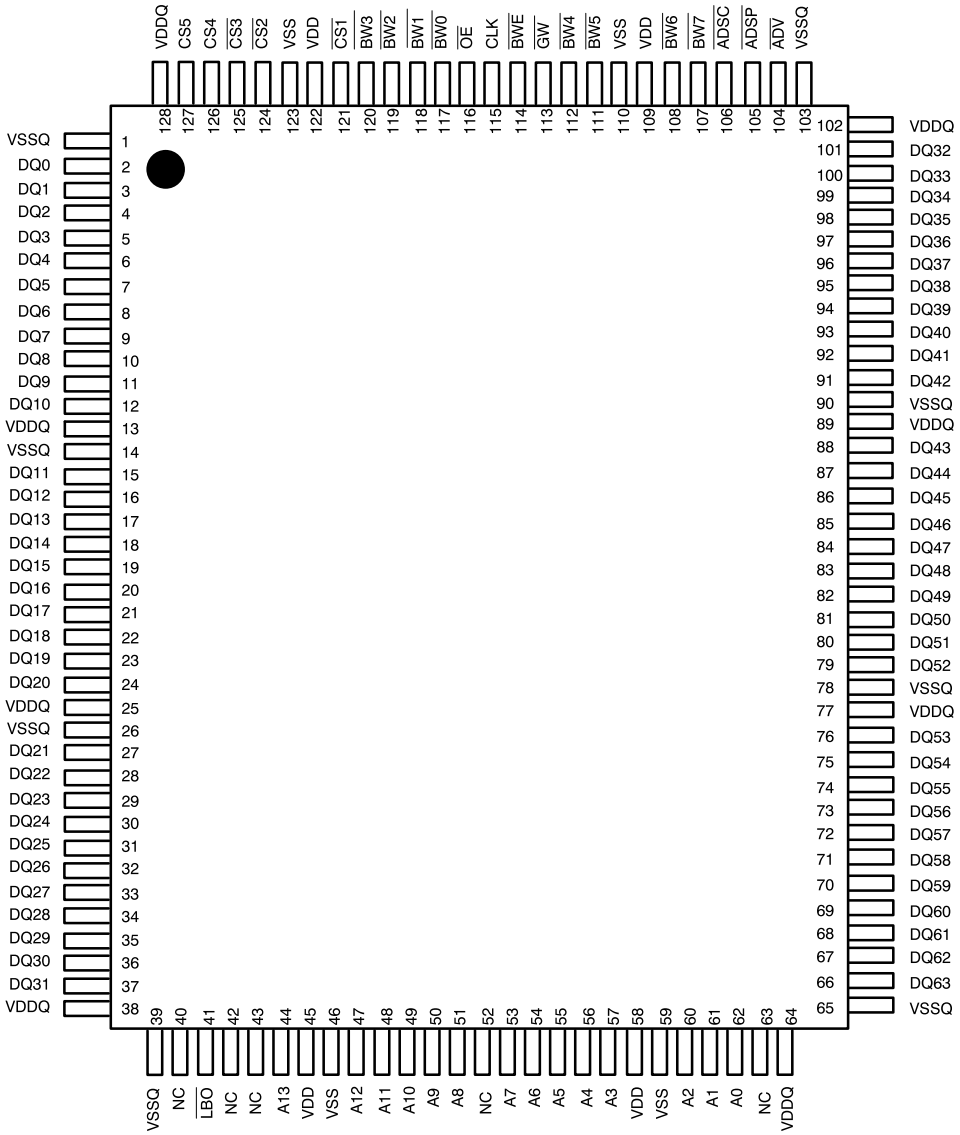


## Selection Guide

| | | 82C694−8 | 82C694−10 |
|---|---|---|---|
| Maximum Access Time (ns) $T_{CO}$ | | 8.5 | 10.0 |
| Maximum Operating Current (mA) | Commercial | TBD | TBD |

## Pin Configuration

**128-pin TQFP**
**Top View**



## Introduction

### System Overview

The hyperCache™ family is a family of three chipsets created to provide flexible solutions for today's PC designs. The hC-ZX, hC-VX, hC-DX Chipsets provide all the functions necessary to implement a 3.3V Pentium-class processor based system with the USB (Universal Serial Bus), PCI (Peripheral Component Interconnect), and the ISA (Industry Standard Architecture) buses. System designers can exploit the advantages of the USB and PCI buses while maintaining access to the large base of ISA cards in the marketplace.

The Cypress hyperCache family offers system designers several key advantages. With only three chips, a complete system can be implemented. Cache can be added up to 1 MB with additional CY82C694 devices in 128-KB increments All chipset solutions are pin-compatible and provide flexible upgrade paths through on-board or external cache modules. Six banks of page-mode or EDO DRAM further increase the system designer's options. The chipset also contains concurrent bus support, PCI enhanced IDE with CD-ROM support, integrated RTC, integrated peripheral control (Interrupts/ DMA), and integrated keyboard controller. This chipset is flexible enough to provide the system designer with many cost/performance/function options to provide an optimum solution for a given design.

### CY82C694 Introduction

The CY82C694 is a 16K by 64 synchronous/pipelined cache Burst SRAM (BSRAM) designed to support a zero wait state secondary cache with minimal glue logic.

## Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise in pipelined mode ($T_{CO}$) is 8.5 ns. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

The CY82C694 supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486 processors. The linear burst sequence is suited for processors that utilize a linear burst sequence, such as the Cyrix M1. The burst order is user selectable, and is determined by sampling the $\overline{LBO}$ (Linear Burst Order) input. Accesses can be initiated with either the processor address strobe ($\overline{ADSP}$) or the controller address strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW}0-7$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all eight bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Five synchronous chip selects ($\overline{CS1}$, $\overline{CS3}$, $\overline{CS5}$, CS2, CS4) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output three-state control. $\overline{ADSP}$ is ignored if $\overline{CS1}$ is HIGH.

### Pipelined Mode

*Single Read Accesses*

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) $\overline{CS1}$, $\overline{CS3}$, $\overline{CS5}$, CS2, and CS4 are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW0}-\overline{BW7}$) are all deasserted HIGH. $\overline{ADSP}$ is ignored if $\overline{CS1}$ is HIGH. The address presented to the address inputs (A0−A13) is stored into the address advancement logic and the Address Register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 8.5 ns. When the asynchronous Output Enable ($\overline{OE}$) is asserted LOW, the data outputs are controlled by the Enable and Enable Delay Registers. When the SRAM is emerging from a deselected state to a selected state, its outputs are always three-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{OE}$ signal. Consecutive single read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output will three-state immediately.

*Single Write Accesses Initiated by $\overline{ADSP}$*

This accesses are initiated when both of the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW, and (2) $\overline{CS1}$, $\overline{CS3}$, $\overline{CS5}$, CS2, and CS4 are all asserted active. The address presented to A0−A13 is loaded into the address register and the address advancement logic while being delivered to the RAM core. The write signals ($\overline{GW}$ and $\overline{BW0}-\overline{BW7}$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$ triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the DQ0−DQ63 inputs is written into the corresponding address location in the RAM core. If $\overline{GW}$ is HIGH, then the write operation is controlled by $\overline{BWE}$ and $\overline{BW}[7:0]$ signals. The CY82C694 provides byte write capability that is described in the writecycle description table. Asserting the Byte Write Enable input ($\overline{BWE}$) with the selected Byte Write ($\overline{BW0}-\overline{BW7}$) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A Synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY82C694 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ0−DQ63 inputs. Doing so will three-state the output drivers. As a safety precaution, DQ0−DQ63 are automatically three-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

*Single Write Accesses Initiated by $\overline{ADSC}$*

$\overline{ADSC}$ write accesses in Pipelined mode are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) $\overline{ADSP}$ is deasserted HIGH, (3) $\overline{CS1}$, $\overline{CS3}$, $\overline{CS5}$, CS2, and CS4 are all asserted active, and (4) the appropriate combination of the write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW0}-\overline{BW7}$) are asserted active to conduct a write to the desired byte(s). $\overline{ADSC}$ triggered write accesses require a single clock cycle to complete. The address presented to A0−A13 is loaded into the address register and the address advancement logic while being delivered to the RAM core. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the DQ0−DQ63 is written into the corresponding address location in the RAM core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A Synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY82C694 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the

DQ0−DQ63 inputs. Doing so will three-state the output drivers. As a safety precaution, DQ0−DQ63 are automatically three-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

## Burst Sequences

The CY82C694 provides a two-bit wraparound counter, fed by $A_0$ and $A_1$, that implement either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence, such as the Cyrix M1. The burst sequence is user selectable through the $\overline{LBO}$ (Linear Bust Order) input.

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

**Interleaved Burst Sequence**

| First Address | Second Address | Third Address | Fourth Address |
|---|---|---|---|
| Ax+1, Ax | Ax+1, Ax | Ax+1, Ax | Ax+1, Ax |
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

**Linear Burst Sequence**

| First Address | Second Address | Third Address | Fourth Address |
|---|---|---|---|
| Ax+1, Ax | Ax+1, Ax | Ax+1, Ax | Ax+1, Ax |
| 00 | 01 | 10 | 11 |
| 01 | 10 | 11 | 00 |
| 10 | 11 | 00 | 01 |
| 11 | 00 | 01 | 10 |

## Cycle Descriptions

| Next Cycle | Add. Used | CS4 | CS2 | $\overline{CS5}$ | $\overline{CS3}$ | $\overline{CS1}$ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{OE}$ | DQ | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Unselected | none | X | X | X | X | 1 | X | 0 | X | X | Hi-Z | X |
| Unselected | none | 0 | X | X | X | 0 | 0 | X | X | X | Hi-Z | X |
| Unselected | none | X | 0 | X | X | 0 | 0 | X | X | X | Hi-Z | X |
| Unselected | none | X | X | 1 | X | 0 | 0 | X | X | X | Hi-Z | X |
| Unselected | none | X | X | X | 1 | 0 | 0 | X | X | X | Hi-Z | X |
| Unselected | none | 0 | X | X | X | 0 | 1 | 0 | X | X | Hi-Z | X |
| Unselected | none | X | 0 | X | X | 0 | 1 | 0 | X | X | Hi-Z | X |
| Unselected | none | X | X | 1 | X | 0 | 1 | 0 | X | X | Hi-Z | X |
| Unselected | none | X | X | X | 1 | 0 | 1 | 0 | X | X | Hi-Z | X |
| Begin Read[1] | External | 1 | 1 | 0 | 0 | 0 | 0 | X | X | X | Hi-Z | X |
| Begin Read[1] | External | 1 | 1 | 0 | 0 | 0 | 1 | 0 | X | X | Hi-Z | Read |
| Continue Read | Next | X | X | X | X | X | 1 | 1 | 0 | 1 | Hi-Z | Read |
| Continue Read | Next | X | X | X | X | X | 1 | 1 | 0 | 0 | Q | Read |
| Continue Read | Next | X | X | X | X | 1 | X | 1 | 0 | 1 | Hi-Z | Read |
| Continue Read | Next | X | X | X | X | 1 | X | 1 | 0 | 0 | Q | Read |
| Suspend Read | Current | X | X | X | X | X | 1 | 1 | 1 | 1 | Hi-Z | Read |
| Suspend Read | Current | X | X | X | X | X | 1 | 1 | 1 | 0 | Q | Read |
| Suspend Read | Current | X | X | X | X | 1 | X | 1 | 1 | 1 | Hi-Z | Read |
| Suspend Read | Current | X | X | X | X | 1 | X | 1 | 1 | 0 | Q | Read |
| Begin Write | Current | X | X | X | X | X | 1 | 1 | 1 | X | D | Write[1] |
| Begin Write | Current | X | X | X | X | 1 | X | 1 | 1 | X | D | Write[1] |
| Begin Write | External | 1 | 1 | 0 | 0 | 0 | 1 | 0 | X | X | D | Write[1] |
| Continue Write | Next | X | X | X | X | X | 1 | 1 | 0 | X | D | Write[1] |
| Continue Write | Next | X | X | X | X | 1 | X | 1 | 0 | X | D | Write[1] |
| Suspend Write | Current | X | X | X | X | X | 1 | 1 | 1 | X | D | Write[1] |
| Suspend Write | Current | X | X | X | X | 1 | X | 1 | 1 | X | D | Write[1] |

X=Don't Care, 1=Logic HIGH, 0=Logic LOW.

**Note:**
1. Writes defined by $\overline{BW}$[7:0], $\overline{GW}$, and $\overline{BWE}$, see Write Cycle Descriptions table.

## Write Cycle Descriptions

| Function[2] | $\overline{GW}$ | $\overline{BWE}$ | $\overline{BW7}$ | $\overline{BW6}$ | $\overline{BW5}$ | $\overline{BW4}$ | $\overline{BW3}$ | $\overline{BW2}$ | $\overline{BW1}$ | $\overline{BW0}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Read | 1 | 1 | X | X | X | X | X | X | X | X |
| Read | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Write All Byte | 0 | X | X | X | X | X | X | X | X | X |
| Write Byte 0 – DQ[7:0] | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| Write Byte 1 – DQ[15:8] | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| Write Byte 2 – DQ[23:16] | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| Write Byte 3 – DQ[31:24] | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| Write Byte 4 – DQ[39:32] | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| Write Byte 5 – DQ[47:40] | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| Write Byte 6 – DQ[55:48] | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| Write Byte 7 – DQ[63:56] | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Write Byte 1, 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| Write Byte 2, 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| Write Byte 2, 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| Write Byte 2, 1, 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| Write Byte 3, 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| Write Byte 3, 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| Write Byte 3, 1, 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| Write Byte 3, 2 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| Write Byte 3, 2, 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| Write Byte 3, 2 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| The remainder follows the same pattern as above. | | | | | | | | | | |

X=Don't Care, 1=Logic HIGH, 0=Logic LOW.

**Note:**
2. The SRAM always starts a Read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, $\overline{BW}$[7:0].

## Pin Description

| Name | I/O | Pin Number | Description |
|---|---|---|---|
| CLK | I | 115 | Clock input. Used to capture the address, data, and control signals (except for $\overline{OE}$). Also used to advance the on-chip burst counter during a burst sequence when $\overline{ADV}$ is asserted. |
| DQ[63:00] | I/O | 2−12, 15−24, 27−37, 66−76, 79−88, 91−101 | 64 bidirectional data I/O lines, used as inputs and outputs to the RAM core. As inputs, they feed into an on-chip register that is triggered by the rising edge of the clock. As outputs, they carry the read data from the selected RAM core location. The direction of the data pins is controlled by $\overline{OE}$: when $\overline{OE}$ is asserted LOW the data pins are driven by the output buffers and are outputs, when $\overline{OE}$ is deasserted HIGH, the data pins are three-stated and can be used as inputs. During the first clock of an initial access cycle, the data pins are three-stated by the Enable and Enable Delay registers. Additionally, the data lines are automatically three-stated when a write cycle is detected. |
| A[13:0] | I | 44, 47−51, 53−57, 60−62 | Fourteen address inputs used to select one of 16K locations. These inputs are captured on the rising edge of the clock if $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, and the device has been selected. A1 and A0 are also loaded into the auto-address-increment logic. |
| $\overline{BWE}$ | I | 114 | Byte Write Enable input sampled at the rising edge of the clock. Used in conjunction with $\overline{BW}$[7:0] to conduct byte write operations. $\overline{BW}$[7:0] are qualified with $\overline{BWE}$. When asserted, $\overline{GW}$ overrides all byte writes, and a global write occurs. |
| $\overline{BW}$[7:0] | I | 107−108, 112−113, 120−117 | Byte Write Select inputs sampled at the rising edge of the clock. During write cycles, these inputs can be used to selectively write certain bytes in the RAM core. These inputs are qualified with Byte Write Enable ($\overline{BWE}$) input. See the Write Table to determine which Byte Write Select corresponds to which data byte. |
| $\overline{GW}$ | I | 113 | Global Write Enable input sampled at the rising edge of the clock. Used to conduct global writes. When asserted, $\overline{GW}$ overrides all byte writes, and a global write occurs. |
| $\overline{CS1}$ | I | 121 | Chip enable, active LOW, sampled at the rising edge of the clock, and $\overline{ADSP}$ mask (i.e., $\overline{ADSP}$ is ignored if $\overline{CS1}$ is HIGH). |
| $\overline{CS2}$, $\overline{CS3}$ | I | 124, 125 | Depth expansion Chip enables, active LOW, sampled at the rising edge of the clock. |
| CS4, CS5 | I | 126, 127 | Depth expansion Chip enables, active HIGH, sampled at the rising edge of the clock. |
| $\overline{LBO}$ | I | 41 | Linear Burst Order input. Used to determine the burst order (linear or interleaved). Tieing this signal LOW will establish a linear burst order. Tieing this signal HIGH will establish an interleaved burst order. |
| $\overline{FT}$ | I | 40 | Flow-Through input. Used to select either Pipelined or Flow-Through mode of operation. Tieing this signal LOW will place the device in the Flow-Through mode. Tieing this signal HIGH will place the device in the Pipelined mode. |
| $\overline{OE}$ | I | 116 | Asynchronous Output Enable. Active LOW, used to control the three-state buffers onto the Data I/O lines. $\overline{OE}$ is masked during the first clock of an initial read cycle, when the output buffers are controlled by the Enable and Enable delay registers. |
| $\overline{ADV}$ | I | 104 | Advance input signal, active LOW, sampled on the rising edge of the clock. When detected active it will cause the on-chip burst counter to increment to the next address in the burst sequence. This signal is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is asserted. |
| $\overline{ADSC}$ | I | 106 | Address input strobe from the controller, active LOW, sampled on the rising edge of the clock. When asserted, the address inputs are captured in the address register. A0 and A1 are also loaded into the 2-bit burst counter. $\overline{ADSC}$ is ignored when asserted with $\overline{ADSP}$. |
| $\overline{ADSP}$ | I | 105 | Address input strobe from the processor, active LOW, sampled on the rising edge of the clock. When asserted, the address inputs are captured in the address register. A0 and A1 are also loaded into the 2-bit burst counter. |
| $V_{DD}$ | Supply | 45, 58, 109, 122 | 5V power supply to the core of the CY82C694 |

## Pin Description (continued)

| Name | I/O | Pin Number | Description |
|---|---|---|---|
| $V_{SS}$ | Supply | 46, 59, 110, 123 | Ground. |
| $V_{DDQ}$ | Supply | 13, 25, 38, 64, 77, 89, 102, 128 | 5V or 3.3V power supply (Outputs) |
| $V_{SSQ}$ | Supply | 1, 14, 26, 39,65, 78, 90, 103 | Ground (outputs). |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on $V_{DD}$ Relative to GND .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[3] ..... −0.5V to $V_{DD}$ + 0.5V

DC Input Voltage[3] ..... −0.5V to $V_{DD}$ + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

| Range | Ambient Temperature[4] | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Com'l | 0°C to +70°C | 5V ± 5% | 3.0V to $V_{DD}$ |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{DD}$ = Min., $I_{OH}$ = −4.0 mA | | 2.4 | $V_{DDQ}$ | V |
| $V_{OL}$ | Output LOW Voltage | $V_{DD}$ = Min., $I_{OL}$ = 8.0 mA | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | $V_{DD}$ + 0.3V | V |
| $V_{IL}$ | Input LOW Voltage[3] | | | −0.3 | 0.8 | V |
| $I_X$ | Input Load Current | $GND \le V_I \le V_{DD}$ | | −1 | 1 | µA |
| $I_{OZ}$ | Output Leakage Current | $GND \le V_I \le V_{DD}$, Output Disabled | | −5 | 5 | µA |
| $I_{OS}$ | Output Short Circuit Current[5] | $V_{DD}$ = Max., $V_{OUT}$ = GND | | | −300 | mA |
| $I_{CC}$ | $V_{DD}$ Operating Supply Current | $V_{DD}$ = Max., Iout = 0 mA, f = $f_{MAX}$ = $1/t_{CYC}$ | Com'l | | 350 | mA |
| $I_{SB1}$ | Automatic CS Power-Down Current−TTL Inputs | Max. $V_{DD}$, Device Deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, f = $f_{MAX}$ | Com'l | | 100 | mA |
| $I_{SB2}$ | Automatic CS Power-Down Current−CMOS Inputs | Max. $V_{DD}$, Device Deselected, $V_{IN} \ge V_{DD}$ − 0.3V or $V_{IN} \le$ 0.3V, f = 0[6] | Com'l | | 45 | mA |

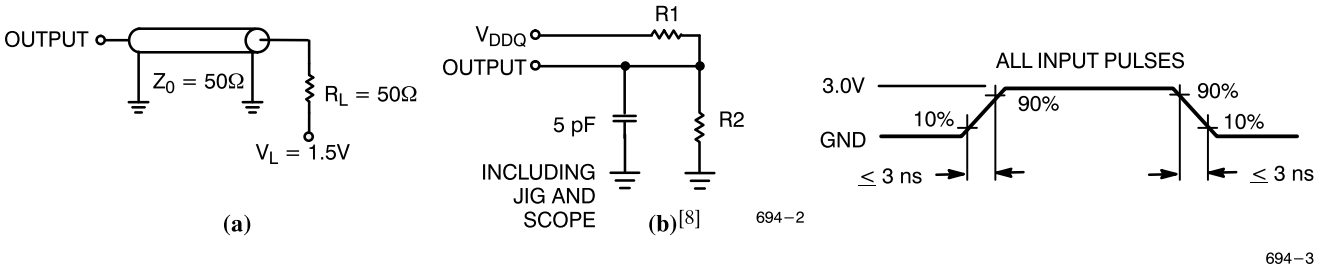
## Capacitance[7]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$: Addresses | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{DD}$ = 5.0V | 4.5 | pF |
| $C_{IN}$: Other Inputs | | | 5 | pF |
| $C_{OUT}$ | Output Capacitance | | 8 | pF |

**Notes:**

3. Minimum voltage equals −2.0V for pulse durations of less than 20 ns.
4. $T_A$ is the "instant on" case temperature.
5. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
6. Inputs are disabled, clock is allowed to run at speed.
7. Tested initially and after any design or process changes that may affect these parameters.
8. Resistor values for $V_{DDQ}$=5V are: R1=481Ω and R2=255Ω. Resistor values for $V_{DDQ}$=3.3V are R1=317Ω and R2=348Ω

## AC Test Loads and Waveforms




## Switching Characteristics Over the Operating Range[9]

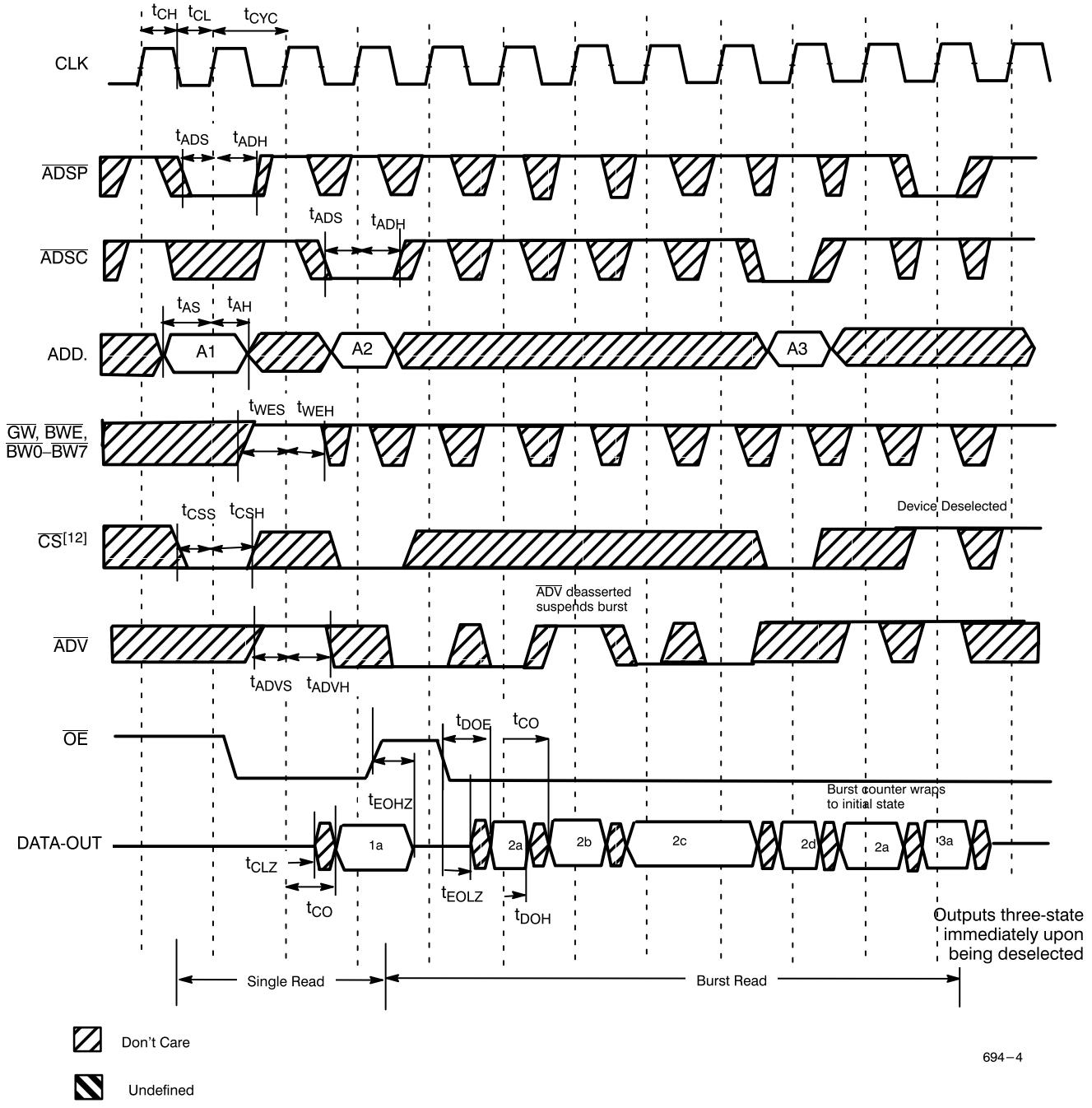
| Parameter | Description | –8 | | –10 | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CYC}$ | Clock Cycle Time | 15 | | 20 | | ns |
| $t_{CH}$ | Clock HIGH | 6 | | 6 | | ns |
| $t_{CL}$ | Clock LOW | 6 | | 6 | | ns |
| $t_{AS}$ | Address Set-Up Before CLK Rise | 2.5 | | 2.5 | | ns |
| $t_{AH}$ | Address Hold After CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{CO}$ | Data Output Valid After CLK Rise (Pipelined mode) | | 8.5 | | 10.0 | ns |
| $t_{DOH}$ | Data Output Hold After CLK Rise | 3 | | 3 | | ns |
| $t_{ADS}$ | $\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise | 2.5 | | 2.5 | | ns |
| $t_{ADH}$ | $\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{WES}$ | $\overline{BWE}$, $\overline{GW}$, $\overline{BW}$[7:0] Set-Up Before CLK Rise | 2.5 | | 2.5 | | ns |
| $t_{WEH}$ | $\overline{BWE}$, $\overline{GW}$, $\overline{BW}$[7:0] Hold After CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{ADVS}$ | $\overline{ADV}$ Set-Up Before CLK Rise | 2.5 | | 2.5 | | ns |
| $t_{ADVH}$ | $\overline{ADV}$ Hold After CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{DS}$ | Data Input Set-Up Before CLK Rise | 2.5 | | 2.5 | | ns |
| $t_{DH}$ | Data Input Hold After CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{CSS}$ | Chip Select Set-Up | 2.5 | | 2.5 | | ns |
| $t_{CSH}$ | Chip Select Hold After CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{CHZ}$ | Clock to High-Z[10] | 2 | 6 | 2 | 6 | ns |
| $t_{CLZ}$ | Clock to High-Z[10] | 0 | | 0 | | ns |
| $t_{EOHZ}$ | $\overline{OE}$ HIGH to Output High-Z[10, 11] | 2 | 6 | 2 | 6 | ns |
| $t_{EOLZ}$ | $\overline{OE}$ HIGH to Output Low-Z[10] | 0 | | 0 | 6 | ns |
| $t_{EOV}$ | $\overline{OE}$ LOW to Output Valid[10, 11] | | 6 | | 6 | ns |

**Notes:**

9. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified $I_{OL}/I_{OH}$ and load capacitance. Shown in (a) and (b) of AC test loads.
10. $t_{CHZ}$, $t_{CLZ}$, $t_{OEV}$, $t_{EOLZ}$, and $t_{EOHZ}$ are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
11. At any given voltage and temperature, $t_{EOHZ}$ min. is less than $t_{EOV}$ min.

## Switching Waveforms

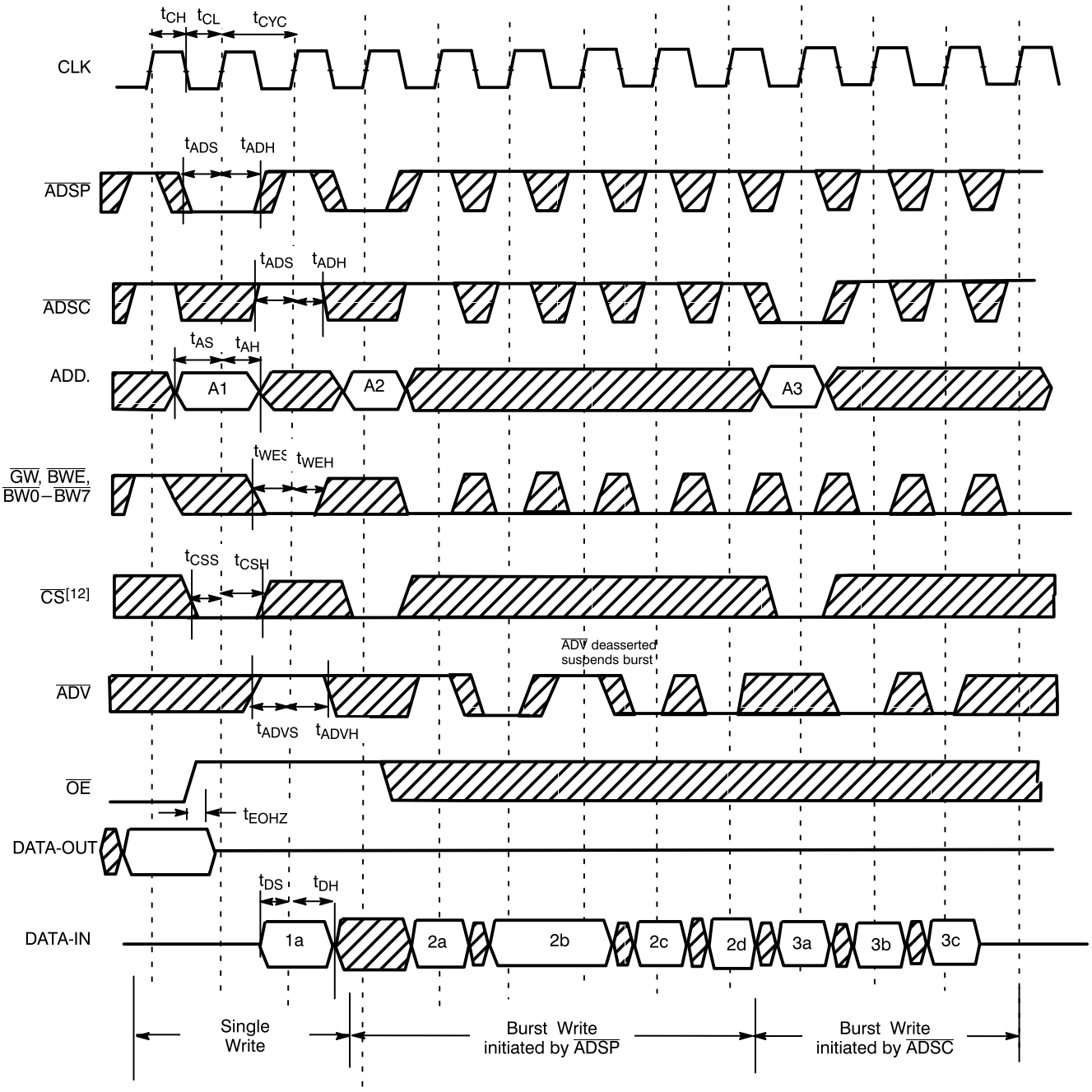
### Read Timing




**Note:**
12. $\overline{CS}$ signifies that all chip selects ($\overline{CS1}$, $\overline{CS3}$, $\overline{CS5}$, CS2, and CS4) are all asserted active.

## Switching Waveforms (continued)

### Write Timing

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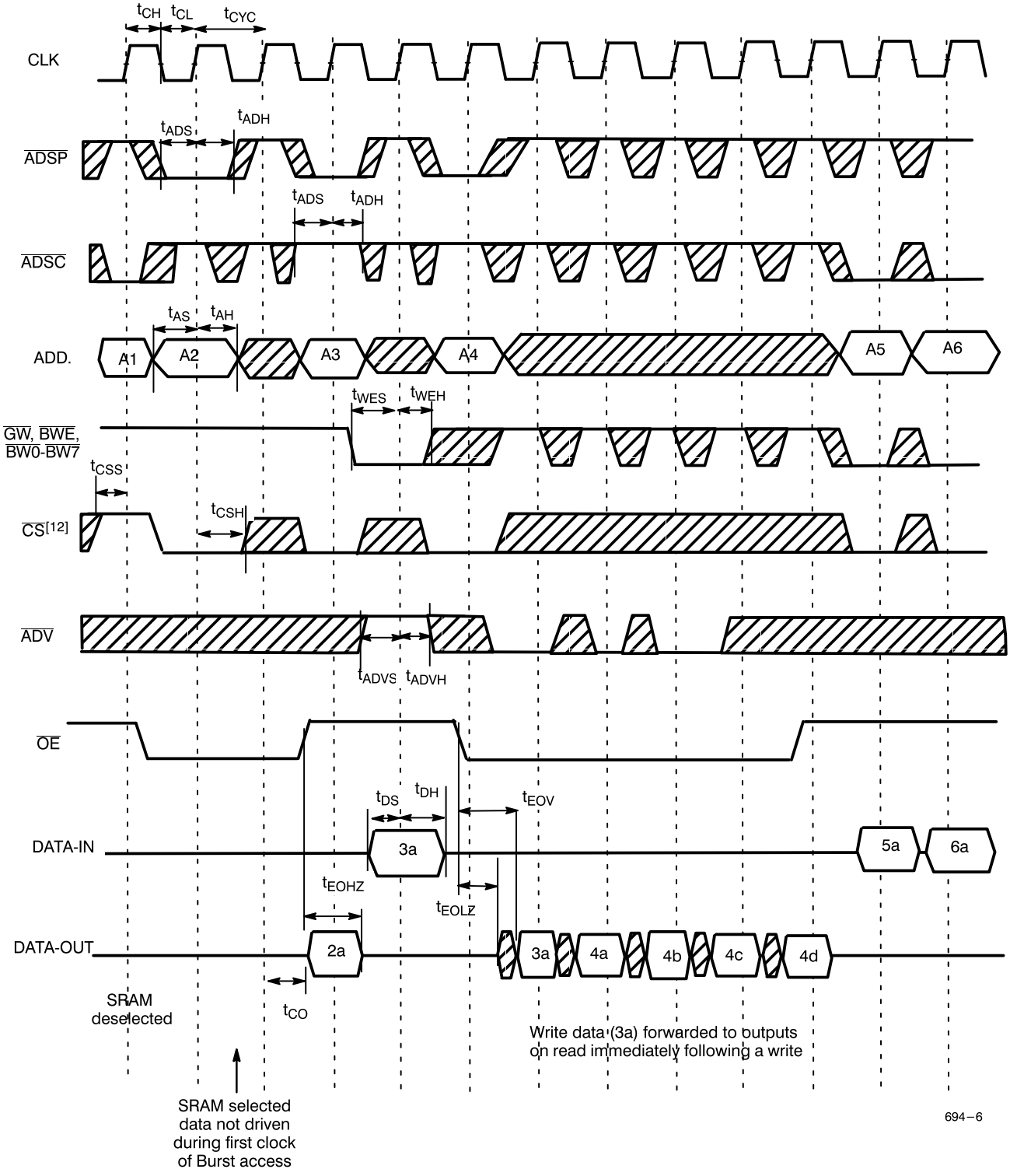
## Switching Waveforms (continued)

### Read/Write Timing



## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 8 | CY82C694−XXX | TBD | 128-Lead Thin Quad Flat Pack | Commercial |
| 10 | CY82C694−XXX | TBD | 128-Lead Thin Quad Flat Pack | Commercial |

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