hC-ZX/hC-VX/ hC-DX

ADVANCED INFORMATION

Pentium™ hyperCache™ Chipset Family

System Features

hC-ZX

- **Zero-cache solution with integrated microcache**
- **CY82C690 Data Path Unit**
- **CY82C691 System Controller**
- **CY82C693/U Peripheral Controller**

hC-VX

- **Value solution with integrated 128-KB two-way set associative pipelined burst SRAM**
- **CY82C692 Data Path Unit**
- **CY82C691 System Controller**
- **CY82C693/U Peripheral Controller**

hC-DX

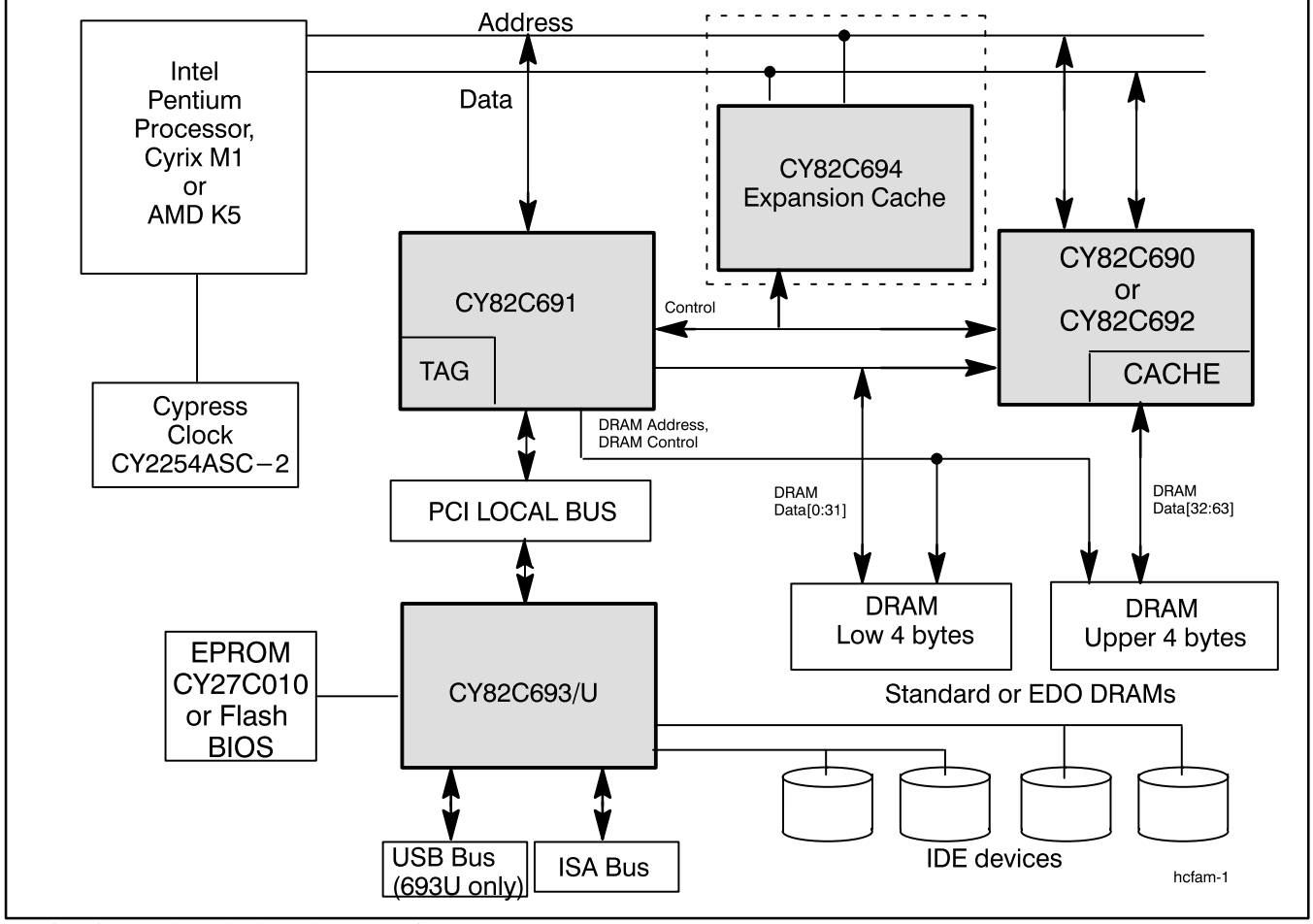
- **Performance solution with 256-KB two-way set associative pipelined burst SRAM**
- **CY82C691 System Controller**
- **CY82C692 Data Path Unit**
- **CY82C693/U Peripheral Controller**
- **CY82C694 Expansion Cache**

System Overview

The hyperCache™ family is a family of three chipsets created to provide flexible solutions for today's PC designs. The hC-ZX, hC-VX, hC-DX Chipsets provide all the functions necessary to implement a 3.3V Pentium-class processor based system with the USB (Universal Serial Bus, PCI (Peripheral Component Interconnect), and the ISA (Industry Standard Architecture) buses. System designers can exploit the advantages of the USB and PCI buses while maintaining access to the large base of ISA cards in the marketplace.

The Cypress hyperCache family offers system designers several key advantages. With only three chips, a complete system can be implemented. Cache can be added up to 1 MB with additional CY82C694 devices in 128-KB increments All chipset solutions are pin-compatible and provide flexible upgrade paths through on-board or external cache modules. Six banks of page-mode or EDO DRAM further increase the system designer's options. The chipset also contains concurrent bus support, PCI enhanced IDE with CD-ROM support, integrated RTC, integrated peripheral control (Interrupts/ DMA), and integrated keyboard controller. This chipset is flexible enough to provide the system designer with many cost/performance/function options to provide an optimum solution for a given design.

System Block Diagram (hC-ZX, hC-VX, hC-DX solutions)



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CY82C691 System Controller

CY82C691 System Controller Features

- **Provides control for the cache, system memory, and the PCI bus**
- **PCI Bus Rev. 2.1 compliant**
- **Supports Pentium™ (ICOMP 735/90, 815/100, etc.), AMD K5, and Cyrix 6x86 (M1) CPUs**
- **Support for WB or WT L1 cache**
- **Supports 3-1-1-1 burst read/write operation at 66, 60, and 50 MHz bus speeds**
- **Supports CPU address pipelining**
- **Support for synchronous or pipelined BSRAMs**
- **Provides power management support through SMM (APM compliant)**
- **Integrated 8Kx21 tag (direct mapped and two-way set associative)**
- **Support for cache sizes up to 1 MB**
- **Supports mixed standard page-mode and EDO DRAMs**
- **Supports the VESA Unified Memory Architecture (VUMA)**
- **Support for standard 72-bit-wide DRAM banks**
- **Supports non-symmetrical DRAM banks**
- **Supports six banks of DRAM (six RAS lines)**
- **Supports DRAM densities up to 16 Mb**
- **Up to 768 MB main memory**
- **Variable drive on DRAM address lines (max. 20 mA)**
- **Provides glueless (0 TTL) system solution**
- **Support for concurrent operation among CPU, cache, DRAM, and PCI**
- **Byte-Merge operation**
- **8 deep PCI post-write/pre-read buffers**
- **Packaged in a 208-pin PQFP**

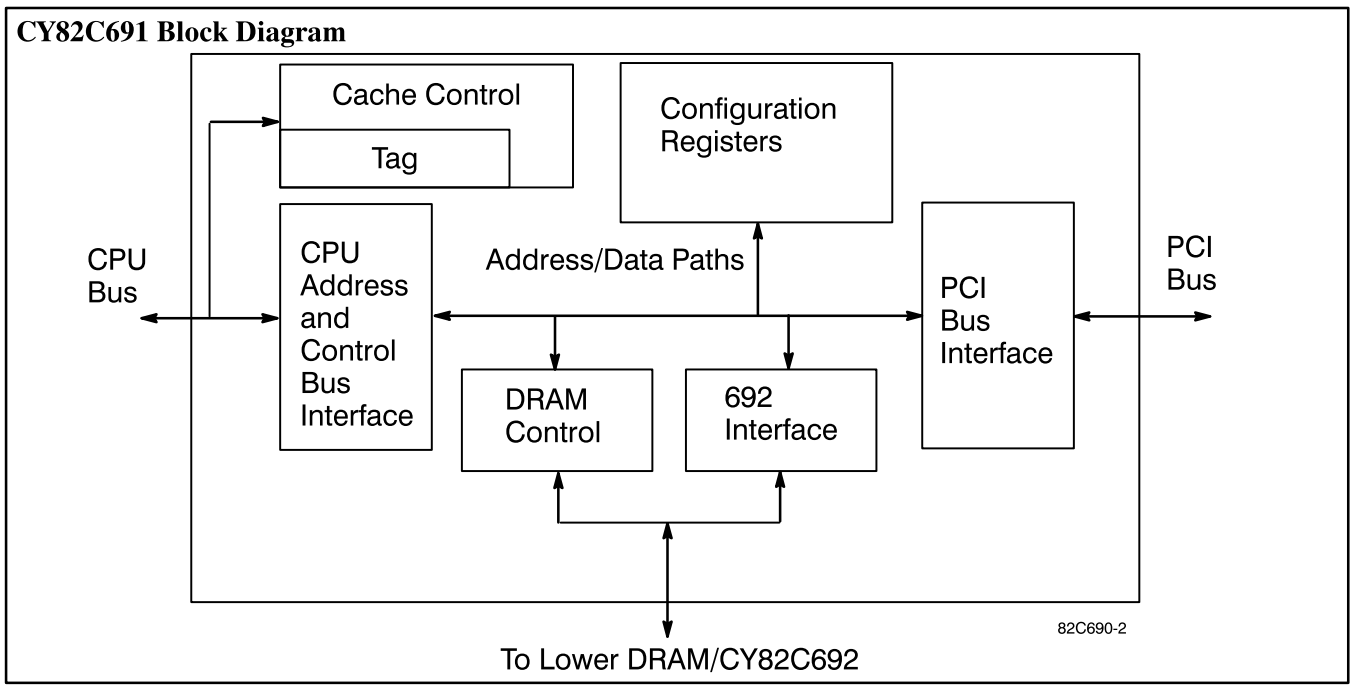
CY82C691 Functional Overview

The CY82C691 System Controller is a highly integrated device. It provides control for the CPU, cache, memory, and PCI. The memory controller supports up to 768 MB of main memory with standard page-mode DRAMs or EDO DRAMs. The cacheable range can be configured to cover the entire DRAM main system memory space. Support is provided for up to 6 banks of 72-bit wide DRAM SIMMs (parity checking/generation is provided by the CY82C692 or CY82C690). Asymmetrical DRAM banks are also supported. 20 mA outputs with programmable drive are provided on the DRAM lines, thus eliminating the need for external buffers.

The cache controller supports a look-aside (parallel) cache with synchronous or pipelined burst SRAMs. Asynchronous SRAMs are not supported. Burst reads and writes to and from the cache with 3-1-1-1 timing are maintained even at 66 MHz. The CY82C691 integrates an 8Kx21 tag-RAM to further reduce system cost. The tag can be configured to be either direct mapped or two-way set associative. Cache sizes can range from 128 KB to 1 MB in 128-KB increments. Support is provided for asymmetrical SRAM banks. For example, a 384-KB cache can be configured with the 128-KB cache in the CY82C692 and a 256-KB external expansion cache. For cache bank sizes greater than or equal to 512 KB, the cache is sectored with two lines per sector. Cache coherency with main memory is maintained at all times.

Bus concurrency is supported between the CPU, cache, DRAM, and PCI bus with the use of post-write and pre-read FIFOs. Pentium pipelined addressing and power management features (SMM) are supported. The CY82C691 also supports the Cyrix M1 processor and the AMD K5 processor. The CY82C691 also generates all the control for the CY82C692 or CY82C690 Data Path/Cache chip.

CY82C691 Block Diagram



CY82C690 Data-Path/Integrated Cache for hC-ZX Chipset

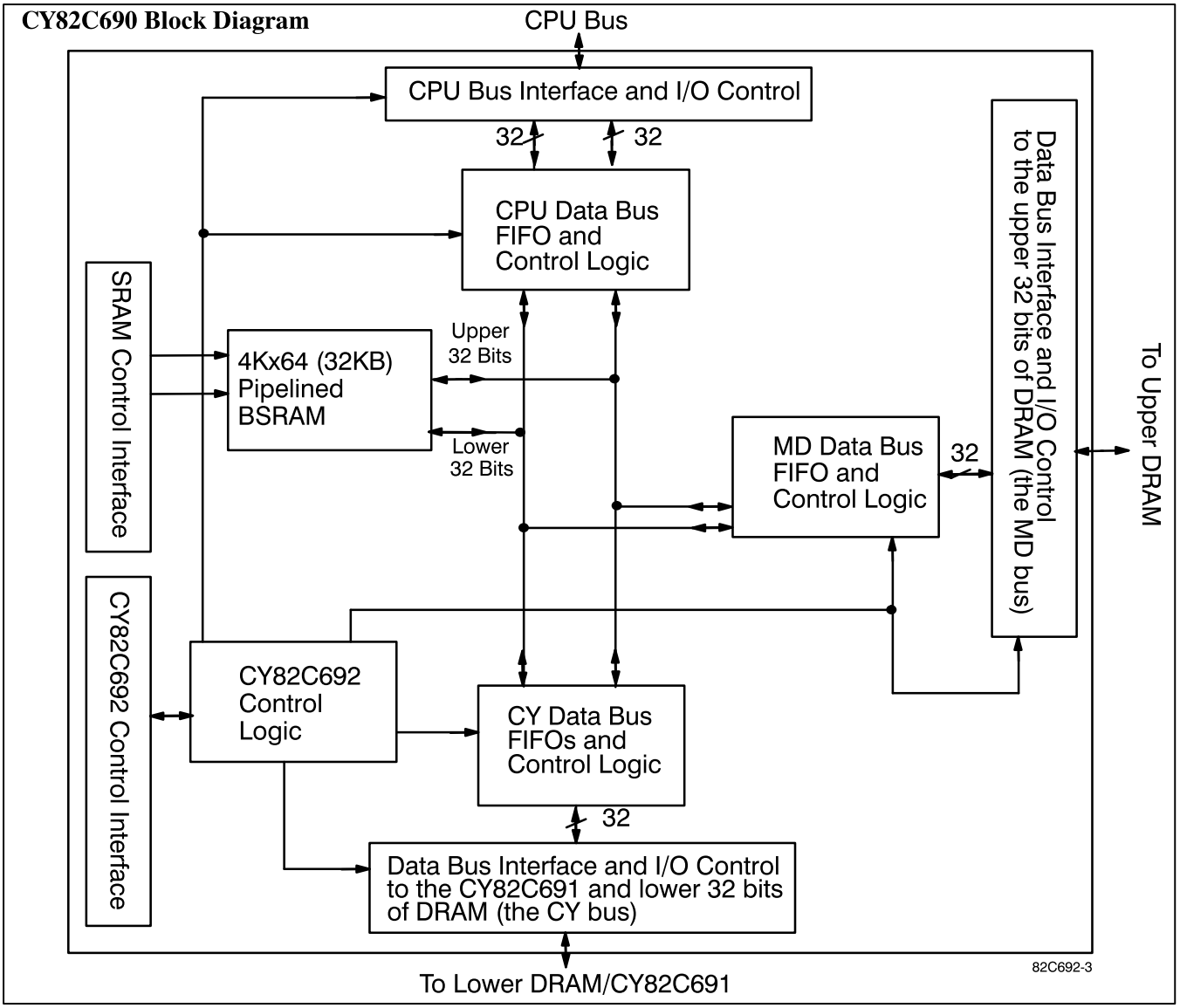
CY82C690 Data Path Features

- Supports all 3.3V Pentium™, AMD K5, and Cyrix M1 CPUs
- Directly interfaces with CY82C691 and CY82C693 to provide high-performance zero cache solution (hC-ZX)
- Provides 64-bit data path between CPU, PCI, and DRAM memory
- Direct interface with the processor and the CY82C691 PCI/Cache/Memory Controller
- 3.3V I/O CPU bus operation
- On-Chip 8-Deep FIFOs support Post-Writing/Pre-Reading PCI data
- Supports Parity checking and generation
- Provides Data steering and Bus size conversion

CY82C690 Integrated Cache Features

- 4K by 64 (32-KB) Integrated Pipelined BSRAM
- Direct-mapped or two-way set associative L2 cache mapping configurations
- Two-bit wraparound counter supporting Intel Burst or Linear burst sequence
- Supports 3-1-1-1 Level 2 cache operation up to 66 MHz bus speed
- Fast Clock-to-Data (T_{CO}) = 8.5 ns
- Synchronous self-timed write to L2 cache BSRAM
- Packaged in a 208-pin PQFP

CY82C690 Block Diagram



CY82C690 Functional Overview

The CY82C690 is a 64-bit data path unit between the DRAM and CPU for the hC-2ZX chipset. The CY82C690 serves two main functions: (1) Provides data steering to/from three different interfaces (CPU bus, the DRAM high or MD bus, and the DRAM low or CY bus), and (2) Provides 32 KB of Level 2 cache with an integrated synchronous pipelined BSRAM. With a clock-to-data valid time (T_{CO})=8.5 ns, 3-1-1-1 burst cycles are supported at bus frequencies up to 66 MHz.

The CY82C690 contains several sets of FIFOs that serve as Pre-Reading/Post-Writing buffers. These buffers are controlled by signals (Control[11:0]) coming from the CY82C691 System Controller. The Pre-Reading/Post-Writing feature enhances system performance by allowing concurrent transactions on the CPU, PCI, and DRAM buses.

The CY82C690 also contains data parity generation/checking logic for all transactions to/from DRAM memory.

The 3.3V CPU bus interface contains an 8-deep, 64-bit wide FIFO. This FIFO is logically broken into two 32-bit FIFOs in order to properly route data and accommodate for bus size conversions. All data going to the CPU data bus must pass through the CPU FIFO.

The DRAM interface is divided between the upper 32 bits and lower 32 bits of data. The upper 32 bits (and parity) are transferred on the MD bus. The MD bus is a dedicated connection between the CY82C690 and the upper 32 bits of DRAM memory. The lower 32 bits of data (and parity) are transferred on the CY bus. The CY bus also serves as the data path connecting the PCI bus (via the CY82C691) to the CPU.

The CY82C690 contains an integrated Level 2 cache configured as a 4Kx64 (32-KB) synchronous pipelined BSRAM. The BSRAM can be used as either a direct mappped or two-way set associative L2 cache. The BSRAM is controlled by dedicated control signals coming from the CY82C691 System Controller. The L2 cache can be expanded with additional CY82C694s (Cypress's 16Kx64 pipelined BSRAM in a 128-pin TQFP) or additional discrete BSRAMs (synchronous or pipelined). Each bank must be comprised of the same type of BSRAM. L2 cache sizes of up to 1 MB are supported, with a maximum of 512 KB per bank.

CY82C692 Data-Path/Integrated Cache for hC-VX/hC-DX Chipsets

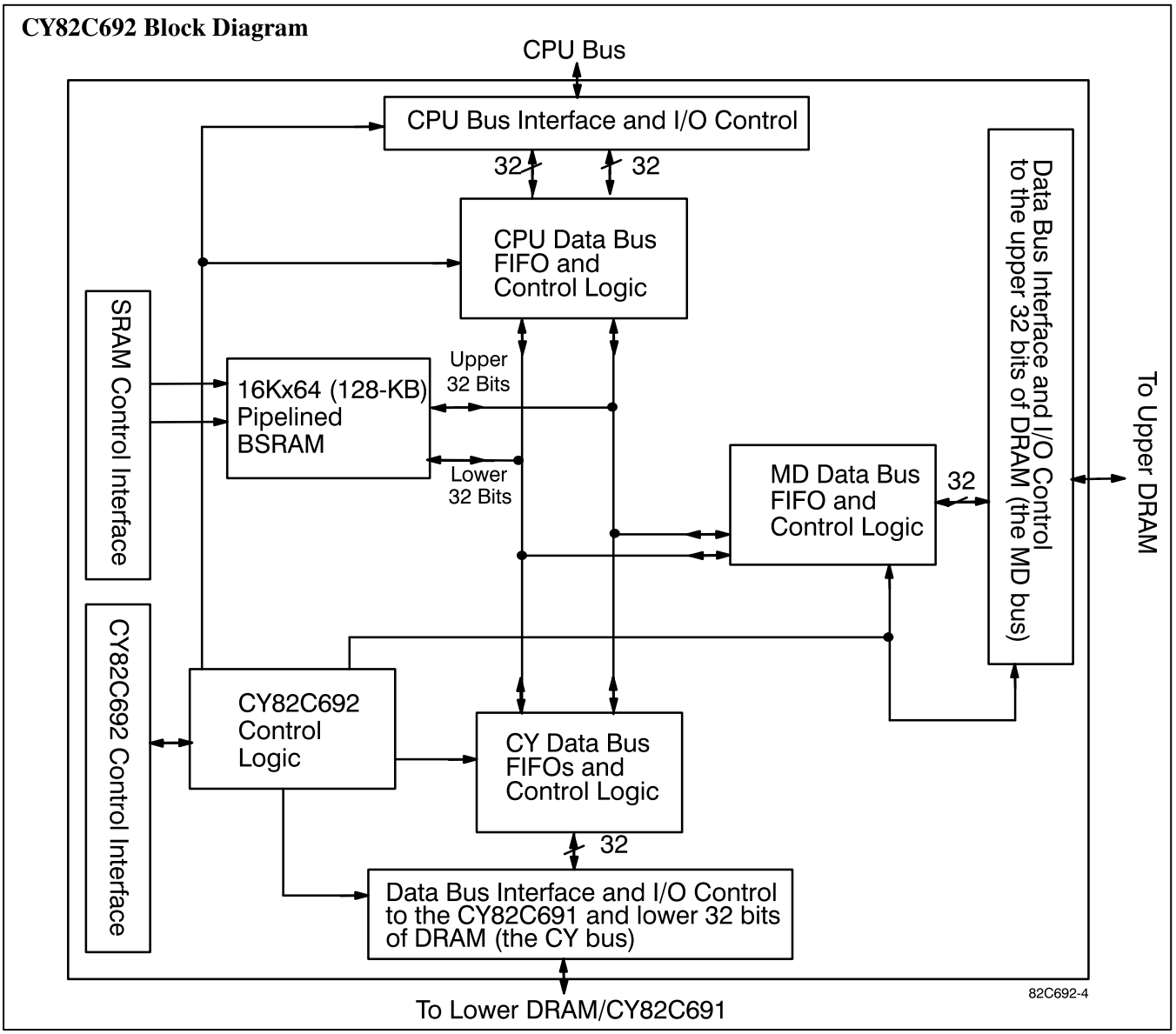
CY82C692 Data Path Features

- Supports all 3.3V Pentium™, AMD K5, and Cyrix M1 CPUs
- Directly interfaces with CY82C691 and CY82C693 to provide high-performance three-chip Pentium Chipset system
- Provides 64-bit data path between CPU, PCI, and DRAM memory
- Direct interface with the processor and the CY82C691 PCI/Cache/Memory Controller
- 3.3V I/O CPU bus operation
- On-Chip 8-Deep FIFOs support Post-Writing/Pre-Reading PCI data
- Supports Parity checking and generation
- Provides Data steering and Bus size conversion

CY82C692 Integrated Cache Features

- 16K by 64 (128-KB) Integrated Pipelined BSRAM
- Direct-mapped or two-way set associative L2 cache mapping configurations
- Two-bit wraparound counter supporting Intel Burst or Linear burst sequence
- Supports 3-1-1-1 Level 2 cache operation up to 66 MHz bus speed
- Fast Clock-to-Data (T_{CO}) = 8.5 ns
- Synchronous self-timed write to L2 cache BSRAM
- Packaged in a 208-pin PQFP

CY82C692 Block Diagram



CY82C692 Functional Overview

The CY82C692 is a 64-bit data path unit between the DRAM and CPU for the hC-VX and hC-DX chipsets. The CY82C692 serves two main functions: (1) Provides data steering to/from three different interfaces (CPU bus, the DRAM high or MD bus, and the DRAM low or CY bus), and (2) Provides 128 KB of Level 2 cache with an integrated synchronous pipelined BSRAM. With a clock-to-data valid time (T_{CO})=8.5 ns, 3-1-1-1 burst cycles are supported at bus frequencies up to 66 MHz.

The CY82C692 contains several sets of FIFOs that serve as Pre-Reading/Post-Writing buffers. These buffers are controlled by signals (Control[11:0]) coming from the CY82C691 System Controller. The Pre-Reading/Post-Writing feature enhances system performance by allowing concurrent transactions on the CPU, PCI, and DRAM buses.

The CY82C692 also contains data parity generation/checking logic for all transactions to/from DRAM memory.

The 3.3V CPU bus interface contains an 8-deep, 64-bit wide FIFO. This FIFO is logically broken into two 32-bit FIFOs in order to properly route data and accommodate for bus size conversions. All data going to the CPU data bus must pass through the CPU FIFO.

The DRAM interface is divided between the upper 32 bits and lower 32 bits of data. The upper 32 bits (and parity) are transferred on the MD bus. The MD bus is a dedicated connection between the CY82C692 and the upper 32 bits of DRAM memory. The lower 32 bits of data (and parity) are transferred on the CY bus. The CY bus also serves as the data path connecting the PCI bus (via the CY82C691) to the CPU.

The CY82C692 contains an integrated Level 2 cache configured as a 16Kx64 (128-KB) synchronous pipelined BSRAM. The BSRAM can be used as either a direct mappped or two-way set associative L2 cache. The BSRAM is controlled by dedicated control signals coming from the CY82C691 System Controller. The L2 cache can be expanded with additional CY82C694s (Cypress's 16Kx64 pipelined BSRAM in a 128-pin TQFP) or additional discrete BSRAMs (synchronous or pipelined). Each bank must be comprised of the same type of BSRAM. L2 cache sizes of up to 1 MB are supported, with a maximum of 512 KB per bank.

CY82C693 Peripheral Controller

CY82C693 Features

- **PCI to ISA bridge**
- **PCI Bus Rev. 2.1 compliant**
- **Supports up to 5 additional PCI masters including the CY82C691**
- **Integrated DMA controllers with Type A, B, and F support.**
- **Integrated Interrupt controllers**
- **Integrated timer/counters**
- **Integrated Real-Time-Clock with 256 bytes of battery-backed SRAM (14 bytes of clock RAM and 242 bytes of CMOS scratch RAM)**
- **Write-only Register Shadowing**
- **Integrated Dual-Channel enhanced IDE controller with**
  - **— PCI bus mastering**
  - **— CD ROM support**
  - **— PIO modes 0 through 4 operation**
  - **— Single-word and Multi-word DMA modes 0 through 2**
- **Integrated Keyboard Controller**
- **APM compliant power management support through SMM or under hardware control.**
- **Flash PROM support with Write-protection**
- **Power-on reset circuitry**
- **QuietBus™ support for the PCI and ISA bus interfaces for better noise immunity**
- **General-purpose I/O pins and registers**
- **Zero TTL system operation**
- **Provides PCI-ISA/ISA-PCI/ IDE-PCI/PCI-IDE post writing**
- **Provides ISA-PCI pre-reading**
- **5 pins reserved for USB support**
- **Packaged in a 208-pin PQFP**

CY82C693 Functional Overview

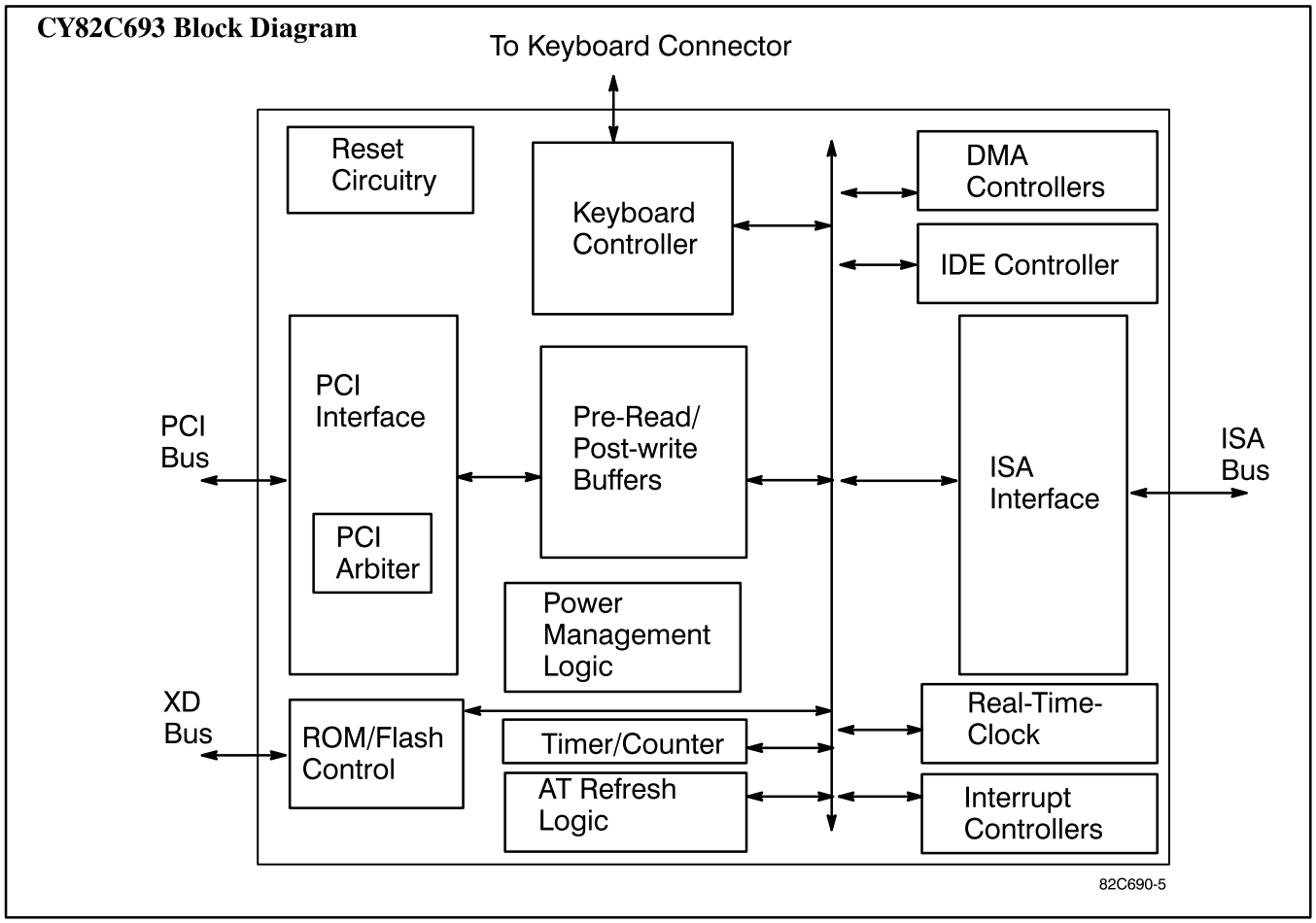
The CY82C693 is a highly integrated peripheral solution for PCI-based motherboards. The CY82C693 provides a bridge between the PCI bus, the ISA bus, and the IDE peripherals. The CY82C693 provides support for 6 PCI masters. In addition, the CY82C693 integrates several key peripherals, including an 8042-compatible keyboard controller, support for a PS/2 mouse, a real time clock with 256 bytes of battery-backed RAM, two 8237-compatible DMA controllers, and a dual-channel enhanced IDE controller. For added flexibility, the keyboard controller can accept custom code.

The CY82C693 also contains the logic to support AT refresh cycles on the ISA bus and provides flexible power management with 5 timers and 10 programmable event detectors. Additional features include two general-purpose I/Os and support for 4 MB of Flash ROM.

USB Support

The CY82C693 has 5 pins reserved for USB support. The logic for an open HCI-compliant USB host controller and 2 USB ports will be incorporated in the CY82C693U (the USB version of the CY82C963).

CY82C693 Block Diagram



CY82C694 128-KB hyperCache™ Chipset Expansion RAM

CY82C694 Features

- **Interfaces directly to hyperCache™ Chipset (CY82C691/692/693) at 66 MHz with 0 wait states**
- **Fully registered inputs and outputs in Pipelined mode operation**
- **16K x 64 common I/O architecture**
- **I/Os capable of 3.3V operation**
- **Fast Clock-to-output times**
  — **T_{CO}=8.5 ns (for 66-MHz systems)**
- **User selectable Two-bit wraparound burst counter supporting Intel™ interleaved or linear bust sequences**
- **Separate processor and controller address strobes**
- **Synchronous self-timed writes**
- **Asynchronous output enable**
- **14 mm x 20 mm 128-pin TQFP package**

CY82C694 Functional Overview

The CY82C690 is a 16K by 64 synchronous/pipelined cache Burst SRAM (BSRAM) designed to support a zero wait state secondary cache with minimal glue logic.

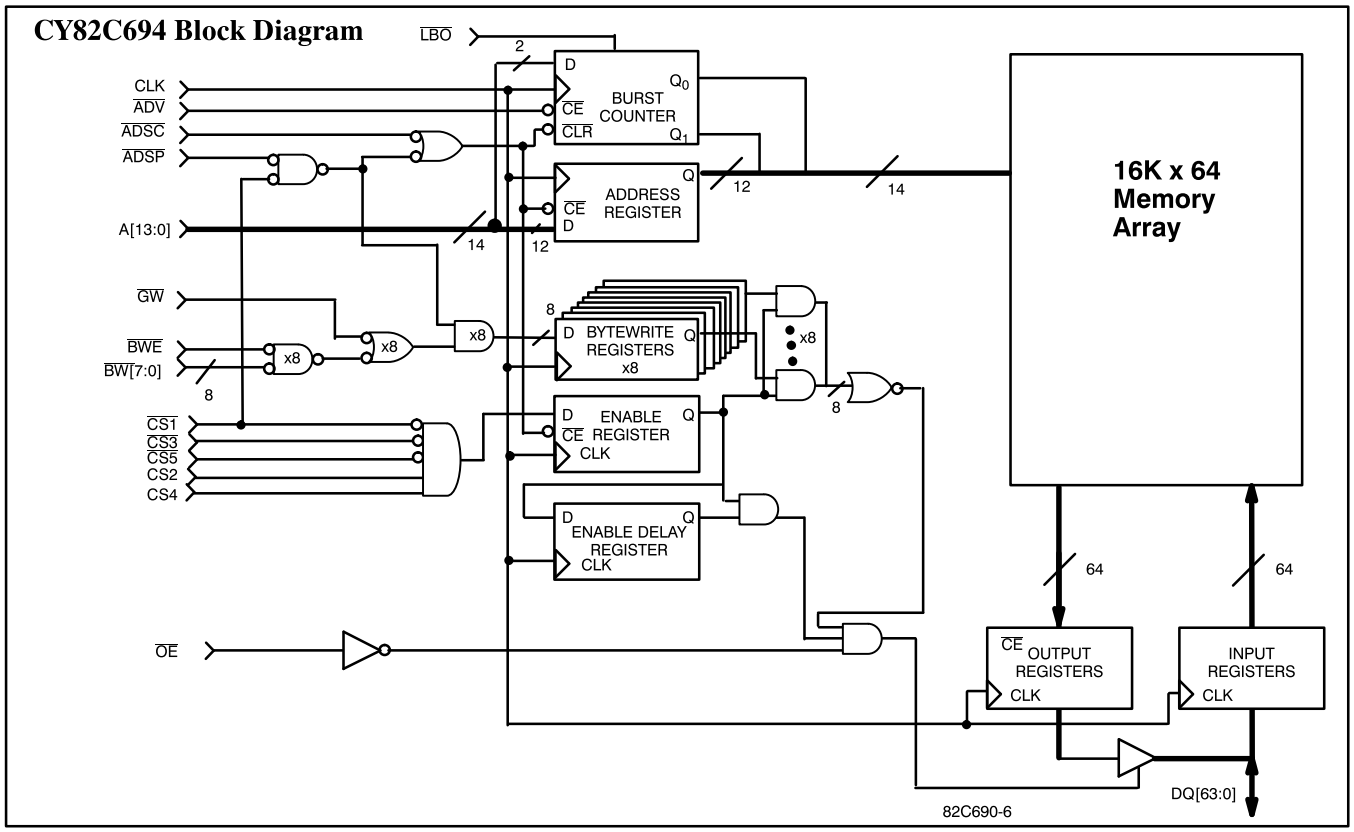
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise in pipelined mode (T_{CO}) is 8.5 ns. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

The CY82C694 supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486 processors. The linear burst sequence is suited for processors that utilize a linear burst sequence, such as the Cyrix M1. The burst order is user selectable, and is determined by sampling the $\overline{LBO}$ (Linear Burst Order) input. Accesses can be initiated with either the processor address strobe ($\overline{ADSP}$) or the controller address strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW}0-7$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all eight bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Five synchronous chip selects ($\overline{CS1}$, $\overline{CS3}$, $\overline{CS5}$, CS2, CS4) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output three-state control. $\overline{ADSP}$ is ignored if $\overline{CS1}$ is HIGH.

CY82C694 Block Diagram



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