Chipset for Pentium-Based PCs Integrates Cache to Boost Performance, Cut System Cost

Historically, as the density of integrated circuits has increased, the chip count in personal computers has decreased. And no one seriously doubts that as process technology continues to evolve, ultimately a single-chip solution will emerge. Until that time, however, chipsets integrating more and more functionality will continue to form the nucleus of a PC.

At the heart of every PC is its central processor unit (CPU). It is clear that, for the foreseeable future, the Pentium and Pentium-compatible processors will be the dominant microprocessors. Over 30 million Pentium processors were sold in 1995, and projections for 1996 show Pentium sales reaching 60 million units.

This rapid growth will be accompanied by an equally rapid growth in the demand for static RAMs (SRAMs) to be used as cache memory in Pentium-based systems. SRAM cache allows a PC's slower DRAM (dynamic RAM) main memory to keep pace with themuch faster Pentium processor. For this and other performance-related reasons, SRAM cache has become a standard feature in almost all Pentium designs.

The typical PC configuration today consists of a central processor (e.g., a Pentium CPU carrying a small first-level, or primary, cache); a PC chipset in three or four large plastic quad flat packages (PQFPs); a reletively large second-level, or secondary, cache; main memory comprised of DRAMs; a clock generator chip; a BIOS (Basic Input/Output System) PROM (programmable read-only memory); and additional TTL system logic chips. (Figure 1.) System providers are driven by continually increasing competitive pressure to reduce system cost while providing higher system performance with lower power consumption, to reduce motherboard size, and to get new models to market fast.

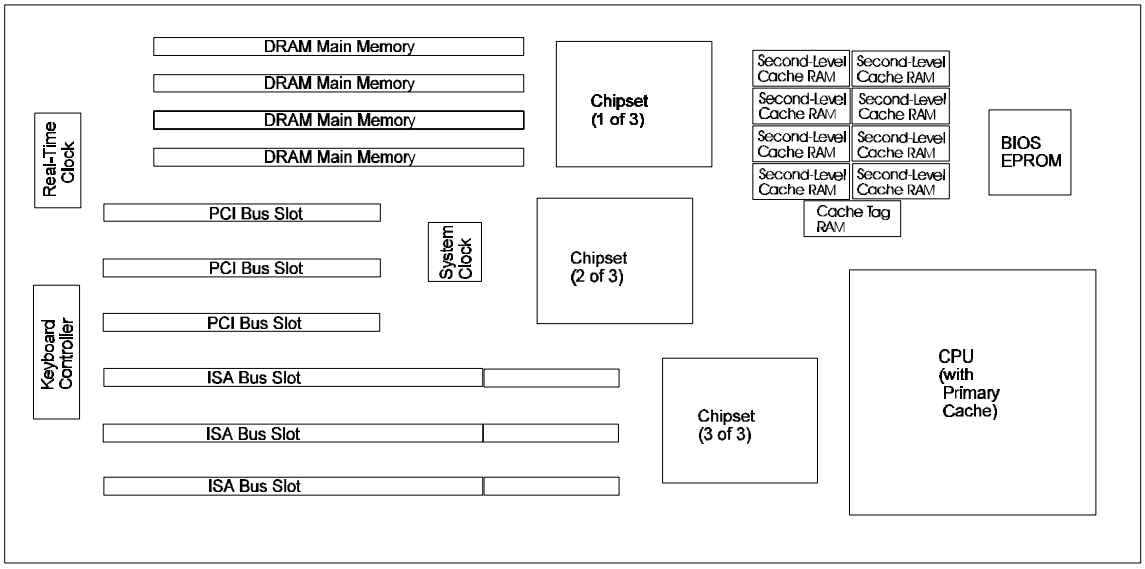

Figure 1. This is a typical layout for a modern PC's motherboard using traditional components, especially in the areas of the chipset and the secondary cache.

The hyperCache Chipset Solution

Cypress's hyperCache Chipset is a full-featured, high-performance chipset for Pentium-based systems that offers PC designers a very effective way to meet their competitive pressures. Cypress has used its expertise in SRAM and logic design, clock chips, chipset architecture, and fine-geometry CMOS fabrication to design and build a chipset unlike any other. The hyperCache Chipset integrates both 16-K x 64-bit-wide secondary cache -- the widest SRAMs available -- and cache tag SRAMs. It provides all the functions necessary to implement a Pentium-based system using the PCI (Peripheral Component Interconnect) bus and the ISA (Industry Standard Architecture) bus.

The hyperCache Chipset's integrated SRAM immediately protects the designer against future SRAM shortages and product incompatibilities -- since the SRAM is in the chipset. Its extremely broad, advanced-functionality architecture provides many desirable features that enhance system performance -- e.g., it allows system designers to exploit the superior features of the PCI bus while maintaining access to the large base of ISA cards available in the marketplace.

Comprising a CY82C691 System Controller chip, a CY82C692 Data Path/Cache chip, and a CY82C693 Peripheral Controller chip (Figure 2), the hyperCache Chipset provides system designers with several key advantages.

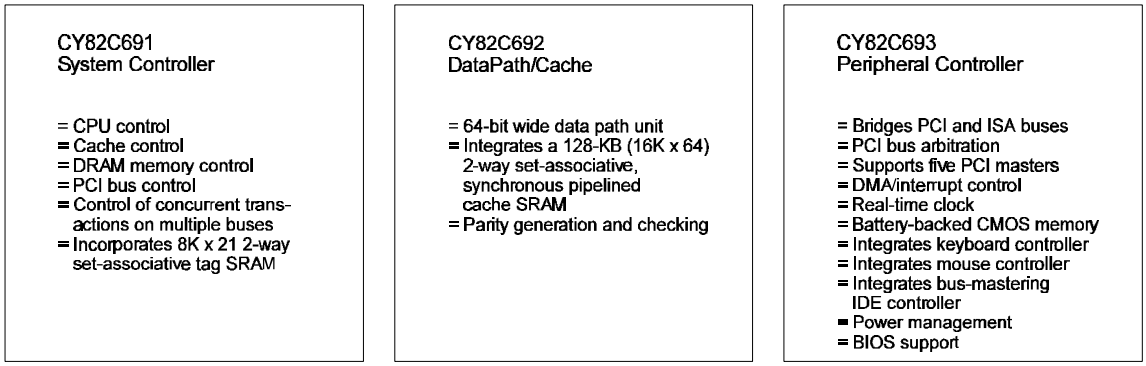

Figure 2. The three chips that comprise the Cypress hyperCache Chipset, and the functionality of each.

With only three chips, for instance, the designer can implement a complete 128-kilobyte, 2-way set-associative, write-back, synchronous, pipelined secondary cache. This cache will perform at a level very close to that of a 256-kilobyte synchronous, pipelined cache. And the designer can increase cache size up to 1 megabyte with additional SRAMs -- such as the Cypress CY82C694, a 16-K x 64 cache SRAM that is actually the SRAM portion of the CY82C692 Data Path/Cache chip.

The hyperCache Chipset supports both write-through and write-back caches in the fastest Pentium-based systems -- i.e., those with external CPU bus speeds to 66 MHz. It allows the designer to specify a main memory of up to 768 MBytes of page-mode and/or EDO (Extended Data Out) DRAMs (in six banks of 16-Mbits x 64 each), for the maximum breadth of system options. Additional features of the chipset include support of concurrent bus operation (simultaneous, independent operation of the CPU bus, cache bus, DRAM bus, and PCI bus); an integrated Enhanced IDE (Integrated Drive Electronics) controller that supports up to four IDE devices (hard and CD-ROM drives)

and increases overall system performance through a PCI bus-mastering capability that frees the CPU from controlling disk accesses; an integrated real-time clock; integrated interrupt/DMA control; and an integrated keyboard/mouse controller. Making all these features available in a three-chip set simplifies the system design task enormously. The hyperCache Chipset also offers its users a cost savings of about 30%, a motherboard area savings of about 10%, and a shorter design cycle.

hyperCache Chipset Provides an Optimum Cache

The factors governing cache performance are the size of the cache, the type of SRAM used, and the organization of the SRAM. With respect to size, the larger the cache the better, in general; the hyperCache Chipset is expandable from 128 KBytes to 1 MByte in 128-KByte increments.

With respect to organization, the hyperCache Chipset's integrated cache is a 2-way set-associative design, which achieves higher performance than the commonly used direct-mapped approach. In a direct-mapped cache, every memory address generated by the CPU has only one possible location inside the cache. With a 2-way set-associative organization, however, there are two locations within the cache at which an address coming from the CPU can be found. Thus, a 2-way set-associative cache achieves higher performance than a direct-mapped cache because it doubles the probability of a cache hit. Published results(1) of cache miss rates for direct-mapped and 2-way set-associative caches show that, using the same type of SRAM, the performance of a 2-way set-associative cache is about the same as that of a direct-mapped cache twice its size.

Note that a 2-way set-associative cache requires more complex cache controller circuitry than the simpler direct-mapped cache, which is why the latter is so widely used in current systems. However, the high integration level of the hyperCache Chipset easily provides the additional logic needed to implement the circuitry of a 2-way set-associative cache controller.

The importance of the 128-KB cache provided on the CY82C692 Data Path/Cache chip and the 8K x 21 cache tag SRAM integrated into the CY82C691 Controller chip can not be overstated. Cache tag SRAM -- a seldom discussed component of secondary cache memory -- is the "directory" of the secondary cache subsystem: it holds information about where in main memory the data in the cache originated. Thus, all cache operations must wait until the tag completes its search -- which means that any high-speed secondary cache worthy of its name must incorporate a very high-speed tag SRAM, which the hyperCache Chipset does. The integrated cache and cache tag SRAMs are what make possible the earlier-mentioned advantages of the hyperCache Chipset -- higher performance at lower cost, and reduced power consumption and board space. Important additional advantages brought by the high level of integration are reduced system loading and lowered system noise.

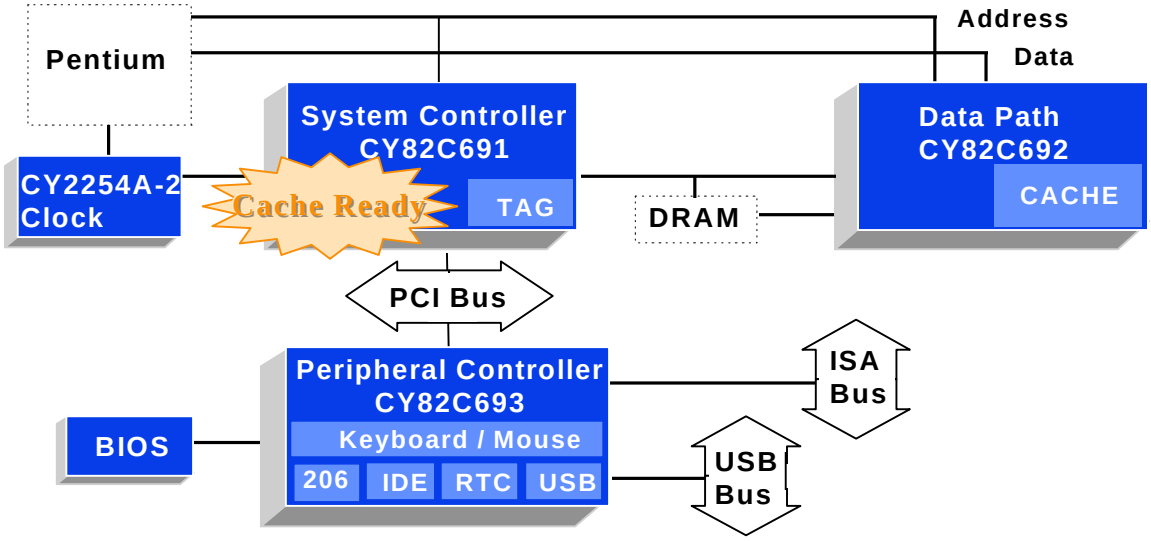

Figure 3. This is the block diagram of a typical hyperCache Chipset-based PC. The CY82C692 Data Path/Cache chip provides a 128-kilobyte secondary cache via its incorporated 16-Kbit x 64 cache SRAM. The hyperCache Chipset permits a secondary cache to be increased to 1 megabyte by adding SRAM in 128-kilobyte increments. A suitable SRAM for such use is Cypress's CY82C694, a 16-Kbit x 64-bit-wide device.

Other Chipset Features

Besides providing a bridge between a PC's ISA and PCI buses, the hyperCache Chipset also has a bus arbitration capability, supporting up to five PCI masters. Some other features of special interest are Cypress-proprietary QuietBus logic, which reduces PCI and ISA bus noise and electromagnetic radiation; power management logic, which through hardware and software provides a "green" Energy Star-compliant PC; direct drive of the ISA bus and DRAM signals, which eliminates the need for external TTL logic ICs; and support of both conventional and flash BIOS ROM, with write protection for a flash BIOS.

Real-time-clock and keyboard/mouse controller functions typically are absent from most chipsets on the market today; they usually are implemented using either two separate chips or a costly high-end super-I/O chip. In contrast, the hyperCache Chipset contains a complete time-of-day clock with alarm, hundred-year calendar, programmable periodic interrupt generator, and 256 bytes of battery-backed CMOS RAM for storage of system and clock data. The hyperCache Chipset also offers all the functions of an 8042 keyboard controller, including internally selectable frequencies from 6 to 16 MHz and IBM PS/2 mouse compatibility. The keyboard controller can be disabled if a custom external keyboard control solution is desired -- all the signals needed to control and interface to an external keyboard controller are multiplexed with existing keyboard interface signals.

# # #

1. John L. Hennessy and David A. Patterson, Computer Architecture: A Quantitative Approach (San Mateo, Calif.: Morgan Kaufmann Publishers, 1990), Chapter 8.