PRELIMINARY

CY2071
CY2081

Clock Generators for PC Peripherals

Features

- **Clock generators for PC peripherals such as modems, disk, tape, and CD-ROM drives**
- **Three configurable clock outputs**
  - **— CY2071 output frequencies must be related**
  - **— CY2081 output frequencies need not be related**
- **Outputs ranging from 500 kHz to 100 MHz (5V) and up to 80 MHz for 3.3V operation**
- **Phase-locked loop oscillator input derived from external crystal (10 MHz to 25 MHz) or external reference clock (1 MHz to 30 MHz)**
- **3.3V or 5V operation (factory configured)**
- **EPROM configurable for quick availability.**
- **8-pin 150-mil packaging achieves minimum footprint for space-critical applications**
- **Sophisticated internal loop filter requires no external components or manufacturing tweaks as commonly required with external filters**

Functional Description

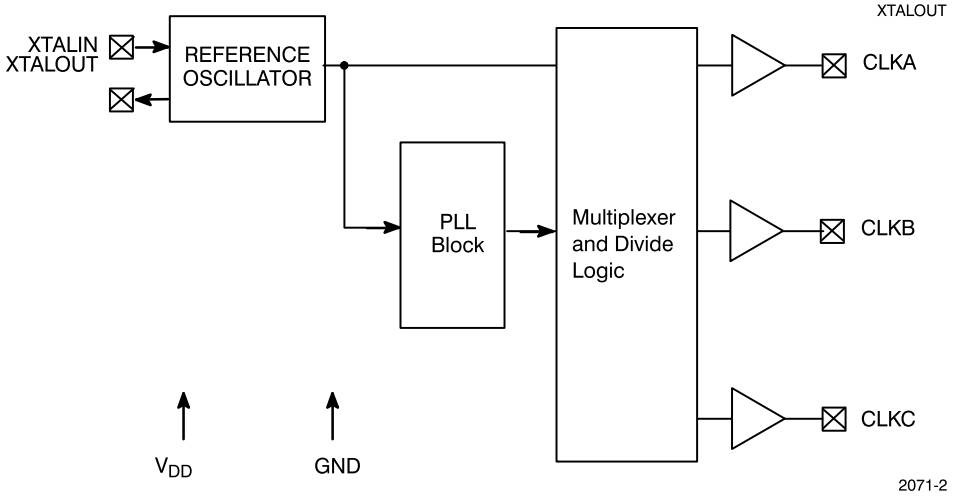
The CY2071 and CY2081 are clock generators designed for PC peripherals such as modems, and hard disk, tape, and CD-ROM drives. Both devices offer three configurable clock outputs in an 8-pin 150-mil SOIC package and can operate off either a 3.3V or 5V power supply. The on-chip reference oscillator is designed for 10 MHz to 25 MHz crystals. Alternatively, an external reference clock of frequency between 1 MHz and 30 MHz can be used. An active-HIGH Output Enable three-states the outputs when deasserted.

The CY2071 outputs three configurable clocks: CLKA, CLKB, and CLKC. Their frequencies must have a Least Common Multiple (LCM) between 20 and 200 MHz. The CY2081 outputs three clocks: CLKA, CLKB, and CLKC, whose frequencies can possess any value within the specified range. Additionally, in both devices, the reference frequency can be obtained on outputs CLKA and CLKB.

The CY2071 and CY2081 can replace multiple Metal Can Oscillators (MCO) in a synchronous system, providing cost and board space savings to the manufacturer. Hence, these devices are ideally suited for applications that require multiple, accurate, and stable clocks synthesized from low-cost generators in small packages. A hard disk drive is an example of such an application. In this case, CLKA drives the PLL in the Read Controller, while CLKB and CLKC drive the MCU and associated sequencers.

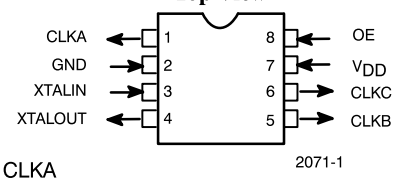
Consider using the CY2291/2 for applications that require more than three output clocks.

Logic Block Diagram



Pin Configuration

SOIC
Top View



Pin Summary

Name	Number	Description
CLKA	1	Configurable clock output
GND	2	Ground
XTALIN[1]	3	Reference Crystal Input or External Reference Clock Input
XTALOUT[1,2]	4	Reference Crystal Feedback
CLKB	5	Configurable clock output
CLKC	6	Configurable clock output
V_{DD}	7	Voltage Supply
OE	8	Active-HIGH Output Enable

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to V_{DD}+0.5V

Storage Temperature ..... −65°C to +150°C

Max. Soldering Temperature (10 sec) ..... 260°C

Junction Temperature ..... 150°C

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions[3]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Digital Supply Voltage	4.5 (3.0)	5.5 (3.6)	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Load Capacitance		25 (15)	pF
f_{REF}	External Reference Crystal	10.0	25.0	MHz
	External Reference Clock[4, 5]	1.0	30.0	MHz

Electrical Characteristics V_{DD} = 5V (3.3V) ±10%, T_A = 0°C to +70°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA			0.4	V
V_{IH}	HIGH-Level Input Voltage[6]	Except Crystal Pins	2.0			V
V_{IL}	LOW-Level Output Voltage[6]	Except Crystal Pins			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD} − 0.5V		<1	10	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V		<1	10	µA
I_{OZ}	Output Leakage Current	Three State Outputs			250	µA
I_{DD}	V_{DD} Supply Current[7]	V_{DD} = V_{DD} max. 5V (3.3V) operation, C_L = 25 pF (15 pF)		40 (24)	60 (40)	mA

Notes:

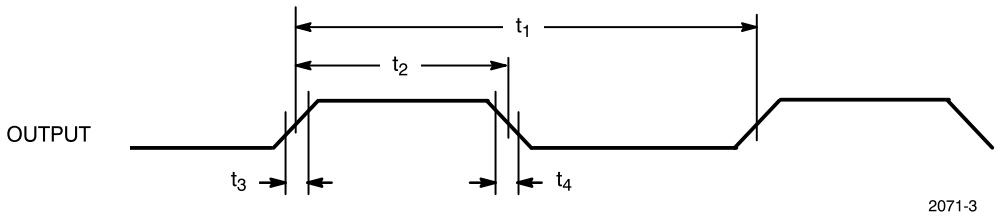
1. For best accuracy, use a parallel-resonant crystal, C_L=17 pF.
2. Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to an external crystal).
3. Electrical parameters are guaranteed with these operating conditions. Values for 3.3V operation are shown in parentheses.
4. External input reference clock must have a duty cycle between 40% and 60%, measured at V_{DD}/2.
5. Please refer to application note “Crystal Oscillator Topics” for information on AC-coupling the external input reference clock.
6. Xtal inputs have CMOS thresholds.
7. Load = max, typical configuration, f_{REF} = 14.318 MHz. Other configurations will vary.

Switching Characteristics[8]

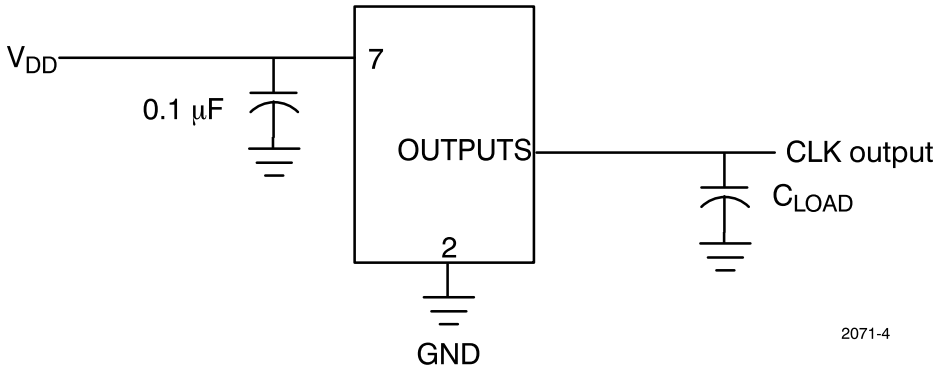
Parameter	Name	Description	Min.	Typ.	Max.	Unit
t_1	Output Period[9]	Clock output range, 5V operation	10 [100 MHz]		2000 [500 KHz]	ns
t_1	Output Period[9]	Clock output range, 3.3V operation	12.5 [80 MHz]		2000 [500 KHz]	ns
t_{1A}	Clock Jitter	Peak-to-peak period jitter (t_1 max. − t_1 min.), % of clock period ($f_{OUT} \leq 16$ MHz)		< 2	5	%
t_{1B}	Clock Jitter	Peak-to-peak period jitter (16 MHz ≤ $f_{OUT} \leq 50$ MHz)			700	ps
t_{1C}	Clock Jitter	Peak-to-peak period jitter ($f_{OUT} \geq 50$ MHz)			500	ps
	Output Duty Cycle[10]	Duty cycle for outputs at C_L=25 pF (15 pF), defined as $t_2 \div t_1$[11]	40%	50%	60%	
t_3	Rise time	Output clock rise time[12] at C_L=25 pF (15 pF at 3.3V operation)			5	ns
t_4	Fall time	Output clock fall time[12] at C_L=25 pF (15 pF at 3.3V operation)			4	ns

Switching Waveforms

All Outputs Duty Cycle and Rise/Fall Time



Test Circuit



Note:
8. Guaranteed by design, not 100% tested.
9. Applies to CLKA and CLKB. Output ranges for CLKC are 2.0 MHz to 50 MHz (5V) and 2.0 MHz to 40 MHz (3.3V).
10. Reference Output duty cycle depends on XTALIN duty cycle.
11. Measured at 1.4V.
12. Measured between 0.4V and 2.4V.

Ordering Information

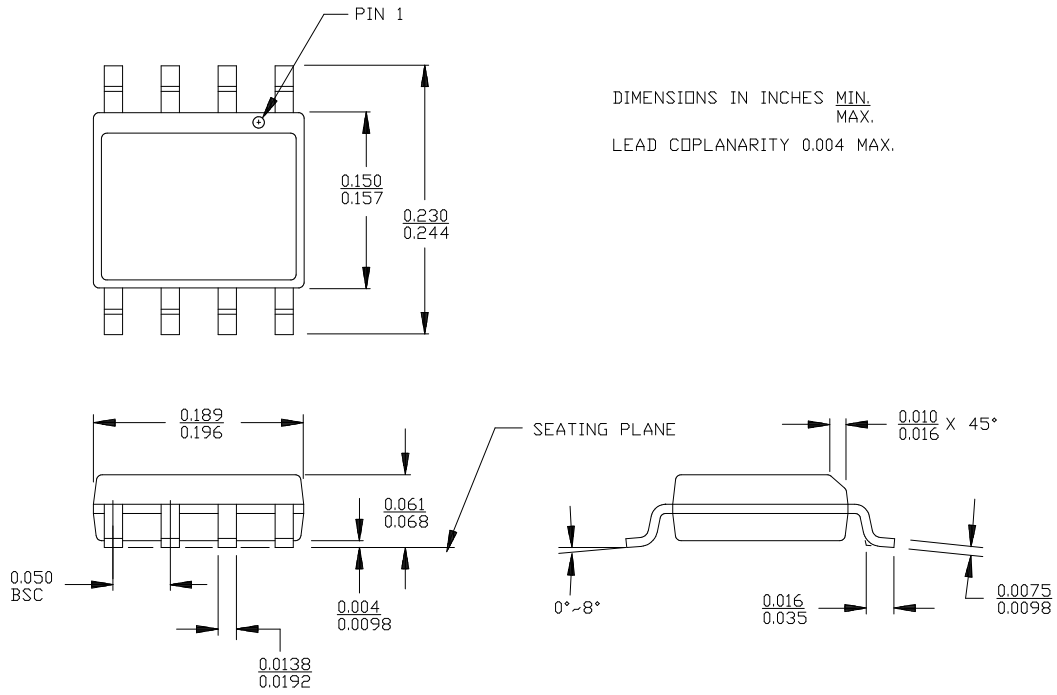
Ordering Code	Package Name	Package Type	Operating Range
CY2071SC−XX	S8	8-Pin (150-Mil) SOIC	Commercial[13]
CY2081SC−XX	S8	8-Pin (150-Mil) SOIC	Commercial[13]

Note:
13. 0°C to +70°C

Document #: 38−00463

Package Diagrams

8-Lead (150-Mil) SOIC S8



CY2071 CONFIGURATION REQUEST FORM

Customer _____ Engineer _____ FAE/Sales _____

Phone # _____ Fax # _____ Date _____

1. OPERATING VOLTAGE (circle one) **3.3V** **5.0V**

2. INPUT REFERENCE FREQUENCY (Circle one) **Crystal** **External Clock**

Default reference = 14.318 MHz. If a different reference is desired, specify the frequency in the box to the right (must be between 10 MHz and 25 MHz for crystal, 1 MHz and 30 MHz for external clock):

3. OUTPUT CONFIGURATION

Fill in the desired frequencies, specifying kHz or MHz, for each output. Please adhere to the notes at the right. Contact your local Cypress representative for assistance.

CLKA _____

CLKB _____

CLKC _____

Notes:

- Buffered reference clock is available on **CLKA** and **CLKB**.
- **CLKA** and **CLKB** outputs can range from 500 kHz to 100 MHz (80 MHz at 3.3V)
- **CLKC** can range from 2.0 MHz to 50 MHz (40 MHz at 3.3V)
- Make sure that the Least Common Multiple (LCM) of **CLKA**, **CLKB**, and **CLKC** frequencies lies between 20 and 200 MHz.

4. FOR CYPRESS USE ONLY

Customer Configuration	Marking
Date	Quantity

CY2081 CONFIGURATION REQUEST FORM

Customer _____ Engineer _____ FAE/Sales _____

Phone # _____ Fax # _____ Date _____

1. OPERATING VOLTAGE (circle one) **3.3V** **5.0V**

2. INPUT REFERENCE FREQUENCY (Circle one) **Crystal** **External Clock**

Default reference = 14.318 MHz. If a different reference is desired, specify the frequency in the box to the right (must be between 10 MHz and 25 MHz for crystal, 1 MHz and 30 MHz for external clock):

3. OUTPUT CONFIGURATION

Fill in the desired frequencies, specifying kHz or MHz, for each output. Please adhere to the notes at the right. Contact your local Cypress representative for assistance.

CLKA _____

CLKB _____

CLKC _____

Notes:

- Buffered reference clock is available on **CLKA** and **CLKB**.
- **CLKA** and **CLKB** outputs can range from 500 kHz to 100 MHz (80 MHz at 3.3V)
- **CLKC** can range from 2.0 MHz to 50 MHz (40 MHz at 3.3V)

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