PRELIMINARY **CY2250**

Pentium™ and P6 Processor Compatible Clock Synthesizer/Driver

Features

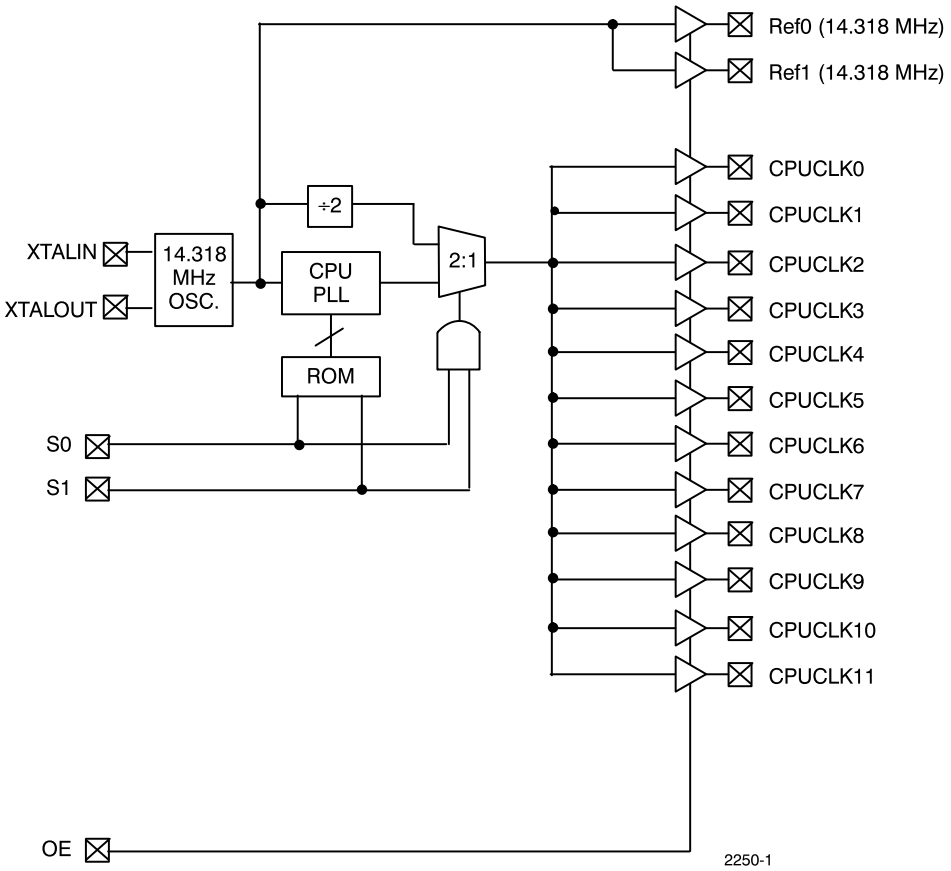
- **Twelve high-drive CPU clock outputs at 50.0, 60.0, and 66.6 MHz, pin-selectable**
- **Two Reference clock outputs at 14.318 MHz**
- **CPU clock jitter ≤ 200 ps cycle-to-cycle**
- **Low skew outputs**
  - **— ≤ 500 ps between CPU clock outputs**
- **Output duty cycle 40% min. to 60% max.**
- **Test mode support**
- **3.3V operation**

Functional Description

The CY2250 is a Clock Synthesizer/Driver chip for the Intel® Pentium™ processor based PC. The part outputs multiple copies of the CPU clock, to serve the requirements of most high-end PCs and servers. The CY2250 has low-skew outputs (≤500 ps between the CPU Clocks). In addition, the CY2250 CPU clock outputs have less than 200 ps cycle-to-cycle jitter. Finally, all the CPU clock outputs meet the 1V/ns slew rate requirement of the Pentium-based system.

The CY2250 accepts a 14.318 MHz reference signal as its input and runs off a 3.3V supply.

Logic Block Diagram



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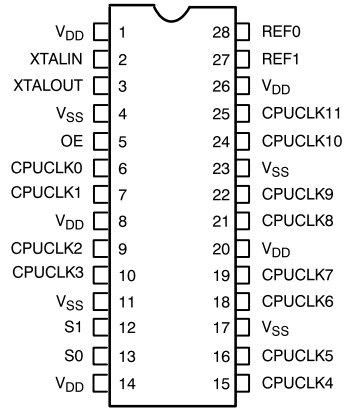
Pin Configuration

Top View
SOIC



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Pin Summary

Name	Number	Description
V_{DD}	1	Voltage supply
XTALIN[1]	2	Reference crystal input
XTALOUT[1]	3	Reference crystal feedback
V_{SS}	4	Ground
OE	5	Output Enable, Active HIGH
CPUCLK0	6	CPU clock output
CPUCLK1	7	CPU clock output
V_{DD}	8	Voltage supply
CPUCLK2	9	CPU clock output
CPUCLK3	10	CPU clock output
V_{SS}	11	Ground
S1	12	CPU clock select input, bit 1
S0	13	CPU clock select input, bit 0
V_{DD}	14	Voltage supply
CPUCLK4	15	CPU clock output
CPUCLK5	16	CPU clock output
V_{SS}	17	Ground
CPUCLK6	18	CPU clock output
CPUCLK7	19	CPU clock output
V_{DD}	20	Voltage supply
CPUCLK8	21	CPU clock output
CPUCLK9	22	CPU clock output
V_{SS}	23	Ground
CPUCLK10	24	CPU clock output
CPUCLK11	25	CPU clock output
V_{DD}	26	Voltage supply
REF1	27	Reference clock output (14.318 MHz)
REF0	28	Reference clock output (14.318 MHz)

Note:
1. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 17 pF.

Function Table

OE	S0	S1	XTALIN Input	CPUCLK [0:11]	Ref. Clock Output
0	X	X	14.31818 MHz	High-Z	High-Z
1	0	0	14.31818 MHz	50.0 MHz	14.318 MHz
1	0	1	14.31818 MHz	60.0 MHz	14.318 MHz
1	1	0	14.31818 MHz	66.6 MHz	14.318 MHz
1	1	1	TCLK[2]	TCLK/2	TCLK

CPU Clock Driver Strength Requirements

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V
- Maximum output impedance: 40Ω measured at 1.5V

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... −0.5 to +7.0V
Input Voltage ..... −0.5V to V_{DD}+0.5
Storage Temperature (Non-Condensing) ... −65°C to +150°C
Max. Soldering Temperature (10 sec) ..... +260°C
Junction Temperature ..... +150°C
Static Discharge Voltage ..... >2000V
(per MIL-STD-883, Method 3015)

Operating Conditions[3]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Ambient Temperature	0	70	°C
C_L	Max. Capacitive Load on CPUCLK REF0 REF1		 20 30 15	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics V_{DD} = 3.3V ±5%, T_A = 0°C to +70°C

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}	High-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OH} = 6 mA	CPUCLK	2.4		V
			I_{OH} = 12 mA	REF0			
			I_{OH} = 8 mA	REF1			
V_{OL}	Low-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OL} = 6 mA	CPUCLK		0.4	V
			I_{OL} = 12 mA	REF0			
			I_{OL} = 8 mA	REF1			
I_{IH}	Input High Current	V_{IH} = V_{DD} − 0.5V			−5	+5	µA
I_{IL}	Input Low Current	V_{IL} = 0.5V			−5	+5	µA
I_{OZ}	Output Leakage Current	Three-state			−10	+10	µA
I_{DD}	Power Supply Current	V_{DD} = 3.465, V_{IN} = 0 or V_{DD}				90	mA

Notes:
2. TCLK is a test clock on the XTALIN input during test mode.
3. Electrical parameters are guaranteed with these operating conditions.

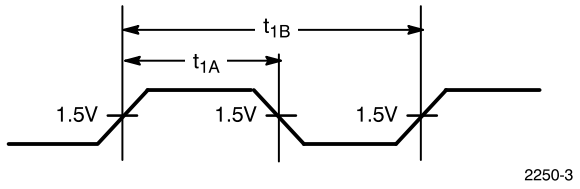
Switching Characteristics[4]

Parameter	Output	Name	Description	Min.	Max.	Unit
t_1	All	Output Duty Cycle[5]	$t_1 = t_{1A} \div t_{1B}$	40%	60%	
t_2	CPUCLK	Output Slew Rate	0.4 to 2.4V	1		V/ns
t_3	REF1, REF0	Rise Time	Measured between 0.4V and 2.4V		4	ns
t_4	REF1, REF0	Fall Time	Measured between 2.4V and 0.4V		4	ns
t_5	CPUCLK	CPU Skew	CPU-CPU clock skew		500	ps
t_6	CPUCLK	Cycle-Cycle Clock Jitter	Clock jitter		200	ps

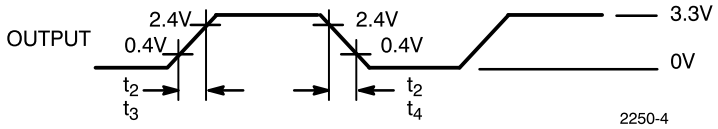
Notes:
4. All parameters specified with outputs fully loaded.
5. Duty cycle is measured at 1.5V.

Switching Waveforms

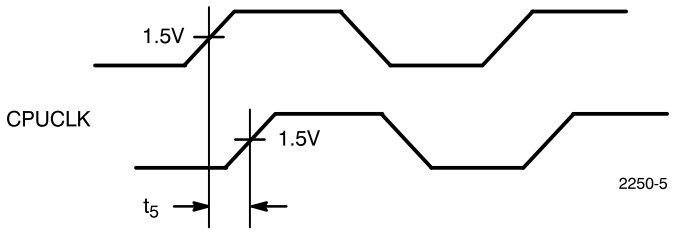
Duty Cycle Timing



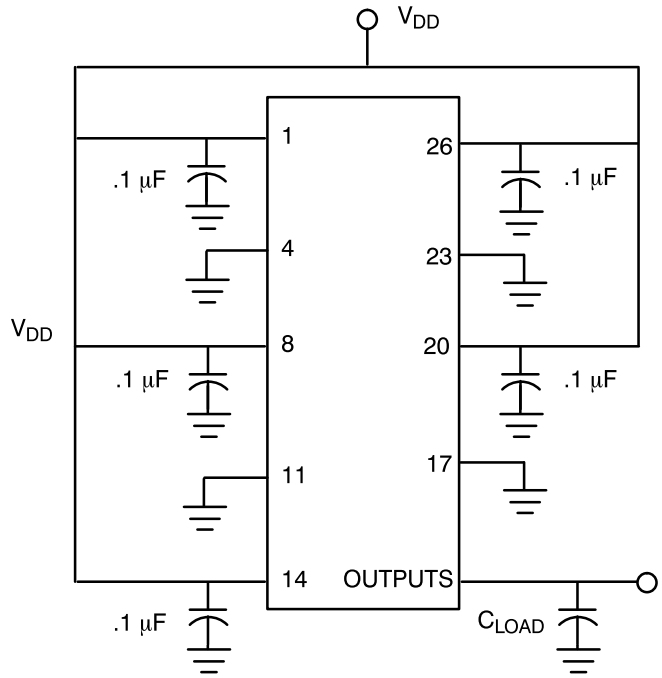
All Outputs Rise/Fall Time



Clock Skew



Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2250SC−1	S21	28-Pin SOIC	Commercial

Document #: 38−00477

Package Diagram

28-Lead (300-Mil) Molded SOIC S21