PRELIMINARY **CY2257**

Pentium™ Processor Compatible Clock Synthesizer/Driver for ALI Aladdin™ Chipset

Features

- **Multiple clock outputs to meet requirements of ALI Aladdin™ chipset**
  - **— Six CPU clocks @ 66.66 MHz, 60 MHz, and 50 MHz, pin selectable**
  - **— Six PCI clocks (CPUCLK/2)**
  - **— Two Ref. clocks @ 14.318 MHz**
- **CPU clock jitter ≤ 250 ps cycle-to-cycle**
- **Low skew outputs**
  - **— ≤ 250 ps between CPU clocks**
  - **— ≤ 500 ps between PCI clocks**
  - **— ≤ 750 ps between CPU clocks and PCI clocks**
- **Output duty cycle 40% min. to 60% max.**
- **Test mode support**
- **3.3V operation**
- **CMOS technology**

Functional Description

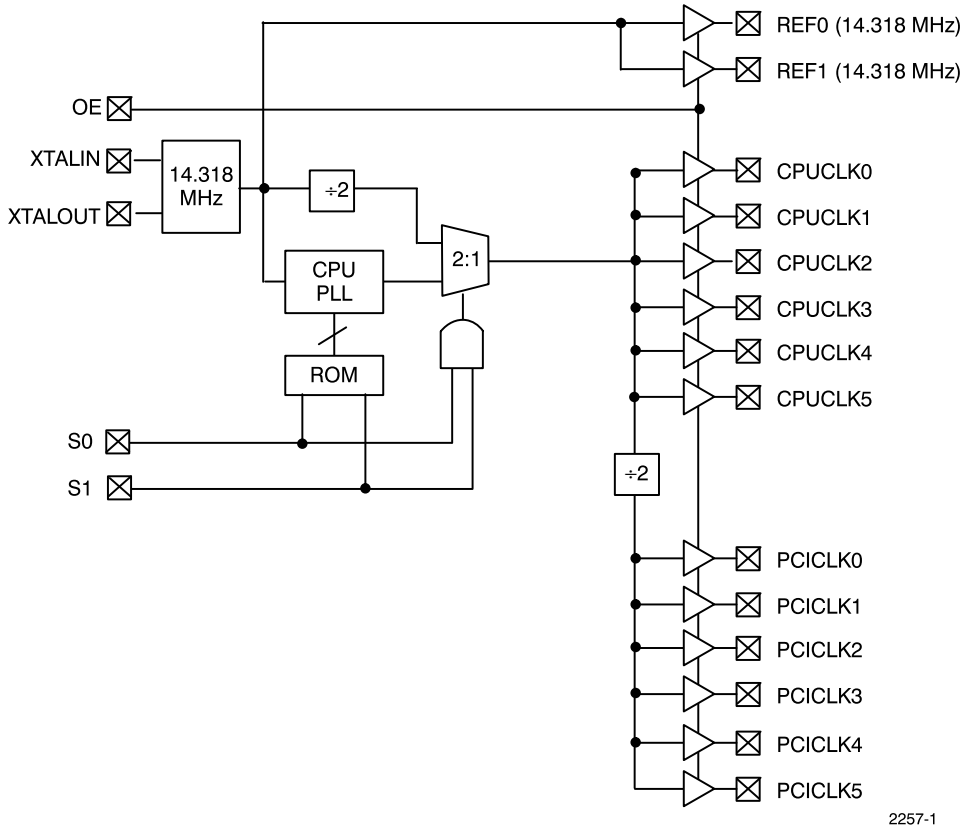
The CY2257 is an integrated Clock Synthesizer/Driver chip with multiple output clocks. The device is specifically designed for the ALI Aladdin™ chipset, which consists of the M1511, M1512, and M1513.

The CY2257 outputs six copies of the CPU clock at frequencies of 50, 60, and 66.66 MHz, pin-selectable by the Select signals, S1 and S0. Additional outputs include six synchronous PCI clocks, each running at half the CPUCLK frequency, and two copies of the Reference clock at 14.318 MHz. All outputs are three-stateable, and are controlled by an active-high OE (Output Enable) pin. Additionally, all outputs are capable of driving high-capacitance loads, thus eliminating the need for external buffers.

The CY2257 has low-skew outputs (≤ 250 ps between the CPU clocks, ≤ 500 ps between the PCI clocks). In addition, the CY2257 CPU clock outputs have less than 250 ps cycle-to-cycle jitter. Finally, both the PCI and CPU clock outputs meet the 1V/ns slew rate requirement of a Pentium™ processor–based system.

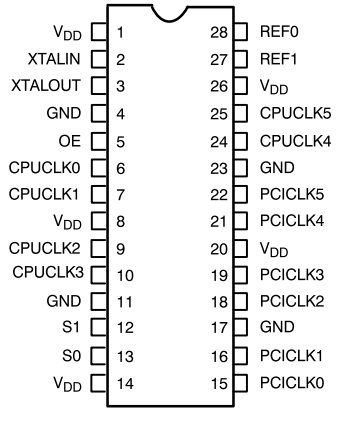
The CY2257 accepts a 14.318 MHz reference signal as its input, and uses it to generate the CPU and PCI clocks from a single PLL. The CY2257 runs off a 3.3V supply.

Logic Block Diagram



Pin Configuration

Top View
SOIC



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Pin Summary

Name	Number	Description
V_{DD}	1	Digital voltage supply
XTALIN[1]	2	Reference crystal input
XTALOUT[1]	3	Reference crystal feedback
GND	4	Ground
OE	5	Output Enable, Active HIGH
CPUCLK0	6	CPU clock output
CPUCLK1	7	CPU clock output
V_{DD}	8	Digital voltage supply
CPUCLK2	9	CPU clock output
CPUCLK3	10	CPU clock output
GND	11	Ground
S1	12	CPU clock select input, bit 1
S0	13	CPU clock select input, bit 0
V_{DD}	14	Digital voltage supply
PCICLK0	15	PCI clock output
PCICLK1	16	PCI clock output
GND	17	Ground
PCICLK2	18	PCI clock output
PCICLK3	19	PCI clock output
V_{DD}	20	Digital voltage supply
PCICLK4	21	PCI clock output
PCICLK5	22	PCI clock output
GND	23	Ground
CPUCLK4	24	CPU clock output
CPUCLK5	25	CPU clock output
V_{DD}	26	Digital voltage supply
REF1	27	Reference clock output (14.318 MHz)
REF0	28	Reference clock output (14.318 MHz)

Notes:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

Function Table

OE	S0	S1	XTALIN Input	CPUCLK [0:5]	PCICLK [0:5]	Ref. Clock Output
0	0	0	14.318 MHz	High-Z	High-Z	High-Z
0	0	1	14.318 MHz	High-Z	High-Z	High-Z
0	1	0	14.318 MHz	High-Z	High-Z	High-Z
0	1	1	TCLK[2]	High-Z	High-Z	High-Z
1	0	0	14.318 MHz	50 MHz	25 MHz	14.318 MHz
1	0	1	14.318 MHz	60 MHz	30 MHz	14.318 MHz
1	1	0	14.318 MHz	66.66 MHz	33.33 MHz	14.318 MHz
1	1	1	TCLK[2]	TCLK/2	TCLK/4	TCLK

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... −65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Operating Range

Ambient Temperature	V_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	3.3V ± 5%

Operating Conditions[3]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Ambient Temperature	0	70	°C
C_L	Max. Capacitive Load on CPUCLK PCICLK REF0 REF1		 20 30 30 15	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Notes:

2. TCLK is a test clock on the XTALIN input during test mode.
3. Electrical parameters are guaranteed with these operating conditions.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	HIGH-level Output Voltage	$V_{DD} = V_{DD}$ Min.	I_{OH} = 6 mA	CPUCLK	2.4		V
			I_{OH} = 12 mA	PCICLK, REF0			
			I_{OH} = 8 mA	REF1			
V_{OL}	LOW-level Output Voltage	$V_{DD} = V_{DD}$ Min.	I_{OL} = 6 mA	CPUCLK		0.4	V
			I_{OL} = 12 mA	PCICLK, REF0			
			I_{OL} = 8 mA	REF1			
V_{IH}	HIGH-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	LOW-level Input Voltage	Except Crystal Inputs				0.8	V
I_{IH}	Input HIGH Current	$V_{IH} = V_{DD} - 0.5V$			−5	+5	µA
I_{IL}	Input LOW Current	V_{IL} = 0.5V			−5	+5	µA
I_{OZ}	Output Leakage Current	Three-state outputs			−10	+10	µA
I_{DD}	Power Supply Current	V_{DD} = 3.465, V_{IN} = 0 or V_{DD}				90	mA

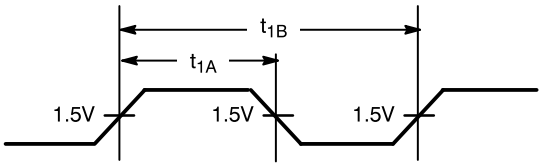
Switching Characteristics[4]

Parameter	Output	Name	Description	Min.	Max.	Unit
t_1	All	Output Duty Cycle[5]	$t_1 = t_{1A} \div t_{1B}$	40%	60%	
t_2	CPUCLK, PCICLK	Output Slew Rate	0.4−2.4V	1		V/ns
t_3	REF0, REF1	Rise Time	20% − 80% of V_{DD}		4	ns
t_4	REF0, REF1	Fall Time	20% − 80% of V_{DD}		4	ns
t_5	CPUCLK	CPU Skew	CPU-CPU clock skew		250	ps
t_6	PCICLK	PCI Skew	PCI-PCI clock skew		500	ps
t_7	CPUCLK, PCICLK	CPU-PCI Skew	CPU to PCI clock skew		750	ps
t_8	CPUCLK	Cycle-Cycle Clock Jitter	Clock jitter		250	ps

Notes:
4. All parameters specified with outputs fully loaded.
5. Duty cycle is measured at 1.5V.

Switching Waveforms

Duty Cycle Timing



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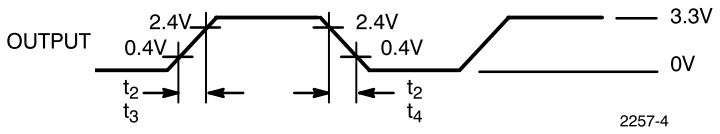
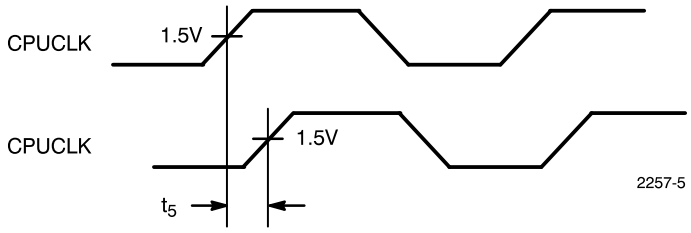
Switching Waveforms (continued)

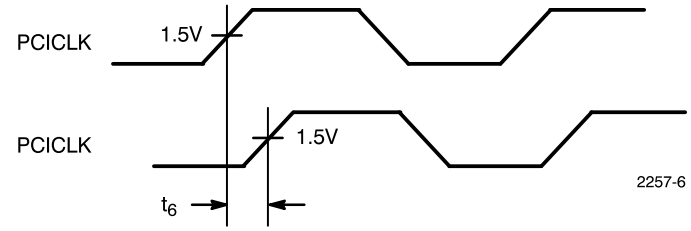
All Outputs Rise/Fall Time



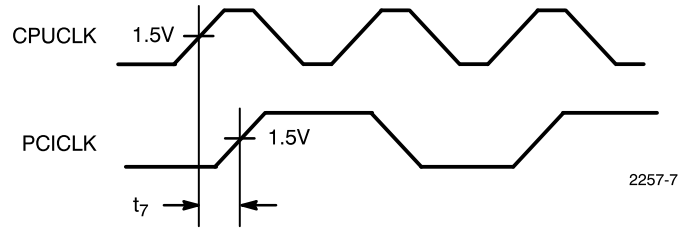
CPU-CPU Clock Skew



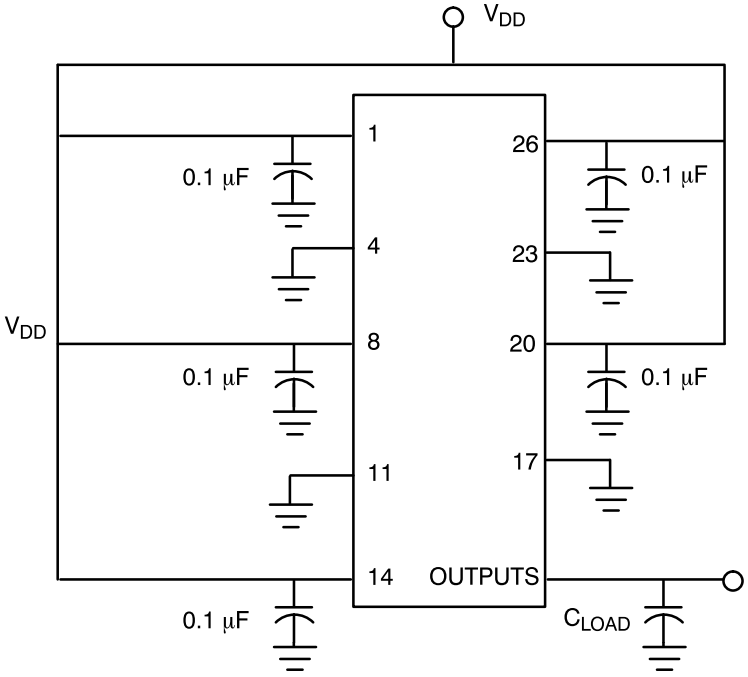
PCI-PCI Clock Skew



CPU-PCI Clock Skew



Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2257	S21	28-Pin SOIC	Commercial

Document #: 38−00462

Package Diagram

28-Lead (300-Mil) Molded SOIC S21