Clock Terminology

There are many different (and often confusing) terms associated with clock-based devices. This application note attempts to clarify these terms, and hence serves as a comprehensive reference on clock terminology. This application note can be divided into two sections. The first section describes and distinguishes between various clock sources available today. The second section defines and distinguishes between various parameters used to describe clocks. This section also provides methods of measuring some of these parameters.

Clock Devices

There are a variety of clock devices available today. Some of them are described below.

Crystals

A *Crystal* is a basic piezoelectric quartz crystal. On its own, it cannot generate electrical clocks. It has to be connected to a clock oscillator to get a clock waveform. There are two kinds of crystals; *Series Resonant,* which can be modeled as a high Q series L-C circuit, and *Parallel Resonant,* which can be modeled as a high Q parallel L-C circuit. The series resonant crystal has minimum impedance at the resonating frequency, while the parallel resonant crystal has maximum impedance at the resonating frequency. Cypress-ICD devices expect parallel resonant crystals for the reference device.

Crystal Oscillators

A *Crystal Oscillator* is an oscillator with the crystal as the feedback element. There are other kinds of oscillators with active or passive feedback components, but the crystal oscillator provides the most accurate output frequency.

Crystal oscillators come in a variety of packages, though the 4-pin package (Metal Can Oscillator) in the 300-mil 14-pin DIP footprint is very popular. Surface mount and Half DIP packages are also available. Finally, crystal oscillators are the preferred clock source in most high-speed digital systems requiring clocks.

Compensated Oscillators

The output frequency of a crystal oscillator varies with temperature and voltage. Applications that require a highly stable clock usually use compensated oscillators. *Compensated Oscillators* try to adjust the variation in frequency due to temperature and voltage. *Temperature Compensating Oscillators (TXCO)* contain circuitry that compensates for temperature changes, and hence combat frequency variations. *Oven Controlled Oscillators* encase their crystals in a temperature-controlled oven, and so maintain a precise operating temperature at the crystal. *Double Oven Oscillators* contain two ovens, with the crystal encased in the inner oven, and the temperature control circuitry and the inner oven encased in the outer oven. Such oscillators provide even better temperature stability than Oven Controlled Oscillators. Obviously, as the frequency stability improves, the cost of the oscillator increases.

Voltage Controlled Oscillator

The output of *Voltage Controlled Oscillators (VXCO)* is controlled by a voltage control input pin. Variation between control voltage and frequency is usually nonlinear.

Frequency Synthesizers

Frequency Synthesizers use one or more *Phase-Locked Loops (PLL)* to generate one to many different frequencies on their outputs, from one or more reference sources. The reference frequency is usually generated by a crystal attached to the synthesizer. The design goal of frequency synthesizers is to replace multiple oscillators in a system, and hence reduce board space and cost. *Figure 1* shows a block diagram of a Phase Locked Loop (PLL).

A PLL has two inputs, a reference input and a feedback input. A PLL corrects frequency in two ways. The first, frequency correction, corrects large differences in frequency between the reference input and the feedback input. Frequency correction is akin to "rough" tuning and occurs when F_{vco} is less than $0.5F_{ref}$ or greater than $2F_{ref}$. Phase correction is the "fine" tuning and occurs when $0.5F_{vco} < F_{ref} < 2F_{vco}$.

The Phase/Frequency Detector detects differences in phase and frequency between the reference and feedback inputs and generates compensating "Up" and "Down" signals depending on whether the feedback frequency is lagging or leading the reference frequency respectively. These control signals are then passed through a charge pump and a loop filter to generate a control voltage, which controls a Voltage-Controlled Oscillator (VCO). The frequency of this oscillator is dependent on the V_{ctrl} input. At steady state, the VCO frequency is:

$F_{vco} = F_{ref} * P/Q$

The output frequency of the PLL can be expressed as

$F_{out} = (F_{ref} * P)/(Q * N)$

The *Sample Rate* of a Frequency Synthesizer determines how often the inputs are sampled in order to perform phase and frequency correction. It is expressed as F_{ref}/Q.

The *Acquisition/Lock Time* of a PLL-based Frequency Synthesizer is the amount of time taken by the Frequency Synthesizer to attain the target frequency after power-up, or after a programmed output frequency change.

The *Resolution* of a PLL-based Frequency Synthesizer is based on the number of bits in the P and Q counter. The Resolution will determine in what size increments the frequency can change.

The *Deadband* of a PLL-based Frequency Synthesizer is the largest phase difference between the ref-

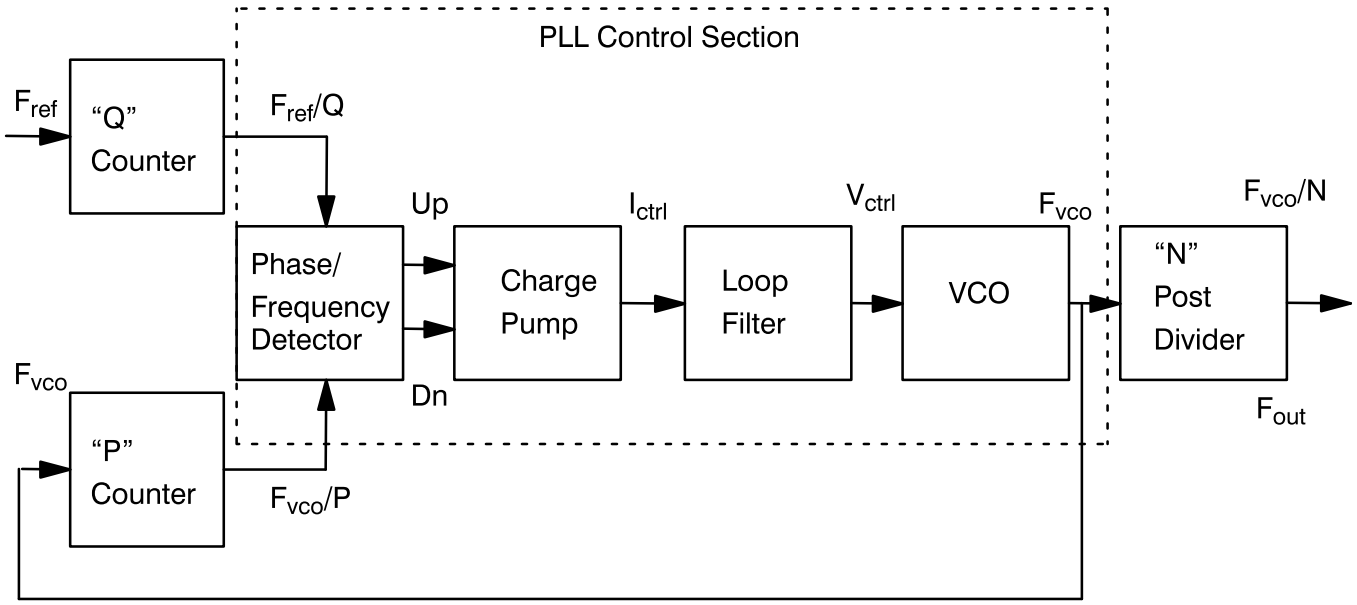


Figure 1. Block Diagram of a Phase Locked Loop

erence and the feedback inputs, which will not be corrected by the PLL.

Multiple PLLs are needed within a single frequency synthesizer to generate multiple unrelated frequencies.

Frequency synthesizers are gaining in popularity as system complexity increases and systems utilize multiple clocks. The term "Clock Generator" is interchangeably used with "Frequency Synthesizer."

Clock Buffers

A *Clock Buffer* is a device in which the output waveform directly follows the input waveform. The input waveform propagates through the device and is redriven by the output buffers. Hence, such devices have a propagation delay associated with them. In addition, due to the differences between the propagation delay through the device on each input-output path, skew will exist on the outputs. An example of a clock buffer is the 74F244, which is available from several manufacturers.

Clock Parameters

This section contains definitions and explanations of various parameters used to describe clocks.

Clock Jitter

Jitter can be defined as the deviations in a clock's output transitions from their ideal positions. The deviation can either be leading or lagging the ideal position. Hence, jitter is expressed in ±ns. Jitter can be classified into three categories: cycle-cycle jitter, period jitter, and long-term jitter.

Cycle-cycle jitter is the difference in a clock's period from one cycle to the next. This kind of jitter is the most difficult to measure and usually requires a Timing Interval Analyzer. *Figure 2* shows a graphical representation of cycle-cycle jitter. J_1 and J_2 are the jitter values measured. The maximum of such values measured over multiple cycles is the maximum cycle-cycle jitter.

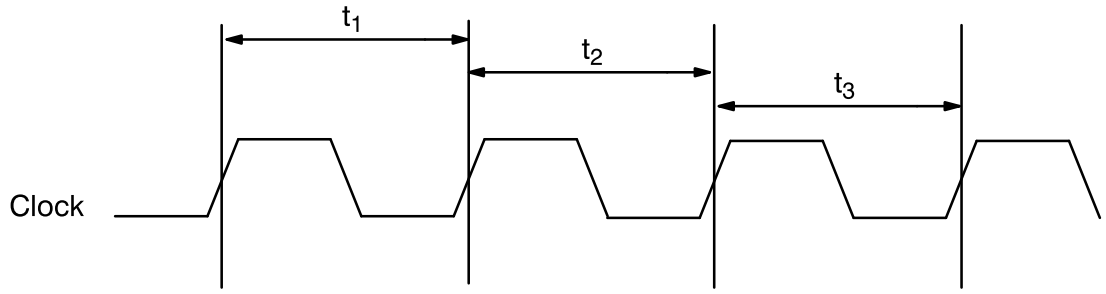
Period jitter, also called short-term jitter, is a change in a clock's output transition from its ideal position over consecutive clock edges. *Figure 3* shows short-term jitter. Note that in the case of short-term jitter, the variation of the rising edge of clock from the ideal position is measured and expressed in units of time or frequency.

Long-term jitter is a change in a clock's output transition from its ideal position, over "many" cycles. The term "many" depends on the application and the frequency. For PC motherboard and graphics applications, this term "many" usually refers to 10−20 microseconds. For other applications, it may be different. *Figure 4* shows a graphical representation of long-term jitter.

Causes of Jitter

There are four primary causes of jitter as indicated below:

- Power supply noise
- The internal PLL of the synthesizer



Jitter $J_1 = t_2 - t_1$

Jitter $J_2 = t_3 - t_2$

Figure 2. Cycle-Cycle Jitter

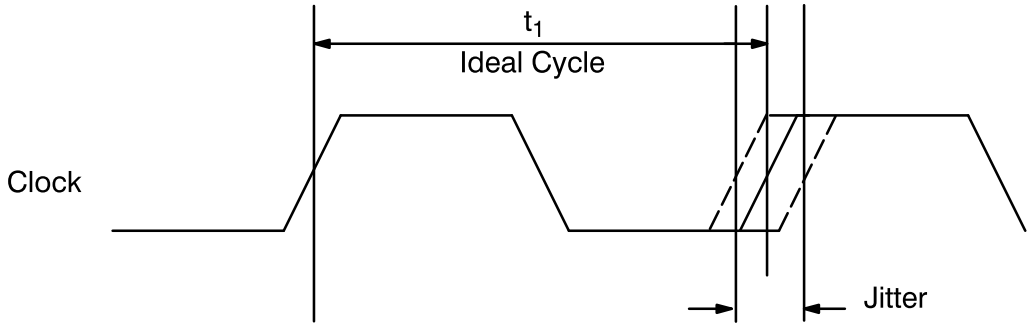


Figure 3. Period Jitter

- Random thermal noise from crystal, or any other resonating device.
- Random mechanical noise from vibrations of the crystal

For a more detailed discussion on jitter, please refer to the application note entitled "Jitter in PLL-Based Systems."

What Systems Does Clock Jitter Affect?

Clock jitter affects almost all high-speed synchronous systems. Common applications affected by jitter are PC motherboards, graphics cards, and communications equipment.

Skew

Skew is the variation in arrival time of two signals specified to arrive at the same time. Skew is composed of two parts, the output skew of the driving device, and board design skew, caused by layout variation of board traces. *Figure 5* explains skew.

Clock Driver Skew (Intrinsic Skew) is the amount of skew caused by the clock driver itself. There are two kinds of clock driver devices; buffer devices and PLL-based devices. Skew occurs on the output of the buffer devices because of the differences in propagation delay of the input signal through the device. A majority of this difference is attributed to differences in output loading. Skew in PLL-based devices can be very small, since a PLL-based device

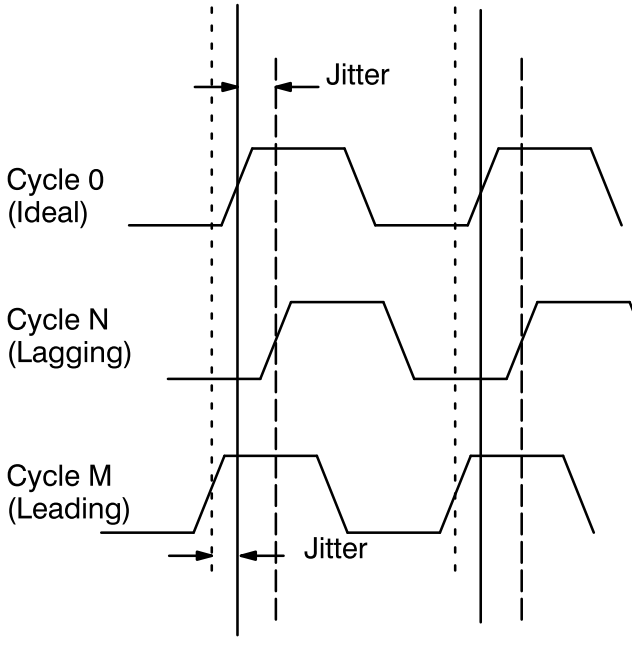


Figure 4. Long-Term Jitter

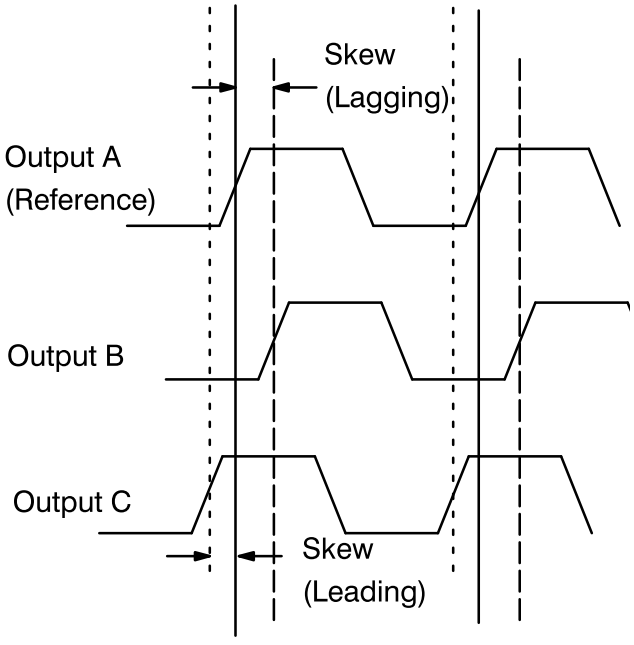


Figure 5. Graphical Representation of Skew

can be adjusted to compensate for differences in output loading.

Board Design Skew (Extrinsic skew) is the amount of skew caused by board layout issues such as:

- Trace Length: The amount of time for a signal to propagate down a trace is dependent on the material of the PCB, length of the trace, width of the trace and capacitive loading. Different trace lengths cause different signal propagation times, and hence cause skew.
- Threshold Voltage Variation: The threshold voltage of the receiving device can cause skew. For example, if a receiving device has a threshold voltage of 1.2V and another device has a threshold voltage of 1.7V, and the rise time of the input signal is 1V/ns, then the two devices will switch 500 ps apart, which is skew.
- Capacitive Loading: The differences in capacitive loading on traces will cause differences in the clock rise times at the load. This affects the time at which the clock edge crosses the input threshold and results in skew.
- Transmission Line Termination: With the extremely fast edge rates in today's clock drivers, traces longer than 4 inches are considered transmission lines. Without proper termination, these lines will exhibit transmission line effects like voltage reflections, which will cause skew.

Why Is Skew Important?

In high-speed systems, clock skew forms an important component of timing margin. A skew of 1 ns is a significant portion of a 15-ns cycle time. If the timing budget does not allow for skew, it is highly likely that the system will perform marginally.

Measuring Skew

The simplest method of measuring skew between two outputs of a device is to display both waveforms in a dual-channel oscilloscope and measure the difference between the rising edges. This is the skew.

Clock buffer datasheets usually specify two parameters, *"output-to-output skew"* and *"part-to-part skew."* The latter parameter includes the former. If neither parameter is specified, then the maximum output skew is the difference between the maximum and minimum propagation delay times through the device.

Stability

Stability is a parameter usually associated with oscillators. Stability is defined as the variation in operating frequency from the nominal frequency and is expressed in ppm (parts per million). The nominal frequency is the frequency shown on the device package.

All variations in frequency are lumped together in the stability specification. Variations in manufacturing processes, aging, temperature, and voltage cause variations in stability. The worst effects are due to temperature variation.

Why Is Stability Important?

Using the stability parameter, a system designer can find the maximum variation in frequency, and hence can design systems based on worst-case specifications. Designing systems without considering stability can cause failure over time.

Aging

Aging is defined as the variation in frequency over time. It is usually expressed in ppm/year, and may be incorporated in the Stability spec, if it is not drawn out separately. It is a parameter usually associated with crystal oscillators. New crystals age faster than old crystals. Typical aging rates are of the order of 5 ppm/yr.

Why Is Aging Important?

Aging may cause marginal operation of a design over an extended period of time, if it is not accounted for in the design.

Voltage Sensitivity

Voltage Sensitivity is the variations in frequency due to variations in operating voltage. It is expressed in ppm/volts. On crystal oscillators, it is usually incorporated in the stability spec. On PLL-based devices, it is usually incorporated in the jitter spec.

Accuracy/Precision

Accuracy/Precision is a measure of how close the part operates to the specified (nominal) frequency.

For example, if a part is specified with a 25.000-MHz output, and the long-term (user-defined) average of its output frequency is 25.001 MHz, the part has 40 ppm accuracy. Accuracy can be expressed as:

Accuracy=(L.T. Avg. Freq. – Nominal Freq.)/Nominal Freq.

Error

On a PLL-based device, it may not always be possible to get the specified frequency on the outputs. The limitation is due to the size of the internal "P" and "Q" counters in the PLL (see later sections for detailed information). If, for example, the specified frequency is 25.000 MHz, and the PLL can output 24.998 MHz, the error is −80 ppm. *Error* can be expressed as:

Error = (Nominal Freq. – Target Freq.)/Target Freq.

Note the difference between error and accuracy. Error specifies the difference between the frequency you want, and the frequency you get. Accuracy specifies the difference between the frequency you get, and the long term average of this frequency.

Slew

The rate of change of voltage or frequency is called *Slew*. Slew is usually measured on the rising and falling edges of digital signals. However, rise times and fall times are more commonly specified, instead of slew, in vendor's catalogs.

Recently, with the advent of low-power devices, slew is being used to define a rate of change of frequency.

Wander/Drift

Wander and *Drift* are the same, and are usually used to express frequency variations due to temperature and voltage. Usually, wander and drift are incorporated in the stability specification.

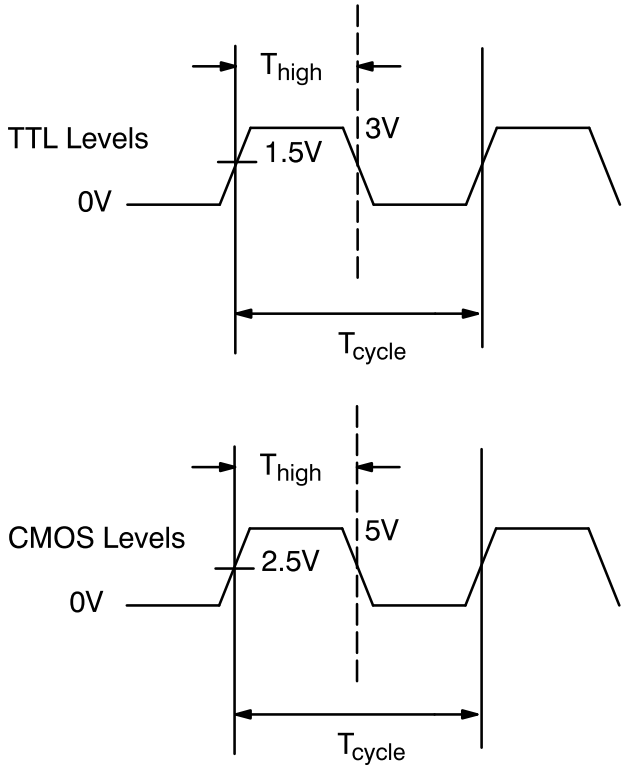


Figure 6. CMOS/TTL Duty Cycle Measurement

Duty Cycle

Duty Cycle is the ratio of the output high time to the total cycle time. It is expressed as a percentage. 50% is the ideal duty cycle, though most clock manufacturers specify duty cycles from 40% − 60%. Duty cycle is important in systems that use both the rising and falling clock edges.

Duty cycles can be expressed for both TTL and CMOS devices. For TTL devices, since the voltage swing is from 0V−3V, the high time is measured at the 1.5V level. For CMOS devices, since the voltage swing is from $0-V_{dd}$ Volts, the high time is measured at $V_{dd}/2$. Hence, if a device claims to meet both CMOS and TTL duty cycle measurements, it refers to the voltage at which the high time is measured, not the output voltage swing. *Figure 6* shows the difference between CMOS and TTL duty cycle measurement levels.

Conclusion

This application note presented clear and detailed descriptions of various clock devices available today, along with parameters used to describe clocks. It also provided methods of measuring some of these parameters.

References

1. Johnson, Howard, and Graham, Martin, *High-Speed Digital Design: A Handbook of Black Magic.* PTR Prentice-Hall. New Jersey, 1993.