ECL Outputs

Introduction

The Cypress Timing Technology products family features ECL-compatible outputs in products such as the ICD2062. These outputs allow clocking at frequencies above 160 MHz, with all the inherent advantages of differential ECL signal transmission.

This application note covers the principal advantages of using ECL outputs and makes recommendations concerning layout and wiring methods for parts such as the ICD2062.

Power Supplies (PECL vs. ECL)

The ECL V_{DD} and V_{EE} pins have traditionally been powered from a −5.2V supply, V_{DD} being grounded and V_{EE} set at −5.2V—the intent is to achieve the lowest V_{DD} noise by grounding the V_{DD} pins. In more recent designs, however, ECL is often used with +5.0V instead of −5.2V. (V_{DD} set to + 5.0V and V_{EE} tied to ground.) Since V_{DD} noise is not a major concern, this permits the use of a standard logic supply. This application note will focus on +5.0V ECL designs (sometimes called PECL).

ECL Advantages

As clock speeds rise beyond 100 MHz, the advantages of using ECL become more obvious. Most of these advantages involve the use of differential signal transmission.

Differential signals are less susceptible to ground noise problems, as all noise becomes common-mode. Single-ended CMOS is much more susceptible, since ground bounce and other noise affect logic thresholds, degrading noise immunity. ECL signals remain unaffected, since noise rides on both signals as an average level. Logic levels are also less critical, since the threshold is the differential cross point, which can tolerate significant signal attenuation. Differential circuits also tend to generate less noise in the power supply.

ECL is designed with termination resistors that allow high-frequency signals to propagate with minimal overshoot and reflection.

These advantages are most pronounced in a bipolar implementation, but many of the same benefits can be realized in CMOS designs.

Pad Structure

Referring to *Figure 1*, transistors Q1 and Q2 form differential ECL output drivers. Unlike single-ended outputs (see *Figure 2*), N-type transistors are not required, since termination resistors are always present and serve as pull-downs.

The ECL output drive logic guarantees that when Q1 switches ON, Q2 switches OFF (and vice versa). A complementary logic state is always maintained, assuring a constant current supply draw in either output state.

Logic Levels

The V_{OH}/V_{OL} logic levels are approximately 4.1V to 3.2V. This gives a differential signal of 0.9 V. This is more than adequate, since bipolar ECL V_{OH}/V_{OL} are typically 4.1V to 3.3V for a differential swing of 0.8V. If the termination resistors are reduced from the 220Ω/330Ω suggested value, the V_{OH} level can be reduced somewhat.

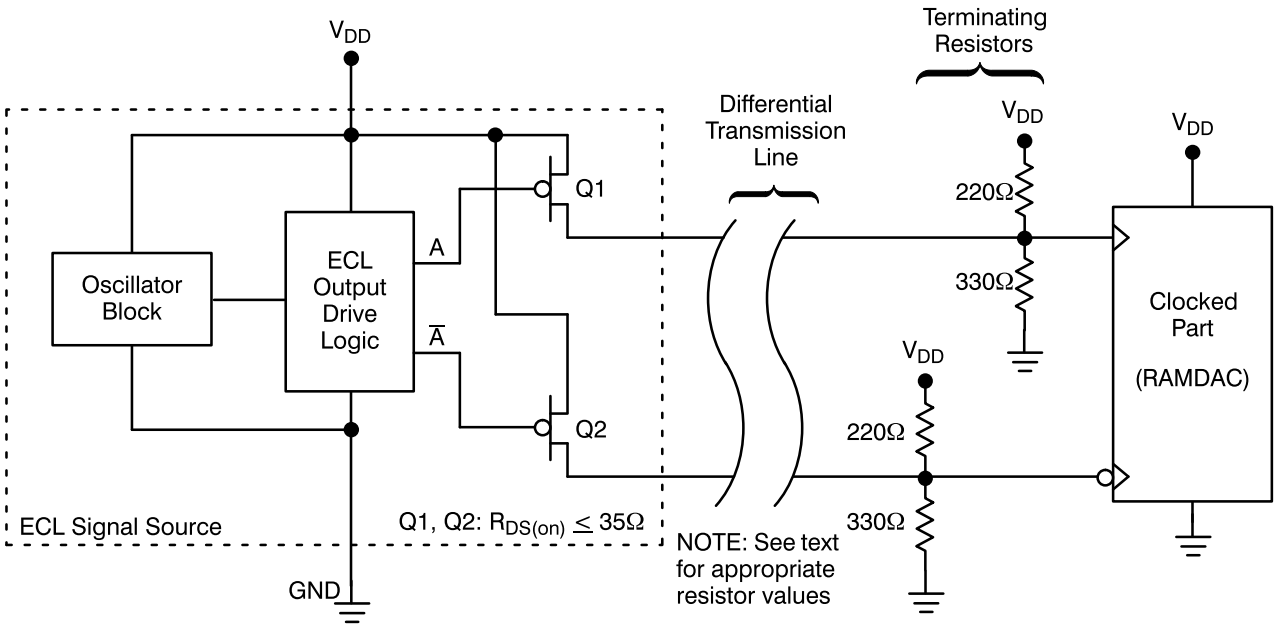

Figure 1. Differential ECL Output Driver

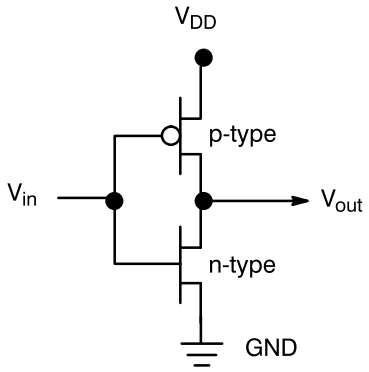

Figure 2. Single-Ended Output Driver

Output Routing and Board Layout Issues

ECL signals maintain their integrity over long routing distances. A 100-MHz single-ended trace should be limited to a few inches, but ECL can travel several feet at that frequency. This is due to ECL's termination resistors at the receiving devices.

For good signal integrity, ECL traces are laid out in pairs. By controlling the board layout and specifying appropriate electrical properties, a constant characteristic impedance of 100Ω to 150Ω can be achieved. By employing transmission live techniques, high-quality signals are ensured.

To reduce V_{DD} noise the clock generator must be properly bypassed at the supply pins, as should the parts to be clocked. Terminating resistors should also be bypassed separately if they are not located near a bypass capacitor.

Terminating Resistor Values

The 220Ω/330Ω values represent a trade-off between low-power draw and best high-frequency performance. For frequencies above 80 MHz, they may pull down too weakly, resulting in inadequate signal swing. These values can go as low as 68Ω/100Ω at 160 MHz (always maintaining an approximate 2:3 ratio). Low values work satisfactorily at both low and high frequencies, the only drawback being a higher current drain.

Summary

A general overview of ECL logic has been presented, with emphasis on the interface of ECL logic to +5V powered CMOS clock generators. Should additional support be required, contact Cypress Applications for assistance.