ICD2023

PC Motherboard Clock Generator

Features

- **Seven independent clock outputs handle all clocking requirements for personal computer motherboards**
- **Phase-locked loop oscillator input derived from single 14.31818 MHz crystal**
- **Programmable frequency range: 10 MHz to 80 MHz with 50% duty cycle**
- **Ideally suited for PC desktop and laptop computer applications**
- **Sophisticated internal loop-filter requires no external components or manufacturing tweaks as commonly required with external filters**
- **Battery input maintains 32.768 KHz clock during power-down**
- **Three-state oscillator control disables outputs for test purposes**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 20-pin SOIC package configuration**

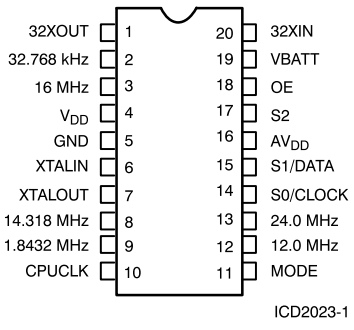
Functional Description

A modern personal computer motherboard often requires as many as seven different crystal can oscillators. The System Logic family of frequency synthesis parts from Cypress/IC Designs replaces the large number of oscillators required to build such multi-function motherboards. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2023 PC Motherboard Clock Generator offers two oscillators, two phase-locked loops and seven different outputs in a single package. Six of the outputs are of a fixed value while the seventh output is fully user-programmable and may be changed on-the-fly to any desired frequency value between 10 MHz and 80 MHz. The ICD2023 is ideally suited for use in both existing designs (since it requires no support from the motherboard chip set and outputs seven frequencies concurrently) and new designs which can utilize the programmable nature of this device.

Pin Configurations

SOIC
Top View



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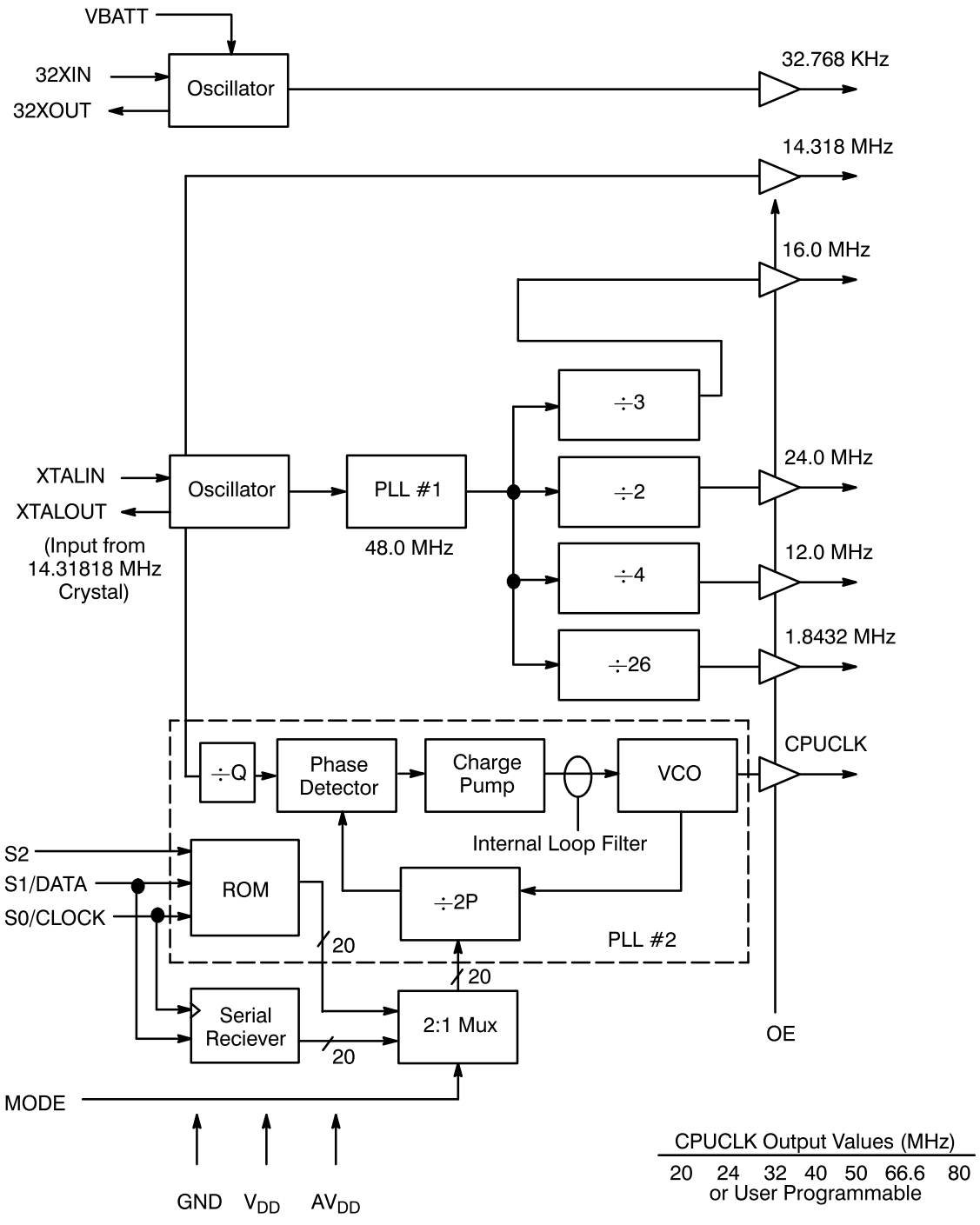
Logic Block Diagram



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Pin Summary

Name	Number	Description
32XOUT[1]	1	Oscillator output to a 32.768 kHz parallel-resonant crystal
32.768 kHz	2	32.768 KHz Output
16 MHz	3	16 MHz Output
V_{DD}	4	+5V
GND	5	Ground
XTALIN[1]	6	Reference Oscillator input for all internal phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT[1]	7	Oscillator Output to a reference crystal.
14.318 MHz	8	14.318 MHz Output
1.8432 MHz	9	1.8432 MHz Output
CPUCLK	10	CPUCLK clock output (See *Table 2*.)
MODE	11	MODE=0, CPUCLK is in programmable mode MODE=1, CPUCLK depends on S2, S1, and S0
12.0 MHz	12	12.0 MHz Output
24.0 MHz	13	24.0 MHz Output
S0/CLOCK	14	MODE=0, S0 is serial clock input line for CPUCLK MODE=1, S0 is select line for CPUCLK (Internal pull-up)
S1/DATA	15	MODE=0, S1 is serial data input line for CPUCLK MODE=1, S1 is select line for CPUCLK (Internal pull-up)
AV_{DD}	16	+5V to Analog Core
S2	17	MODE=0 and S2 =1; CPUCLK=(14.31818 MHz) reference frequency MODE=1, S2 is select line for CPUCLK (Internal pull-up)
OE	18	Output Enable three-states output when signal is LOW (pin has internal pull-up)
V_{BATT}	19	Battery backup voltage
32XIN[1]	20	Oscillator input from a 32.768 kHz parallel-resonant crystal.

General Considerations

Fixed Frequency Oscillator Operation

The following table describes each output:

Table 1. Fixed Frequency Oscillator Operation

Output Clock Function	Desired Frequency (MHz)	Actual Frequency (MHz)	PPM Error
Real-Time Clock[2]	32.768 kHz	32.768 kHz	0
System Bus[3]	14.318	14.318	0
Int. Bus Clock[4]	16.000	15.983	1058
Keyboard Clock[5]	12.000	11.987	1058
Floppy Disk Clock[6]	24.000	23.975	1058
Serial Port[7]	1.843	1.844	543

Notes:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.
2. Pass-through 32.768 kHz XTAL.
3. Pass-through 14.31818 MHz XTAL.
4. Output = 47.94295/3.
5. Output = 47.94295/4.
6. Output = 47.94295/2.
7. Output = 47.94295/26.

CPUCLK Programmable Oscillator: Selection Mode

CPUCLK offers a programmable output based on two modes of operation. The first mode uses three select lines to select one of eight different preset frequencies, while the other mode allows the user to program any desired frequency between 10 MHz and 80 MHz. The two different modes are controlled by the MODE signal.

When MODE=1, the select lines can be changed to choose different frequencies. When this occurs, PLL #2 will immediately seek the newly selected frequency as shown in the following table. During the transition period, the CPUCLK output will not glitch.

Table 2. CPUCLK Output with MODE=1

S2	S1	S0	Desired Freq. (MHz)	Actual Freq. (MHz)	PPM Error
0	0	0	20.000	20.0454	2272
0	0	1	24.000	23.9746	1058
0	1	0	32.000	32.0455	1422
0	1	1	40.000	40.0909	2272
1	0	0	50.000	49.9923	154
1	0	1	66.667	66.5962	57
1	1	0	80.000	80.1818	2272
1	1	1	100.000[8]	99.8182	1818

CPUCLK Programmable Oscillator: Serial Mode

When MODE=0, CPUCLK enters its programmable mode. Signals S0 (clock) and S1 (data) become a serial interface, allowing a 20-bit number to be shifted in. In ICD2023 programmable oscillator (CPUCLK) requires a 20-bit programming word (W). This word contains 4 fields:

Table 3. Programming Word Bit Fields

Field	# of Bits
Index (I)[9]	4
P Counter value (P)	7
Mux (M)	3
Q Counter Value (Q)[10]	6

If a signal S2=1 and MODE=0, then the reference frequency (14.31818 MHz) is multiplexed to the CPUCLK output. This enables a glitch-free transition to the reference frequency while the VCO stabilizes.

The frequency of the programmable oscillator $f_{(VCO)}$ is determined by these fields as follows:

$P'=P-3 \quad Q'=Q-2$

$f_{(VCO)}=2 \times f_{(REF)} \times P/Q$

where $f_{(REF)}$=Reference frequency=14.31818 MHz.

The value of $f_{(VCO)}$ should be kept between 40 MHz and 80 MHz. Therefore, for output frequencies below 40 MHz, $f_{(VCO)}$ must be multiplied up into the required range. The mux bits allow a post-divide of the higher VCO to bring the output to those desired values below 40 MHz.

Table 4. Mux Bits M_0-M_1

M_1	M_0	Divisor
0	0	16
0	1	4
1	0	2
1	1	1

The M2 mux bit is used to select which one of the two Phase-Locked Loops is to be utilized in the CPUCLK output. Normally, the PLL #2 section (see Logic Block Diagram) is used. However, if the desired output frequency requires $f_{(VCO)}$ to be set to 48 MHz, then PLL #1 section should be used. This both reduces power consumption (since only one VCO is activated) and eliminates the possibility of jitter which can arise when two VCOs of the same frequency beat (heterodyne) against each other.

Table 5. Mux Bits M_2

M_1	CPUCLK
0	PLL #2
1	PLL #1 (48 MHz)

The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be should be chosen from *Table 6*. (Note that this table is referenced to the VCO frequency $f_{(VCO)}$, rather than to the desired output frequency.)

Table 6. Index Field (I)

I	$f_{(VCO)}$ MHz
0001	40.0–47.5
0010	47.5–52.2
0011	52.2–56.3
0100	56.3–61.9
0101	61.9–65.0
0110	65.0–68.1
0111	68.1–80.0
1111	Turn off VCO

If the desired VCO frequency lies on a boundary in the table (if it is exactly the upper limit of one entry and the lower limit of the next) then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, Cypress/IC Designs provides *BitCalc* (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers. Contact your local Cypress representative for more information.

Notes:

8. Duty cycle specs not guaranteed above 80 MHz.
9. MSB (Most Significant Bits).
10. LSB (Least Significant Bits).

Programming Constraints

There are five primary programming constraints the user must be aware of:

Table 7. Programming Constraints

Parameter	Minimum	Maximum
$f_{(REF)}$	14.31818 MHz	14.31818 MHz
$f_{(REF)}/Q$	200 kHz	1 MHz
$f_{(VCO)}$	40 MHz	80 MHz
Q	3	65
P	4	130

The constraints have to do with trade-offs between optimum speed and lowest noise, VCO stability and factors affecting the loop equation. The factors are listed for completeness sake; however, by using the *BitCalc* program all of these constraints become transparent.

ICD2023 Programming Example

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz<40 MHz, double it to 79.0 MHz. Set M2, M1 and M0 to 0, 1 and 0, respectively. Set I to 0111. The result:

$$f_{(VCO)}=79.0=(2 \times 14.31818 \times P/Q)$$
$$P/Q=2.7857$$

Several choices of P and Q are available:

Table 8. P and Q Value Pairs

P	Q	$f_{(VCO)}$ (MHz)	Error (PPM)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Choose (P, Q)=(80,29) for best accuracy (40 ppm).

Therefore:

P'=P−3=80−3=77=1001101 (4dH)
Q'=Q−2=29−2=27=0011011 (1bH)

and the full programming word, W is:

W=I, P', M, Q'=0111, 1001101, 010, 011011
=01111001101010011011 (79a9bH)

A LOW-to-HIGH transition on S0 is used to shift the programming word W into S1 as a serial bit stream, LSB first. (See the set-up and hold timing specifications elsewhere in this datasheet.) If more than 20 shifts are performed, only the last 20 data bits received will be retained.

Output Frequency Accuracy

The accuracy of the ICD2023 output frequencies depends on the target output frequency. As stated previously, the output frequencies of the ICD2023 are an integral fraction of the input reference frequency:

$$f_{(OUT)}=2 \times f_{(REF)} \times P/Q$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2023 normally produces an output frequency within 0.1% of the target frequencies listed. This is more than sufficient to meet standard motherboard requirements. Specifics regarding accuracy are available from the output of the *BitCalc* program.

Three-State Output Operation

The OE signal, when pulled LOW, will three-state all the clock output lines (except 32.768 kHz). This supports wired-OR connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The OE signal contains an internal pull-up; it can be left unconnected if 3-state operation is not required.

V_{BATT}

The V_{BATT} input powers the Real-Time Clock Oscillator (RTC). The back-up power is typically supplied by a 3V lithium battery; however, any voltage between 2V and 5V is acceptable. If the 32 kHz output is not used, all related inputs and outputs and V_{BATT} should be grounded.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential . . . . . −0.5V to +7.0V
DC Input Voltage . . . . . −0.5V to V_{DD} +0.5V
Storage Temperature . . . . . −65°C to +150°C
Max soldering temperature (10 sec) . . . . . 260°C
Junction temperature . . . . . 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{BATT}	Backup Battery Voltage	Typical=3.0 Volts	2.0	5.0	V
V_{OH}	Output HIGH Voltage	I_{OH} = − 4.0mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{OH-32}	32.768 kHz Output HIGH				V
V_{OL-32}	32.768 kHz Output LOW				V
V_{IL}	Input LOW Voltage	Except crystal inputs		0.8	V
V_{IH}	Input HIGH Voltage	Except crystal inputs	2.0		V
I_{IH}	Input HIGH Current	$V_{IH} = V_{DD}-0.5V$		150	µA
I_{IL}	Input LOW Current	V_{IL} = +0.5V		−250.0	µA
I_{OZ}	Output Leakage Current	(Three-state)		10	µA
I_{DD}	Supply Current	V_{DD} = Max., fully loaded output, typical = 40[11]	25	65.0	mA
I_{BATT}	Backup Battery Current	V_{BATT} = 3V, fully loaded output, typical = 8 µA		50	µA

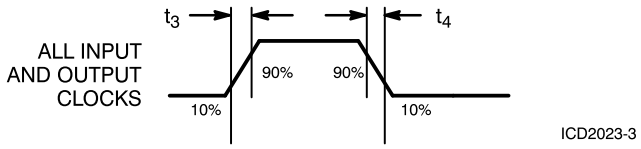
Switching Characteristics Over the Operating Range[12]

Parameter	Description	Test Conditions	Min.	Max.	Unit
	CPUCLK	Clock Output	10	80	MHz
t_1	Ref Frequency	Reference Oscillator nominal value		14.318	MHz
t_2	Duty Cycle	Duty cycle for the outputs defined as $t_{2A} \div t_{2B}$	40%	60%	
t_3	Rise Time	Rise time for the outputs into a 25 pF load		4	ns
t_4	Fall Time	Fall time for the outputs into a 25 pF load		4	ns
t_5	Set-Up Time	Delay required after MODE goes LOW prior to starting the S0 clock line		0	ns
t_6	Cycle Time	Minimum cycle time for the S0 clock	200		ns
t_7	Set-Up Time	Time required for the data to be valid prior to the rising edge of S0/CLOCK	10		ns
t_8	Hold Time	Time required for the data to remain valid prior to the rising edge of S0/CLOCK	5		ns
t_9	Clk Unstable	Time CPUCLK remains valid after MODE signal goes LOW		0	ns
t_{10}	Clk Stable	Time required for the CPUCLK to become valid after last S0/clock edge		10	msec
t_{11}	Clk Unstable	Time the output oscillators remain valid after the S0, S1 or S2 select signals change value		0	ns
t_{12}	Clk Stable	Time required for the outputs to become valid after the S0, S1, or S2 signals change value		10	msec
t_{13}	Three-State	Time for the outputd to go into three-state mode after OE signal assertion		12	ns
t_{14}	Clk Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH		12	ns

Notes:
11. CPUCLK = 66 MHz and inputs at GND or V_{DD}.
12. Input capacitance is typically 10 pF, except for the crystal pads.

Switching Waveforms

Rise and Fall Times



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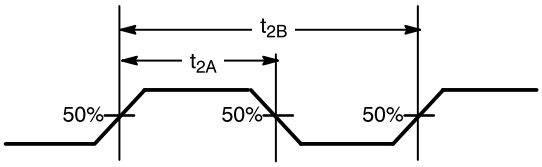
Duty Cycle Timing



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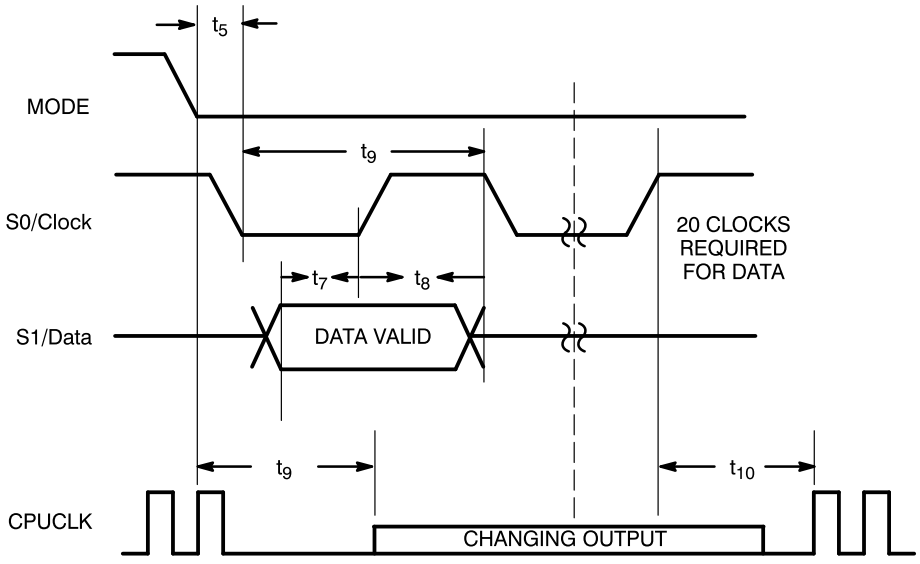
Serial Programming Timing



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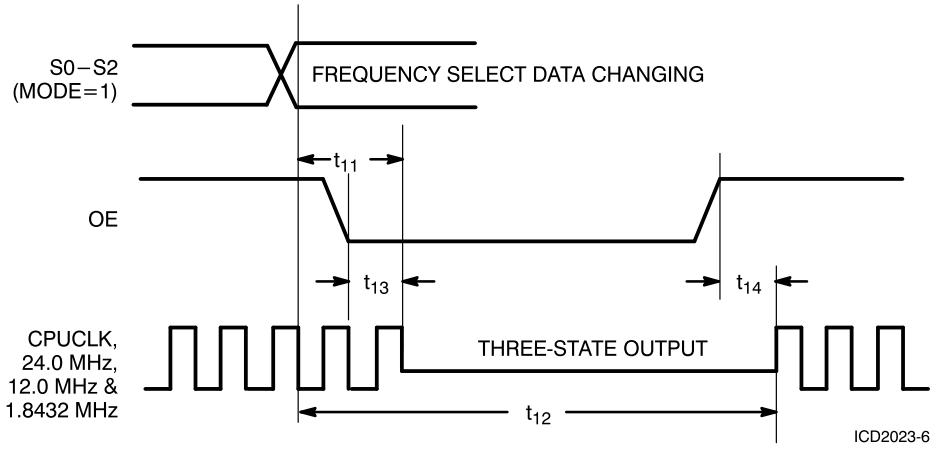
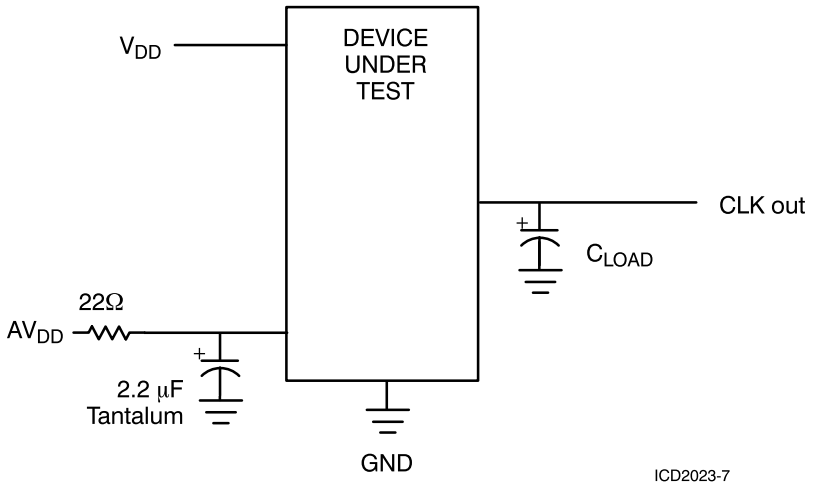
Switching Waveforms (continued)

State Timing



Test Circuit



Ordering Information[13]

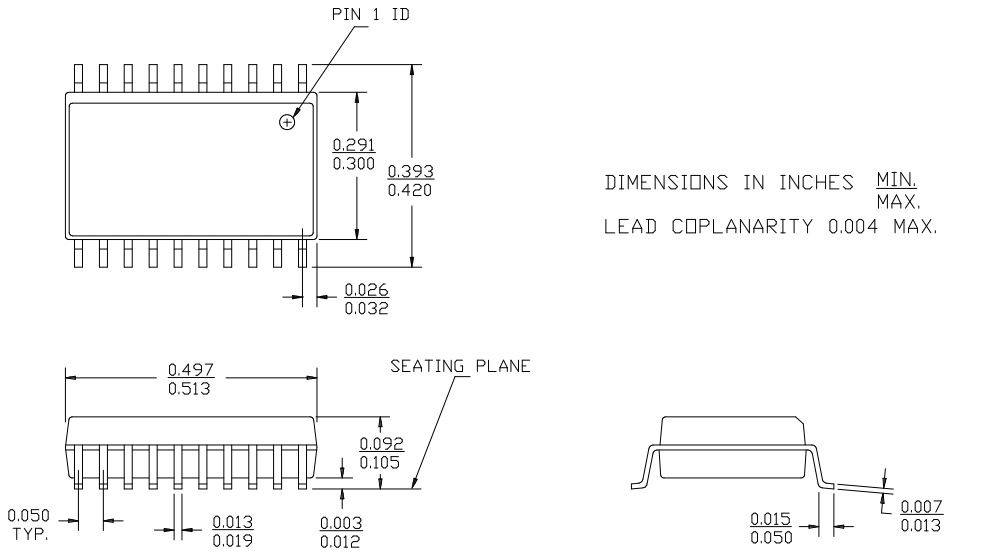
Ordering Code	Package Name	Package Type	Operating Range
ICD2023−	S5	20-Pin SOIC	Commercial[14]

Note:
13. Please contact your local Cypress representative.
14. 0°C to +70°C

Document #: 38−00397

Package Diagram

20-Lead (300-Mil) Molded SOIC S5



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