ICD2027

PC Motherboard Clock Generator

Features

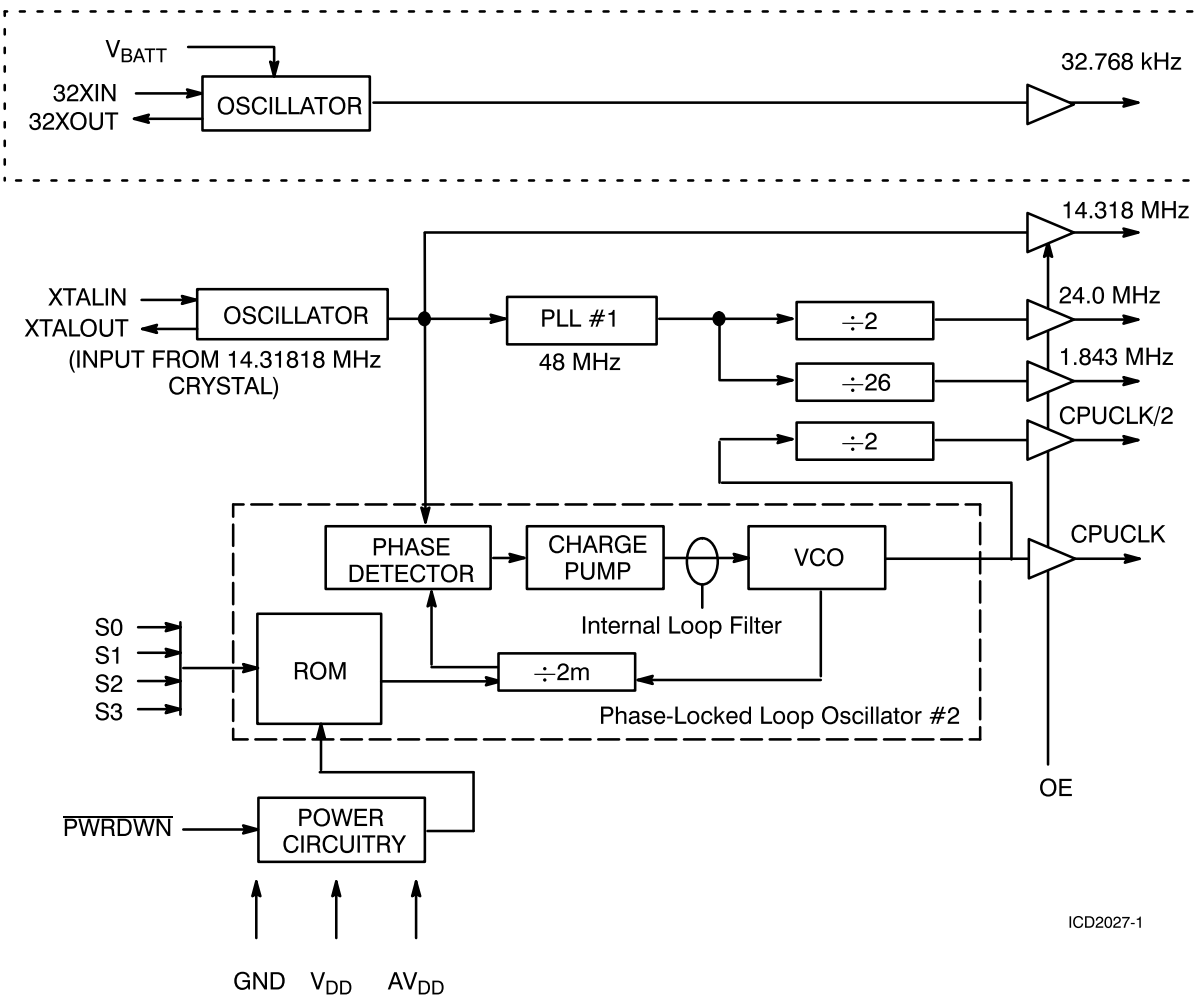
- **Six clock outputs handle all clocking requirements for personal computer motherboards**
- **Phase-locked loop oscillator input derived from single 14.31818 MHz crystal**
- **Frequency range: 760 kHz to 100 MHz with 50% duty cycle**
- **Two power-down modes—hardware pin and software programmable**
- **Concurrent and low skew ÷1 and ÷2, CPUCLK outputs**
- **Ideally suited for desktop PC, laptop, and notebook applications**
- **Battery input maintains 32.768 kHz clock during power-down**
- **Three-state oscillator control disables outputs for test purposes**
- **Sophisticated internal loop-filter requires no external components**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 20-pin SOIC package configuration**

Functional Description

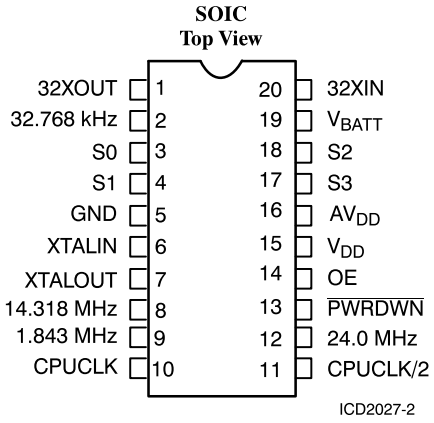
A modern personal computer motherboard often requires as many as seven different crystal can oscillators per printed circuit board. A new family of frequency synthesis parts from Cypress/IC Designs replaces the large number of oscillators required to build such multifunction motherboards. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2027 PC Motherboard Clock Generator offers two oscillators, two phase-locked loops, and six different outputs in a single package. Four of the outputs are of a fixed value, while the other two may be changed “on the fly” to any one of 16 preset frequency values between 760 kHz and 100 MHz. The ICD2027 is ideally suited for use in laptop/notebook designs due to its dual power-down modes. The ICD2027 also requires no support from the motherboard chip set and outputs all six frequencies concurrently.

Block Diagram



Pin Configuration



Pin Summary

Name	Number	Description
32XOUT[1]	1	Oscillator output to a 32.768 kHz parallel-resonant crystal
32.768 kHz	2	32.768 kHz clock output
S0	3	Input select line 0 for CPUCLK (pin has internal pull-down)
S1	4	Input select line 1 for CPUCLK (pin has internal pull-down)
GND	5	Ground
XTALIN[1]	6	Reference Oscillator input for all internal phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT[1]	7	Oscillator Output to a reference crystal.
14.318 MHz	8	14.31818 MHz clock output
1.8432 MHz	9	1.8432 MHz clock output
CPUCLK	10	CPUCLK programmable clock output (See *Table 1* for values.)
CPUCLK/2	11	Half the frequency of CPUCLK. Output is phase-coherent with the CPUCLK output.
24.0 MHz	12	24.0 MHz clock output
$\overline{\text{PWRDWN}}$	13	Puts device in Power-Down mode when signal is pulled LOW (pin has internal pull-down)
OE	14	Output Enable three-states output when signal is LOW (pin has internal pull-up)
V_{DD}	15	+5V to I/O ring
AV_{DD}	16	+5V to analog core
S3	14	Input select line 3 for CPUCLK (pin has internal pull-down)
S2	18	Input select line 2 for CPUCLK (pin has internal pull-down)
V_{BATT}	19	+2 to +5V for battery backup operation
32XIN[1]	20	Oscillator input from 32.768 kHz crystal

Note:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

General Considerations

CPUCLK Selection

CPUCLK is the selectable output. It uses four select lines (S0, S1, S2, S3) to select 1 of 16 different preset frequencies, as shown in *Table 1* (Reference Frequency = 14.31818 MHz).

Table 1. CPUCLK ROM Selection Outputs[2]

S3	S2	S1	S0	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)
0	0	0	0	0.7950[3]	$f_{(REF)}/18$	0
0	0	0	1	0.7950	$f_{(REF)}/18$	0
0	0	1	0	33.3000	33.2981	57
0	0	1	1	0.7600	0.7599	75
0	1	0	0	2.0000	2.0003	167
0	1	0	1	3.0000	2.9968	1057
0	1	1	0	8.0000	8.0013	167
0	1	1	1	10.0000	10.0227	2273
1	0	0	0	20.0000	20.0455	2273
1	0	0	1	24.0000	23.9747	1057
1	0	1	0	32.0000	32.0053	167
1	0	1	1	40.0000	40.0909	2273
1	1	0	0	50.0000	50.0000	0
1	1	0	1	66.6000	66.5962	57
1	1	1	0	80.0000	80.1818	2273
1	1	1	1	100.0000	99.8182	1818

Fixed Frequency Operation

Table 2 describes each output.

Table 2. Fixed Frequency Oscillators

Output Clock Function	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)
Real-Time Clock[4]	32.768 kHz	32.768 kHz	0
System Bus[5]	14.31818	14.31818	0
Floppy Disk Clock	24.00000	23.97470	1058
Serial Port	1.84320	1.84420	1058

Notes:
2. The select lines have internal pull-downs so that in a system power-down situation, the power-down mode is chosen in the CPUCLK table as the default. Therefore, upon power-up, one of the select lines must be pulled HIGH.
3. Soft power-down mode.
4. Pass-through 32.768 kHz XTAL.
5. Pass-through 14.31818 MHz XTAL.

Power-Down Operation

There are two power-down modes within the ICD2027. The first is the hardware mode. When Pin 13 is pulled LOW ($\overline{PWRDWN}$=0), the part is immediately forced into its lowest power mode. This shuts down everything but the 32.768-kHz oscillator and its output. All power is now supplied by the V_{BATT} input. For minimum power consumption in power-down mode, all select lines should be set LOW and OE should be set HIGH

The second mode is a programmable soft power-down mode. This mode shuts down the two phase-locked loops and all outputs except for the CPUCLK output, which runs at 795 kHz—a frequency sufficient to refresh dynamic RAMs (see *Table 3*).

Table 3. Soft Power-Down Mode (S0−S3=0000)

Output Signal	Status
32.768 kHz	32.768 kHz
CPUCLK	795.00 kHz
CPUCLK/2	(shutdown)
14.318 MHz	(shutdown)
1.8432 MHz	(shutdown)
24.000 MHz	(shutdown)

Three-State Output Operation

The OE signal, when pulled LOW, will three-state all the clock output lines (except 32.768 kHz). This supports Wired-OR connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The OE signal contains an internal pull-up; it can be left unconnected if three-state operation is not required.

Skew-Free ÷2 on CPUCLK/2

The CPUCLK/2 output is available concurrently as a ÷2 of the desired CPUCLK output. The ÷2 output is also closely matched in order to minimize the phase differences between the two outputs. Typical phase coherence is less than 1 ns of skew between the two outputs, with 2 ns guaranteed worst case.

V_{BATT}

The V_{BATT} input powers the Real-Time Clock Oscillator (RTC). The backup power is typically supplied by a 3V lithium battery; however, any voltage between 2V and 5V is acceptable. If the 32-kHz output is not used, all related inputs and outputs and V_{BATT} should be grounded.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential . . . . . −0.5V to +7.0V
DC Input Voltage . . . . . −0.5V to V_{DD} +0.5V
Storage Temperature . . . . . −65°C to +150°C
Max soldering temperature (10 sec) . . . . . 260°C
Junction temperature . . . . . 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{BATT}	Backup Battery Voltage	Typical = 3.0V	2.0	5.0	V
V_{IH}	Input HIGH Voltage	Except Crystal Inputs	2.0		V
V_{IL}	Input LOW Voltage	Except Crystal Inputs		0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
I_{IH}	Input HIGH Current	V_{IH} = 5.25V		150	µA
I_{IL}	Input LOW Current	V_{IL} = 0V		−250	µA
I_{OZ}	Output Leakage Current	(Three-state)		10	µA
I_{DD}	Power Supply Current	Inputs @ V_{DD} or GND	20	65	mA
I_{DD-PD}	Soft Power-Down Current			7.5	mA
I_{BATT}	Backup Battery Current	Typical = 5 µA		15	µA

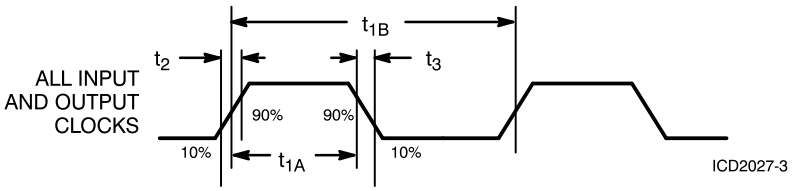
Switching Characteristics[6]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
f_{REF}	Reference Frequency	Reference input normal value		14.318		MHz
$t_{(REF)}$	Reference Period	1 ÷ $f_{(REF)}$		69.8		ns
t_1	Duty Cycle	Duty cycle for the output clock defined as $t_{1A} \div t_{1B}$	40%		60%	
t_2	Rise Time	Rise time for the outputs into a 25-pF load			4	ns
t_3	Fall Time	Fall time for the outputs into a 25-pF load			4	ns
t_4	Three-state	Time for the outputs to go into three-state mode after OE signal assertion			12	ns
t_5	clk Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH			12	ns
t_6	CPUCLK/2 Skew	Skew delay between CPUCLK and CPUCLK/2 outputs		1	2	ns
t_{freq1}	freq1 Output	Old frequency output				
t_{freq2}	freq2 Output	New frequency output				
t_7	$f_{(REF)}$ Mux Time	Time clock output remains HIGH while output muxes to reference frequency	$t_{(REF)}/2$		$3(t_{(REF)}/2)$	ns
t_8	t_{freq2} Mux Time	Time clock output remains HIGH while output muxes to new frequency value	$t_{freq2}/2$		$3/(t_{freq2}/2)$	ns
t_{MUXREF}		Time for VCO to settle between changes			6.2	msec

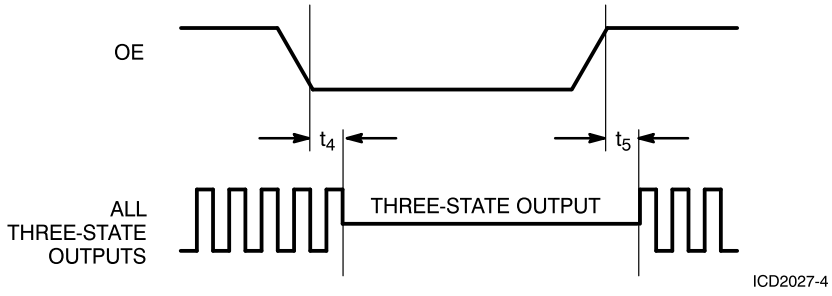
Notes:
6. Input capacitance is typically 10 pF, except for the crystal pads.

Switching Waveforms

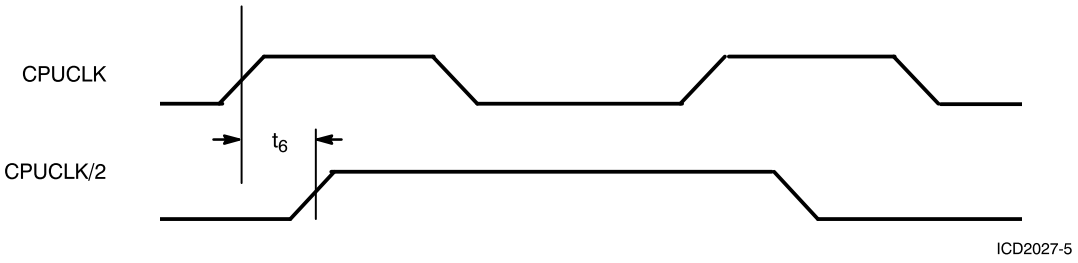
Rise and Fall Times



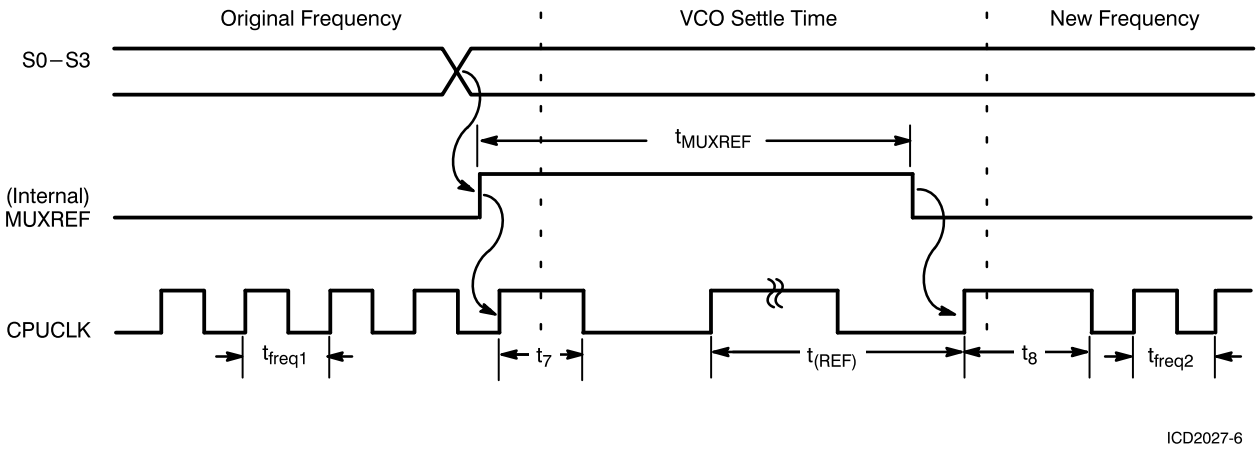
Three-State Timing



CPUCLK Skew



Select Timing



Ordering Information

Ordering Code	Package Name	Package Type	Temperature Range	CPUCLK ROM Option
ICD2027	S5	20-Pin SOIC	C=Commercial=0°C to +70°C	1

Example: Order ICD2027SC−1 for the ICD2027, 20-pin plastic SOIC, commercial temperature range device which uses the standard CPUCLK ROM Option 1 table of frequency decodes. Custom CPUCLK ROM decodes are available by special order. Please call your local Cypress representative.

Document #: 38−00399

Package Diagram

20-Lead (300-Mil) Molded SOIC S5