ICD2042A

Dual VGA Clock Generator

Features

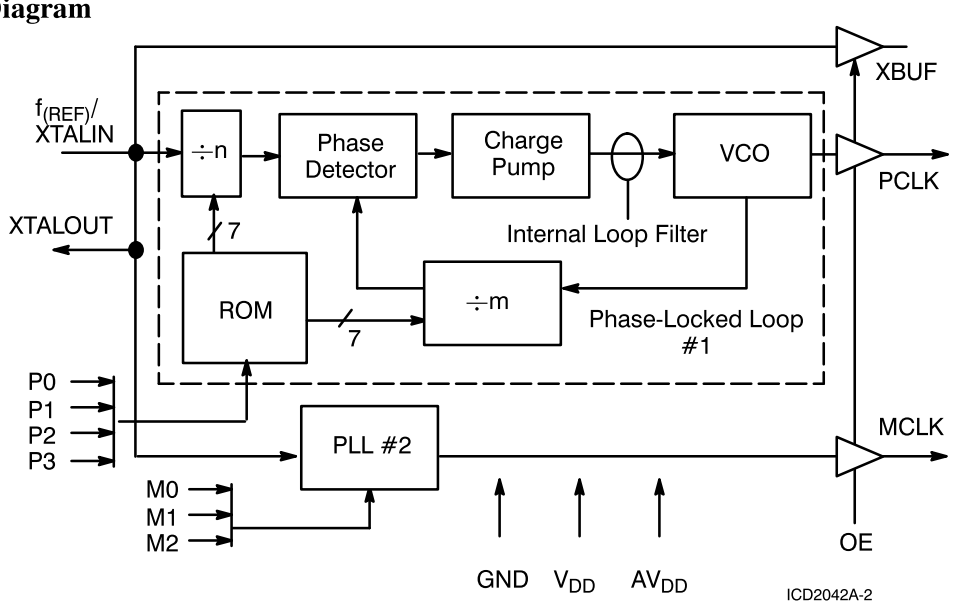
- **Three independent clock outputs: separate pixel and memory clocks and buffered reference clock**
- **Phase-locked loop output range of 1350 kHz − 120 MHz**
- **Phase-locked loop oscillator input derived from PC system bus or from single 14.318 MHz crystal**
- **Ideally suited for VGA, XGA, and 8514 graphics applications**
- **Sophisticated internal loop-filter requires no external components**
- **Three-state output control disables outputs for test purposes**
- **Change-on-the-fly frequency selection supports most popular VGA/8514 chip sets**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 16-pin SOIC package**

Functional Description

The proliferation of video standards, support for various monitors, increasing screen resolutions, and different memory speeds present in the DOS graphics community often require as many as six different crystal can oscillators per PC board. A new family of frequency synthesis parts from Cypress/IC Designs replaces the large number of these oscillators required to build such multi-function graphic boards as EGA, VGA, Super VGA, and 8514. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

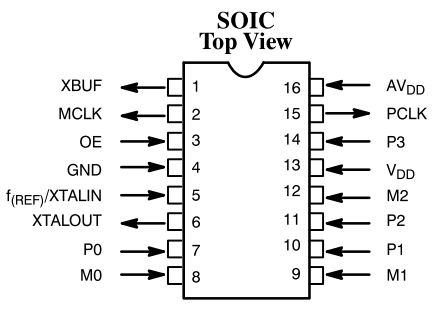
The ICD2042A Dual VGA Clock Generator supports new designs using the newer graphics chip sets which generate output frequency select information. The ICD2042A features two independent clock outputs for the pixel clock and the memory clock which are chosen via select lines. Additional features include three-stateable outputs and direct support for popular graphics chip set selection decodes.

Logic Block Diagram



ICD2042A-2

Pin Configuration



ICD2042A-1

Pin Summary

Name	Number	Description
XBUF	1	Buffered reference frequency output (14.318 MHz)
MCLK	2	Memory Clock output (see *Table 1*)
OE	3	Output Enable, three-states output when signal is LOW (pin has internal pull-up)
GND	4	Ground
$f_{(REF)}$/ XTALIN[1]	5	Reference Oscillator input for all internal phase-locked loops (nominally from a parallel-resonant 14.318-MHz crystal).
XTALOUT[1]	6	Oscillator output to a reference crystal. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.)
P0	7	Pixel Clock Select input—Bit 0 (internal pull-up)
M0	8	Memory Clock Select input—Bit 0 (internal pull-up)
M1	9	Memory Clock Select input—Bit 1 (internal pull-up)
P1	10	Pixel Clock Select input—Bit 1 (internal pull-up)
P2	11	Pixel Clock Select input—Bit 2 (internal pull-up)
M2	12	Memory Clock Select input—Bit 2 (internal pull-up)
V_{DD}	13	+5V to I/O Ring
P3	14	Pixel Clock Select input—Bit 3 (internal pull-down)
PCLK	15	Pixel Clock Output
AV_{DD}	16	+5V to Analog Core (special order: bond V_{DD} to AV_{DD} internally)

General Considerations

Design Recommendations

The ICD2061A, with its ability to program the output frequencies, is recommended for designs in which a fixed ROM would be inconvenient and/or the desired volume does not warrant a custom ROM.

The ICD2042A is currently a custom order only.

Pixel and Memory Clock Oscillator Selection

The output frequency value of the Pixel clock oscillator (PCLK) is selected by the four Pixel clock selection inputs: P0, P1, P2, and P3. This feature allows the ICD2042A to support different video configurations. The output frequency value of the Memory clock oscillator (MCLK) is selected by the three Memory clock selection inputs: M0, M1, and M2. The selection table is shown in *Table 1*.

At any time during operation, the select lines can be changed to select a different frequency. When this occurs, the internal phase-locked loop will immediately seek the newly selected frequency. During the transition period, the clock output will multiplex glitch-free to the reference signal until the PLL settles to the new frequency.

Normally, the MCLK select lines are hard-wired during manufacturing to correspond to the desired memory speed. A different memory clock frequency output may be generated by changing the memory select lines of the ICD2042A. The timing for this transition is shown in AC Characteristics.

Note:

1. For best accuracy, use a parallel-resonant crystal, asume C_{LOAD} = 17 pF.

Table 1. Memory Clock ROM Decode Options

M2	M1	M0	Word	2042−23	2042−24	2042−27
				Frequencies in MHz		
0	0	0	0	48.000	48.000	40.000
0	0	1	1	39.800	39.800	41.000
0	1	0	2	66.000	66.000	41.500
0	1	1	3	50.000	50.000	42.000
1	0	0	4	56.644	56.644	42.500
1	0	1	5	32.200	32.000	43.000
1	1	0	6	44.000	44.000	44.000
1	1	1	7	39.800	39.800	48.000

Three-State Output Operation

The OE signal, when pulled LOW, will three-state the MCLK, PCLK, and XBUF output lines. This supports procedures such as automated testing, where the clock must be disabled. The OE signal contains an internal pull-up but should be tied to V_{DD} if not used.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential . . . . . −0.5V to +7.0V
DC Input Voltage . . . . . −0.5V to V_{DD} +0.5V
Storage Temperature . . . . . −65°C to +150°C
Max soldering temperature (10 sec) . . . . . 260°C
Junction temperature . . . . . 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = − 4.0mA	V_{DD}−0.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage	Except crystal inputs	2.0		V
V_{IL}	Input LOW Voltage	Except crystal inputs		0.8	V
I_{IH}	Input HIGH Current	V_{IH} = V_{DD}−0.5V		150	µA
I_{IL}	Input LOW Current	V_{IL}= 0.5V		−250	µA
I_{OZ}	Output Leakage Current	(Three-state)		10	µA
I_{DD}	Power Supply Current	Inputs @ V_{DD} and GND		60	mA
I_{ADD}	Analog Power Supply Current			6	mA

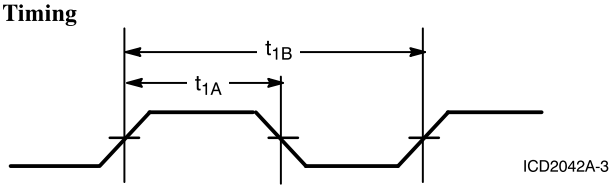
Switching Characteristics Over the Operating Range[2]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference Oscillator nominal value[3]	4	14.318	25	MHz
$t_{(REF)}$	Ref Clock Period	1 ÷ $f_{(REF)}$	40	69.8	250	ns
t_1	Input Duty Cycle	Duty cycle for the input oscillators defined as t_{1A} ÷ t_{1B}	25%	50%	75%	
t_2	Output Period	Clock output time period	8.3 120 MHz		2857 350 KHz	ns
t_3	Output Duty Cycle	Duty cycle for the outputs defined as t_{1A} ÷ t_{1B} (measured at 2.5V)	40%		60%	
t_4	Rise Time	Rise time for the outputs into a 25 pF load			4	ns
t_5	Fall Time	Fall time for the outputs into a 25 pF load			4	ns
t_6	Three-State	Time for the outputs to go into three-state mode after OE signal deassertion			12	ns
t_7	Clk Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH			12	ns
t_{MUXREF}	Clk Stable	Time required for the outputs to become valid after P0−P3 or M0−M2 select signals change value	3.4	5	6.9	msec
t_8	$f_{(REF)}$ Mux Time	Time clock output remains HIGH while output muxes to reference frequency	$t_{(REF)}/2$		$3(t_{(REF)})/2$	ns
t_9	t_{freq2} Mux Time	Time clock output remains HIGH while output muxes to new frequency value	$t_{freq2}/2$		$3(t_{freq2})/2$	ns

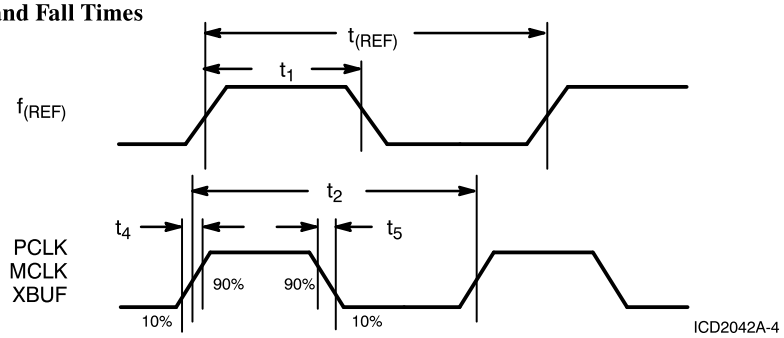
Notes:
2. Input capacitance is typically 10 pF, except for the crystal pads.
3. Different reference frequencies require a custom ROM; standard parts use 14.31818 MHz, unless otherwise stated.

Switching Waveforms

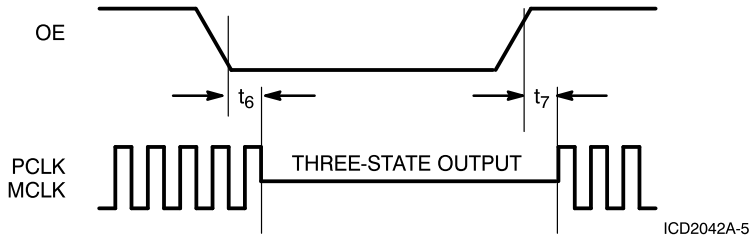
Duty Cycle Timing



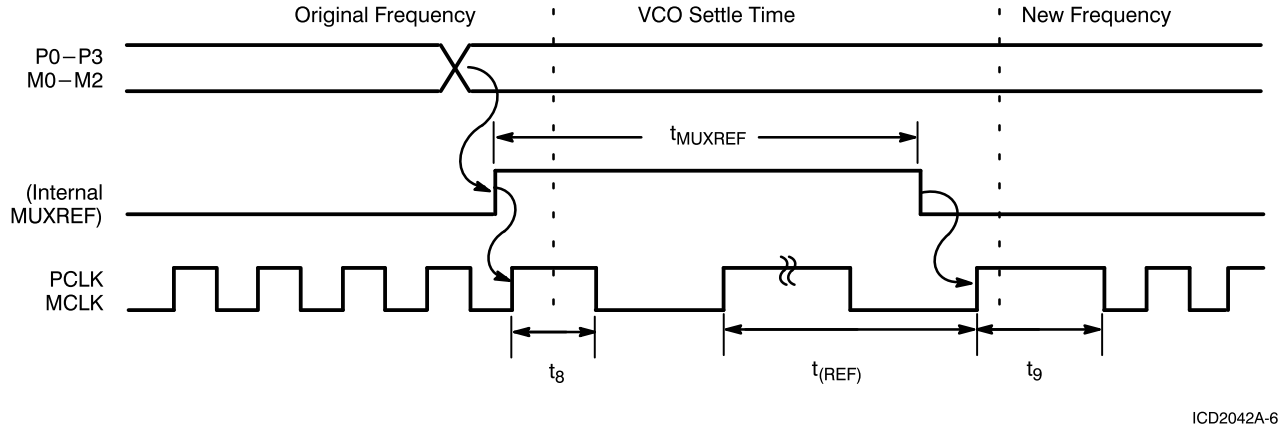
Rise and Fall Times



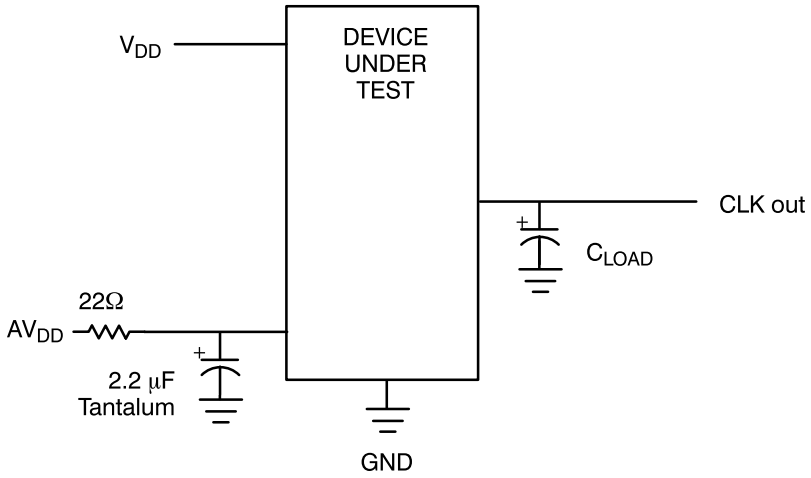
Three-State Timing



Selection Timing



Test Circuit



Ordering Information

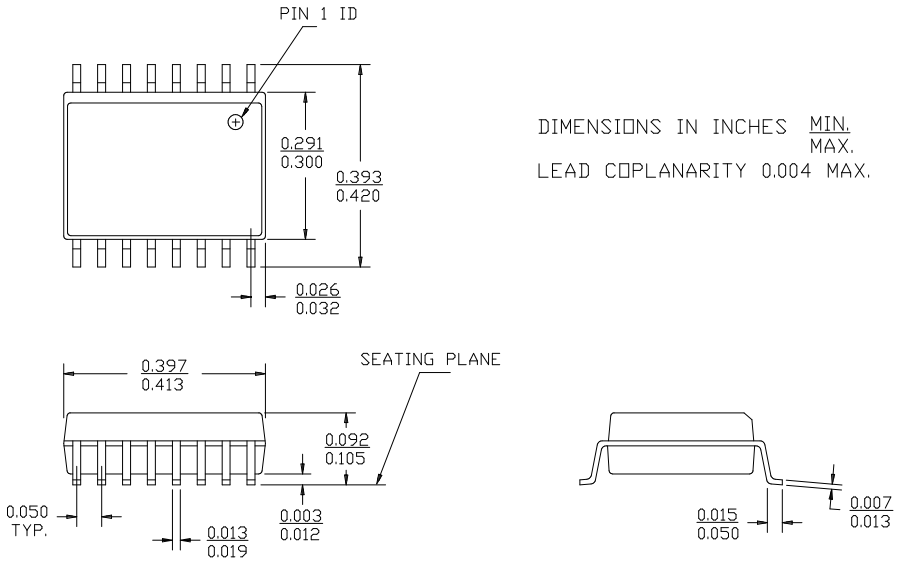
Ordering Code	Package Name	Package Type	Operating Range
ICD2042A	S1	16-Pin SOIC	Commercial[4]

Note:
4. 0°C to +70°C

Document #: 38−00402

Package Diagram

16-Lead Molded SOIC S1



ICD2042A-8