ICD2063

Programmable Graphics Clock Generator

Features

- **Second generation dual PLL graphics clock generator**
- **Compatible with the ICD2061A**
- **2 independent clock outputs:**
  - **— VCLK Output— 390 kHz – 135 MHz (100 MHz at 3.3V)**
  - **— MCLK Output 312 kHz – 100 MHz (80 MHz at 3.3V)**
- **Individually programmable PLLs using a highly reliable, Manchester-encoded, 21-bit serial data word**
- **2-pin serial programming interface allows direct connection to most graphics chip sets with no external hardware required**
- **2 advanced power-down capabilities**
- **Three-state oscillator control disables outputs for test purposes**
- **Phase-locked loop oscillator input derived from single 14.318 MHz crystal**
- **3.3V and 5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 16-pin SOIC package configuration**

Functional Description

The ICD2063 Dual Programmable Graphics Clock Generator features a fully programmable set of clock oscillators which can handle all frequency requirements of most graphics systems. The ICD2063 offers the selection ease of ROM-based clock chips and the versatility of serially programmable frequency synthesizers. It features both 3.3V and 5V operation with advanced power-down capabilities, making it ideally suited for the portable computer market.

The ICD2063 Dual Programmable Graphics Clock Generator offers two fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value between limits which depend on selected modes and operating voltage. The ICD2063 is ideally suited for any design where multiple or varying frequencies are required, replacing more expensive metal can oscillators or less functional ROM-based clock synthesizers.

While primarily designed for the graphics subsystem market, the programming versatility of the ICD2063 makes it ideal wherever two variable, yet highly accurate clock sources are required.

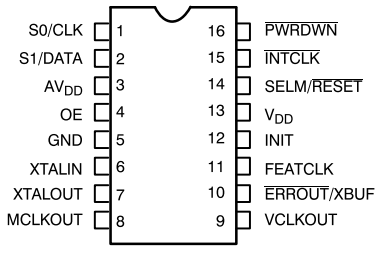
ICD2063 Changes from the ICD2061A

The ICD2063 revision of the ICD2061A is a complete mask redesign which includes many feature enhancements. The following major modifications have been implemented:

- **3.3V Operation**—The ICD2063 supports 3.3V operation in addition to 5V operation.
- **Expanded Register Set**—There are now 4 Video registers and 2 Memory registers. This allows better support for Windows NT drivers.
- **Expanded VCO Range**—The upper frequency limit has been increased to 135 MHz.
- **No Index Field Required**—The Serial Word now treats the Index Field (Mode Field) as a "Don't Care" bit region, for complete software compatibility with the ICD2061A.
- **Buffered Crystal Output** (Optional)—XBUF Output may be specified, replacing the $\overline{\text{ERROUT}}$ signal.
- **Smooth Frequency Transition**—The two phase-locked loops now transition smoothly from one frequency to another.
- **No MUXREF Required**—The necessity for the MUXREF procedure has been eliminated by the smooth frequency transition. For compatibility with the ICD2061A, there is an option which multiplexes a known output during frequency transitions. New to the ICD2063 is that the VCLK VCO is multiplexed to the MCLK output. See the *MUXREF Option* section for details.
- **Very High Frequency Resolution**—The MCLK Phase-Locked Loop Output can be multiplexed to the VCLK PLL Reference Input, thus enabling very high frequency resolution, at the expense of slightly higher jitter. See the *Extended VCLK Frequency Precision* section.
- **Reduced Register Initialization ROM**—The former INIT2 pin now selects between the 2 memory registers MREG0 and MREG1.
- **Hardware Reset** (Optional)—A hardware reset is available as an option, replacing the memory selection signal.

Pin Configuration

SOIC
Top View



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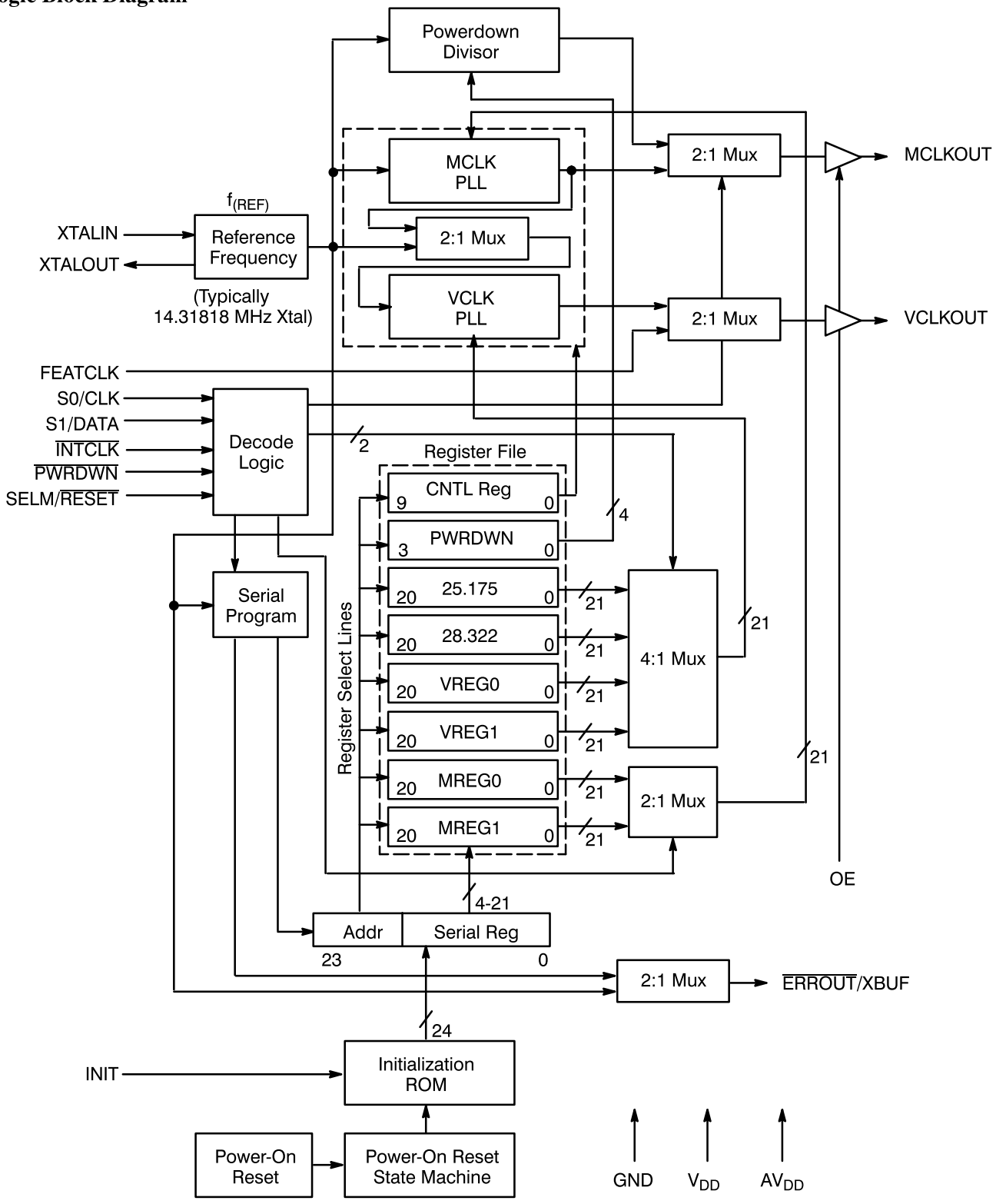
Logic Block Diagram



Pin Summary

Name	Number	Description
S0/CLK	1	Bit 0 (LSB) of frequency select logic, used to select PLL frequencies. Clock Input in serial programming mode. (Internal pull-down allows no-connect.)
S1/DATA	2	Bit 1 (MSB) of frequency select logic, used to select PLL frequencies. Data Input in serial programming mode. (Internal pull-down allows no-connect.)
AV_{DD}	3	+5V or 3.3V to Analog Core
OE	4	Output Enable. Three-states output when pulled LOW. (Internal pull-up allows no connect.)
GND	5	Ground
XTALIN[1]	6	Reference Oscillator input for all phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT[1]	7	Oscillator Output to a reference crystal. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.)
MCLKOUT	8	Memory Clock output
VCLKOUT	9	Video Clock output
$\overline{\text{ERROUT}}$/ XBUF	10	Error Output: a LOW signals an error during serial programming −OR− Buffered Crystal Reference Output (selectable via configuration option)
FEATCLK	11	External clock input (Feature Clock) (Internal pull-up allows no-connect.)
INIT	12	Selects state of initialization ROM during power-up. See *Table 2*. (This pin has no internal pull-up or pull-down; it *must* be tied HIGH or LOW externally.)
V_{DD}	13	+5V or 3.3V to I/O Ring
SELM/$\overline{\text{RESET}}$	14	Selectable via configuration option: SELM—Selects 1 of 2 Memory Clock Output (MCLKOUT) frequencies (see *Register Selection* subsection *MCLKOUT*) $\overline{\text{RESET}}$—Hardware RESET control signal (see the *Power-On Reset, RESET, and Register Initialization* section)
$\overline{\text{INTCLK}}$	15	Selects the Feature Clock external clock input as VCLKOUT output (Internal pull-up allows no-connect.) (See *Table 3*.)
$\overline{\text{PWRDWN}}$	16	Power-down pin (active LOW) (Internal pull-up allows no-connect if power-down operation not required. See *Power Management Issues* for specific details concerning the use of this pin.)

Register Definitions

Register File

The Register File consists of the following registers and their respective addresses in the Serial Data register:

Table 1. Register Addressing[2]

A2	A1	A0	Register	Usage
0	0	0	25.175 MHz	Fixed Video Clock Frequency
0	0	1	28.322 MHz	Fixed Video Clock Frequency
0	1	0	VREG0	Programmable Video Clock Register 0
0	1	1	MREG0	Programmable Memory Clock Register 0
1	0	0	PWRDWN	Divisor for Power-Down mode
1	0	1	VREG1	Programmable Video Clock Register 1
1	1	0	CNTL	Control Register
1	1	1	MREG1	Programmable Memory Clock Register 1

Notes:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD}=17 pF.
2. All register values are preserved in power-down mode.

Power-On Reset, $\overline{\text{RESET}}$, and Register Initialization

On power-up the ICD2063 Clock Generator initializes all of its registers to a known state upon power-up. This is implemented by the Power-On initialization circuitry. Two Video Clock registers and two Memory Clock registers are initialized based on the state of the INIT pin at power-up.

The Power-On Reset function operates transparently to the video subsystem. It performs its initialization function and is cleared before the system Power-On Reset permits the system to begin its boot process. The INIT pin must be strapped to V_{DD} or GND.

If the $\overline{\text{RESET}}$ option on pin 14 is chosen, then this pin, when pulled LOW, forces the equivalent of a Power-On Reset operation: the registers are reloaded with the contents of the initialization ROM (depending on the state of the INIT pin).

The various registers are initialized as shown in *Table 2* (all frequencies in MHz).

Table 2. Register Initialization ROM

INIT Pin	25.175	28.322	VREG0	VREG1	MREG0	MREG1
0	25.175	28.322	36.000	44.900	40.000	40.000
1	25.175	28.322	40.000	65.000	45.000	45.000

Register Selection

VCLKOUT

The Video Clock output is controlled not only by the S0, S1, and $\overline{\text{INTCLK}}$ pins, but also by the $\overline{\text{PWRDWN}}$ and OE inputs. Additionally, the clock generator may be multiplexed with an external frequency input (FEATCLK) which corresponds to the IBM VGA Feature Clock standard. *Table 3* shows the VCLKOUT selection criteria.

Table 3. VCLKOUT Selection

OE	PWRDWN	$\overline{\text{INTCLK}}$	S1	S0	VCLKOUT
0	X	X	X	X	High-Z
1	0	X	X	X	Forced LOW
1	1	X	0	0	25.175 MHz
1	1	X	0	1	28.322 MHz
1	1	0	1	0	FEATCLK
1	1	1	1	0	VREG0
1	1	X	1	1	VREG1

The Clock Select pins S0 and S1 have a dual purpose. When these pins are performing serial download, the VCLKOUT signal remains unchanged (unless the currently selected register is the one being programmed). When the pins S0 and S1 are functioning as register selects, a timeout interval is required to determine whether the user desires register select or serial programming functionality. If serial programming was not started at the end of the timeout interval, new register selection occurs, at which point the frequency changes to a new value. See the *Serial Programming Architecture* section for selection and transition details.

MCLKOUT

The Memory Clock output (MCLKOUT) is selected by $\overline{\text{PWRDWN}}$, OE, and by—depending on which configuration is chosen—either the SELM input or the S0 and S1 inputs, as shown in *Tables 4* and *5*.

If the Memory Select option on pin 14 is chosen, then the SELM input is available to set MCLKOUT and the decode is defined as shown in *Table 4*.

Table 4. MCLKOUT Selection (Memory Select Mode)

OE	PWRDWN	SELM	MCLKOUT
0	X	X	High-Z
1	0	X	PWRDWN or LOW (depending on mode)
1	1	0	MREG0
1	1	1	MREG1

If the $\overline{\text{RESET}}$ option is chosen, the MCLKOUT and VCLKOUT are both selected using the S0 and S1 pins (MREG1 can *only* be selected when VREG1 is selected).

See the *Frequency Transition Options* section for more specifics.

Table 5. MCLKOUT Selection (Reset Mode)

OE	PWRDWN	$\overline{\text{INTCLK}}$	S1	S0	VCLKOUT	MCLKOUT
0	X	X	X	X	High-Z	High-Z
1	0	X	X	X	Forced LOW	PWRDWN or LOW (depending on mode)
1	1	X	0	0	25.175 MHz	MREG0
1	1	X	0	1	28.322 MHz	MREG0
1	1	0	1	0	FEATCLK	MREG0
1	1	1	1	0	VREG0	MREG0
1	1	X	1	1	VREG1	MREG1

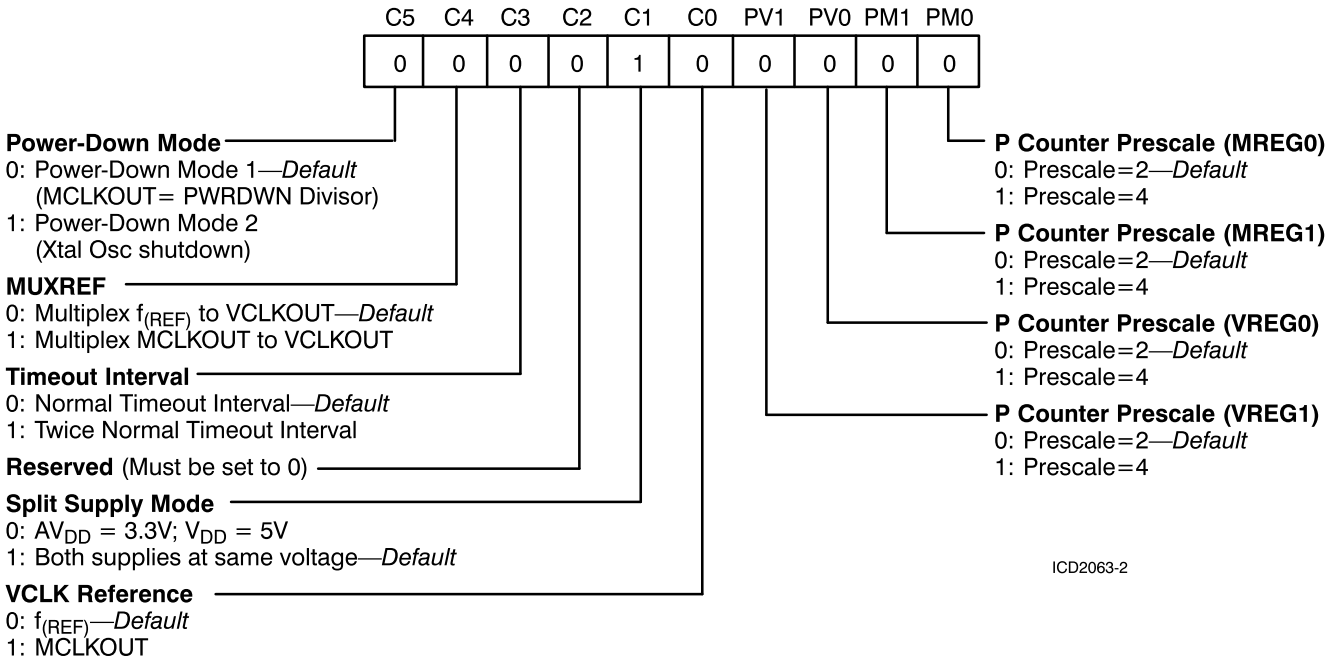


Figure 1. Control Register Definition

Control Register Definition

The Control Register (CNTL) allows the user to adjust various internal options. Most of these options are for special cases, and should have no applicability to standard graphics usage. The register word is defined in *Figure 1*.

VCLK Reference—This control bit determines whether the VCLK VCO uses $f_{(REF)}$ or the MCLK output as a reference. Refer to the *Extended VCLK Frequency Precision* section for more details.

Split Supply Mode—This control bit allows mixing 3.3V (AV_{DD}) and 5V (V_{DD}) supplies. The default is for both to be the same (5V or 3.3V). The alternative is AV_{DD} = 3.3V, V_{DD} = 5V. See the *3.3 Volt and 5 Volt Issues* section for more details. The purpose is to maintain duty cycle 50%.

Timeout Interval—The timeout interval is normally defined as in the *Switching Characteristics*. It is derived from the MCLK VCO, and if this VCO is programmed to certain extremes, then the timeout may be too short. If this control bit is set, then the timeout interval is doubled.

MUXREF (MUXREF Mode only)—This control bit determines which clock is multiplexed to the VCLKOUT output during frequency changes. While the VCLK VCO changes to a different frequency, a known clock is multiplexed to the output. The default is to multiplex the $f_{(REF)}$ reference frequency, but some graphic controllers cannot run as slow as $f_{(REF)}$. This bit, when set, allows the MCLK to be used as an alternative frequency.

Power-Down Mode—This control bit determines which Power-Down Mode the $\overline{\text{PWRDWN}}$ pin will implement. The default (Power-Down Mode 1) forces the MCLKOUT signal to be a function of the PWRDWN register. Power-Down Mode 2 turns off the crystal oscillator and disables all outputs. There is a more detailed description in the section entitled *Power Management Issues*.

P Counter Prescale (VREG0, VREG1, MREG0, MREG1)—These control bits determine whether or not to prescale the P Counter value, which allows fine tuning the output frequency of the respective register. Prescaling is explained in more detail in the *Prescaling* section.

Serial Programming Architecture

The ICD2063 programming scheme is simple, yet impenetrable to accidental access. Because the only common denominator between most VGA and 8514 controllers is a few clock select pins, these have to perform the dual functions of clock selection and serial programming. The Serial Program Block (See ICD2063 Logic Block Diagram) contains several components: a Serial Unlock Decoder (containing the unlocking mechanism and Manchester decoder), a watchdog timer, the Serial Data register and a Demultiplexer to the Register File (see *Figure 2*).

Unlocking Mechanism

The Unlocking Mechanism watches for an initial break sequence, detailed in *Figure 3*.

The initial unlock sequence consists of at least five LOW-to-HIGH transitions of CLK with DATA HIGH, followed immediately by a single LOW-to-HIGH transition of CLK with DATA LOW. Following this unlock sequence, the encoded serial data is clocked into the Serial Data register.

Note that the ICD2063 may not be serially programmed when in Power-Down Mode.

Watchdog Timer

Following any transition of CLK or DATA, the watchdog timer is reset and begins counting. Throughout the entire programming process, the watchdog timer ensures that there is a transition on CLK or DATA within the timeout specification (of 2 msec—see *Switching Characteristics*.) If a timeout does occur, the lock mechanism is rearmed and the current data in the Serial Data register is ignored.

Since the VCLK registers are selected by the S0 or S1 bits, and since any change in their state may affect the resultant output frequency, new data input on the Selection Bits is only permitted

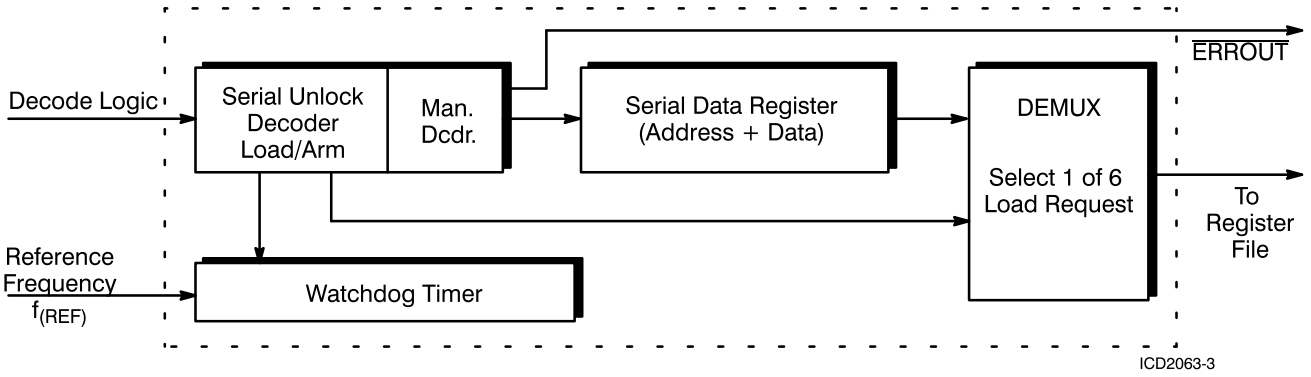


Figure 2. Serial Programming Block Diagram

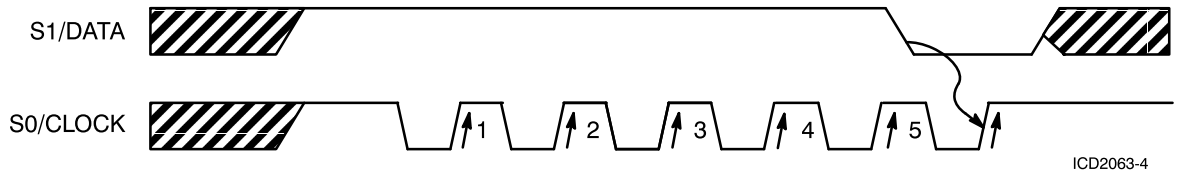


Figure 3. Unlock Sequence

to pass through to the Decode Logic after the Watchdog Timer has timed out. This delay of S0 and S1 data permits a serial program cycle to take place without affecting the current register selection. The process of serial programming has no effect on the performance of the graphics subsystem. Note that there is a latency amounting to the duration of the Watchdog Timer before any new register selections take effect.

Serial Data Register

The serial data is clocked into the Serial Data register in the order shown in *Figure 4*.

The serial data is sent using a modified Manchester-encoded data format. This is defined as:

1. An individual data bit is sampled on the rising edge of CLK.
2. The complement of the data bit must be sampled on the previous falling edge of CLK.
3. The Set-Up and Hold Time requirements must be met on both CLK edges.
4. The unlock sequence, start, and stop bits are not Manchester-encoded.

For specifics on timing, see the "Serial Programming Timing" section in the switching waveforms..

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit (which also functions as a load strobe to transfer the data from the Serial Reg into the desired register). For the VCO registers (VREG0−1, MREG0−1), the data is made up of 4 fields: D[20:18] = Mode (formerly Index); D[17:11]=P'; D[10:8]=Post-VCO Divider; D[7:1]=Q'. (See the *Programming the ICD2063* section for more details on the VCO data word.) For the other registers with fewer than 21 bits (PWRDWN, CNTL), the upper bits are used (starting with the MSB). A total of 24 bits must always be loaded into the Serial Data Register (or an error is

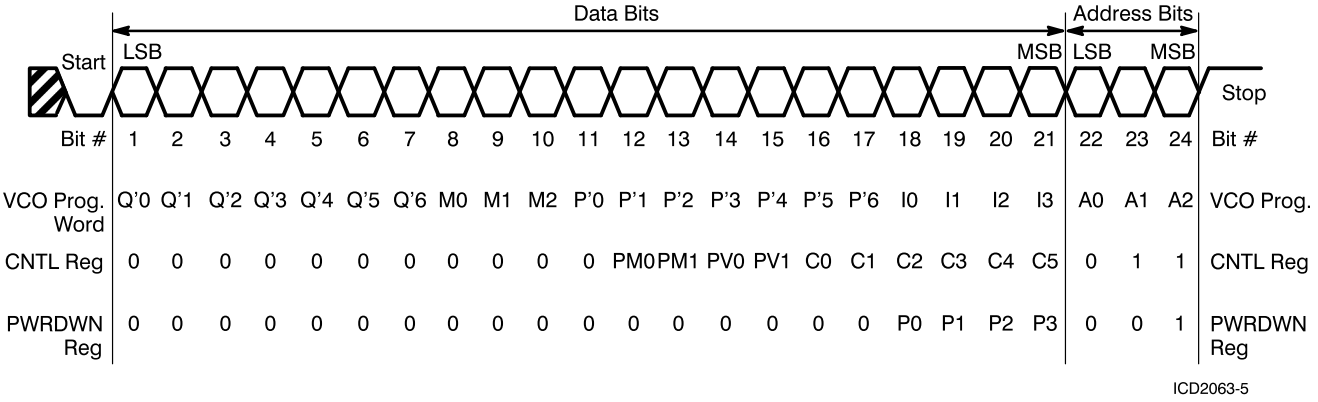


Figure 4. Serial Data Timing

issued). Undefined bits should always be set to zero to maintain software compatibility with future enhancements.

Following the entry of the last data bit, a stop bit or Load command is issued by bringing data HIGH and toggling CLK HIGH-to-LOW and LOW-to-HIGH. The unlocking mechanism then automatically rearms itself following the load. Only when the watchdog timer has timed out are the S0 and S1 selection pins permitted to return to their normal register select function.

Note that the Serial Data register that receives the address and data bits is exactly the correct length to accept the data being sent. The stop bit is used as a load command that passes the Serial Data register contents on to the register file location indicated by the address bits. If a stop bit is not received after the Serial Data register has been filled, but rather more valid encoded data is received, then all of the received serial data is ignored, the unlocking mechanism rearmed, and an error is issued. The device counts the serial data clock edges to know exactly when the serial buffer is full, and thus to know which bit is the stop bit. Following the stop bit, the unlocking mechanism rearms itself. If corrupt data is detected (i.e., incorrectly Manchester-encoded data), then the unlocking mechanism is rearmed, the serial counter reset, all received data ignored, and $\overline{\text{ERROUT}}$ is asserted.

$\overline{\text{ERROUT}}$ Operation

The $\overline{\text{ERROUT}}$ signal is used to report when a program error has been detected internally by the ICD2063. The signal stays active until the next unlock sequence.

Figure 5 shows the basic mechanism used to detect valid and erroneous serial data. Note that the circuit must have different values on the rising and falling edge when sampling the falling edge first. Valid data is read on the rising edge of CLK.

The $\overline{\text{ERROUT}}$ signal is invoked for any of the following error conditions: incorrect start bit, incorrect Manchester encoding; incorrect length of data word; incorrect stop bit; timeout.

Note that if there is no input pin available on the target VGA controller chip to monitor $\overline{\text{ERROUT}}$, a software routine which counts VSYNC pulses in order to measure output frequency may be used as a determination of programming accuracy.

Note also that the $\overline{\text{ERROUT}}$ signal is an order option. If the XBUF option is chosen instead, then $\overline{\text{ERROUT}}$ is not available, and the user may want to implement the above technique to verify that the desired programming did indeed take place.

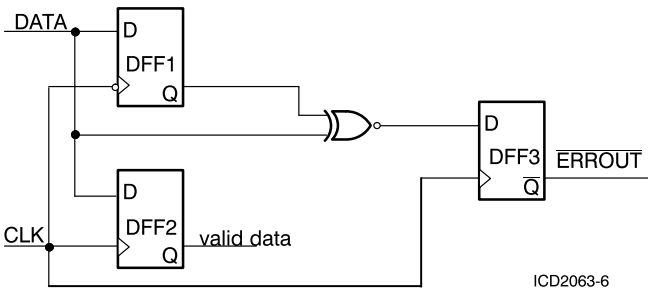


Figure 5. Serial Data Timing

Programming the ICD2063

The desired output frequency is defined via a serial interface, with a 21-bit number shifted in. The ICD2063 has two programmable oscillators, requiring a 21-bit programming word (W) to be loaded into each channel's respective registers independently. This word contains 4 fields:

Table 6. Programming Word Bit Fields

Field	# of bits	Notes
Mode (I)	4	MSB (Most Significant Bits)
P Counter value (P')	7	
Post-VCO Divisor (M)	3	
Q Counter value (Q')	7	LSB (Least Significant Bits)

The frequency of the Programmable Oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P' = P - 3$$
$$Q' = Q - 2$$
$$f_{(VCO)} = (\text{Prescale} \times f_{(REF)} \times P/Q)$$

where $f_{(REF)}$=Reference frequency (between 1 MHz−60 MHz; typically 14.31818 MHz) and Prescale=2 or 4 (default is 2, defined by CNTL Reg).

Note that if a reference frequency other than 14.31818 MHz is used, then the initially loaded ROM frequencies will not be correct.

Table 7 lists the various limits for $f_{(VCO)}$.

Table 7. VCO Frequency Ranges

	5 Volt Operation	3.3 Volt Operation
VCLK PLL	50 MHz − 135 MHz	50 MHz − 100 MHz
MCLK PLL	40 MHz − 100 MHz	40 MHz − 80 MHz

For lower output frequencies, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO divisor is selected by setting the values of the Post-VCO Divider field (M). See *Table 8*.

Table 8. Post-VCO Divider (M)

M	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The Mode Field (I), formerly the Index Field, is included for historical reasons to preserve software compatibility with the ICD2061A. In the ICD2063, it is only used for a few special circumstances, as detailed in the following paragraphs.

Table 9. Index Field (I)

I	VCLK VCO	MCLK VCO
0000	50.0 − 51.0	50.0 − 51.0
0001	51.0 − 53.2	51.0 − 53.2
0010	53.2 − 58.5	53.2 − 58.5
0011	58.5 − 60.7	58.5 − 60.7
0100	60.7 − 64.4	60.7 − 64.4
0101	64.4 − 66.8	64.4 − 66.8
0110	66.8 − 73.5	66.8 − 73.5
0111	73.5 − 75.6	73.5 − 75.6
1000	75.6 − 80.9	75.6 − 80.9
1001	80.9 − 83.2	80.9 − 83.2
1010	83.2 − 91.5	83.2 − 91.5
1011	91.5 − 100.0	91.5 − 100.0
1100	100.0 − 120.0	100.0 − 120.0
1101	100.0 − 120.0	100.0 − 120./0
1110	VCLK VCO is turned off and output is forced LOW	Ignored[3]
1111	VCLK is turned off and both channels run from the same MCLK VCO	Ignored[3]

The Mode Field was included to allow turning off the VCLK VCO and optionally multiplexing the MCLK VCO, then dividing down to the desired frequency. This will significantly reduce heterodyne jitter and is useful if the frequencies are 2^n multiples.

When the Index Field is set to 1111, VCLK is turned off and both channels run from the same MCLK VCO. To reduce jitter, do not run the two VCOs at integral multiples of each other. Hence, to obtain output clocks which are integral multiples of each other, multiplex the MCLK VCO to VCLKOUT and divide down to the desired frequency.

The MCLK VCO completely ignores the Mode Field values. For new designs, Cypress/IC Designs recommends the setting the Mode Field to 0000.

To assist with these calculations, Cypress/IC Designs provides *BitCalc* (Part #ICD/BCALC), a Windows™ program that automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers.

Programming Constraints

Table 10 shows the primary programming constraints of which the user must be aware:

Note:

3. In MUXREF mode, the memory clock cannot be changed—neither by the selects nor by reprogramming—because the VCLK is shut down and the MCLK is multiplexed to VCLK..

Table 10. Programming Constraints

Parameter	Minimum	Maximum
$f_{(REF)}$	1 MHz	60 MHz
$f_{(REF)}/Q$	200 kHz	1 MHz
$f_{(VCO)}$ (VCLK)	5V: 50 MHz 3.3V: 50 MHz	5V: 135 MHz 3.3V: 100 MHz
$f_{(VCO)}$ (MCLK)	5V: 40 MHz 3.3V: 40 MHz	5V: 100 MHz 3.3V: 80 MHz
Q	3	129
P	4	130

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed here for completeness' sake; however, by using the *BitCalc* program, these constraints become transparent.

Programming Example

The following is an example of the calculations *BitCalc* performs. This example assumes that Prescaling = 2, which is the default value.

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency and V_{DD} = 5:

Since 39.5 MHz<50 MHz, double it to 79.0 MHz. Set M to 001. Since I is a "Don't Care," set it to 0000. The result:

$f_{(VCO)}=79.0=(2 \times 14.31818 \times P/Q)$
$P/Q = 2.7587$

Several choices of P and Q are available:

Table 11. P&Q Value Pairs

P	Q	$f_{(VCO)}$ (MHz)	Error (PPM)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Choose (P, Q)=(80,29) for best accuracy (40 PPM).

Therefore:

P'=P−3=80−3=77=1001101 (4dH)
Q'=Q−2=29−2=27=0011011 (1bH)

and by concatenating I=0000, P'=1001101, M=001, Q'=0011011, we obtain the programming word

W=00001001101001001101 1 (01349bH)

The programming word W is then sent as a serial bit stream, LSB first. Appropriate start and stop bits must also be included as defined in the *Serial Programming Architecture* section.

Prescaling Example

For most users, the resolution of the ICD2063 in its default modes is sufficient. For those demanding greater precision, Prescale can be set to 4. This section provides an example.

Assume the desired VCLKOUT frequency is 100 MHz. *Table 12* compares the results of using the default prescaling value of 2 and the optional prescaling value of 4.

Table 12. Effects of Prescaling

Prescale	Desired Freq. (MHz)	Actual Freq. (MHz)	P	Q	Error (PPM)
2	100	99.84028	129	37	1600
4	100	99.99998	110	63	0

But this precision has its price, namely that the user now has to set and reset the Prescale Bits PS0−2 (corresponding to REG0−2), which involves loading a Control Word (taking care to preserve the current values of the other Control Bits), before the VCO Program Word can be loaded. Once the appropriate Prescale Bits are set, then frequency programming can proceed as before. However, if it is desired to program a new frequency without prescaling, a new Control Word must first be loaded with the proper bits set, with the precautions noted above.

To summarize, the sequence is:

1. Set the Prescale bits (load a Control Word)
2. Program the VCO (load a Program Word)

Note that care must be taken not to change the Prescale Bit of the currently active register: The results will be unpredictable at best, and it could cause the VCO to go out of lock.

Extended VCLK Frequency Precision

An optional mode set in the CNTL register allows the VCLK PLL to use the MCLK PLL as its reference frequency instead of $f_{(REF)}$. The advantage is that, by proper tuning of the input reference, *very* fine frequency control is possible on the output of VCLK.

Just about any desired value can be achieved with worst-case precision of less than 5 ppm.

The reference frequency oscillator is used to drive the MCLK PLL, which is then fed internally to the VCLK PLL to generate the desired signal. However, please note the following:

- **No usable MCLK output**—This method essentially uses two PLLs to derive a single output, so that the MCLK output will probable be meaningless. Therefore, this method is probably not suited to normal VGA graphics applications.
- **Some increased jitter**—The trade-off associated with deriving the VCLK PLL reference from another PLL is that the MCLK+VCLK combination will tend to exhibit more jitter than a single PLL with a crystal-controlled reference—but the jitter should stay below 1 ns.
- **More challenging programming model**—Another trade-off of having 21 bits each to define both the reference frequency and the output is that it makes finding the optimum 2 programming words an iterative process. To aid in these calculations, Cypress/IC Designs strongly recommends using *BitCalc*, a utility designed to help in this analysis.

Power Management Issues

Power-Down Mode 1

The ICD2063 contains a mechanism to reduce the quiescent power when stand-by operation is desired. In Power-Down Mode 1 (invoked by pulling the $\overline{\text{PWRDWN}}$ signal LOW and having the proper CNTL register bit set to zero), both VCOs are shut down, the VCLKOUT output is forced LOW, and the MCLKOUT output is set to a user-defined low-frequency value to refresh dynamic RAM.

The power-down MCLKOUT value is determined by the following equation:

$MCLKOUT_{Power\text{-}Down} = f_{(REF)} \div$ (PWRDWN Reg Divisor Value)

The Power-Down register divisor is determined according to the following 4-bit word programmed into the PWRDWN register. (See *Table 13*.)

Table 13. PWRDWN Register Programming

PWRDWN bits				PWRDWN Register Value (Hex)	Power-Down Divisor	$MCLKOUT_{Power\text{-}Down}$ ($f_{(REF)}$=14.31818 MHz)
P3	P2	P1	P0			
0	0	0	0	0	N/A	N/A
0	0	0	1	1	32	447.4 kHz
0	0	1	0	2	30	477.3 kHz
0	0	1	1	3	28	511.4 kHz
0	1	0	0	4	26	550.7 kHz
0	1	0	1	5	24	596.6 kHz
0	1	1	0	6	22	650.8 kHz
0	1	1	1	7	20	715.9 kHz
1	**0**	**0**	**0**	**8**	**18 (default)**	**795.5 kHz**
1	0	0	1	9	16	894.9 kHz
1	0	1	0	A	14	1.023 MHz
1	0	1	1	B	12	1.193 MHz
1	1	0	0	C	10	1.432 MHz
1	1	0	1	D	8	1.790 MHz
1	1	1	0	E	6	2.386 MHz
1	1	1	1	F	4	3.580 MHz

On power-up, the value of the PWRDWN register is loaded with a default value of 8 (1000 binary), which yields an MCLKOUT frequency of 795 kHz (14.31818/18). The default mode is Power-Down Mode 1.

Note that the ICD2063 may not be serially programmed when in Power-Down Mode.

Power-Down Mode 2

If there is no need for any output during power-down operation, then an alternate Power-Down Mode is available, which will completely shut down all outputs and the reference oscillator, yet still preserve all register contents. This results in the absolute least power consumption.

Power-Down Mode 2 is invoked by first programming the power-down bit in the CNTL register, and then pulling the $\overline{\text{PWRDWN}}$ pin LOW.

The XTALIN pin is forced LOW; therefore if an external reference clock is used instead of a crystal, it must be stopped LOW.

The $\overline{\text{PWRDWN}}$ Pin

This pin has a standard internal pull-up during normal operation. When the user pulls it down to invoke Power-Down Mode 1 or 2, the normal pull-up resistor is dynamically switched to a weak pull-up, which significantly reduces power consumption. If, after pulling this pin LOW, the pin is allowed to float, the weak pull-up will gradually cause the signal to rise, enabling the normal pull-up, and will eventually turn the device back on.

Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: I=C • V • f, where:

I=current (in mA)
C=Load capacitance (max., 25 pF)
V=output voltage (usually 5V or 3.3V)
f=output frequency (in MHz)

To calculate total operating current, sum the following terms:

$I_{(VCLKOUT)} \Rightarrow C \bullet V \bullet f_{(VCLK)}$
$I_{(MCLKOUT)} \Rightarrow C \bullet V \bullet f_{(MCLK)}$
$I_{(XBUF)}$ (if used) $\Rightarrow C \bullet V \bullet f_{(REF)}$
$I_{(Internal)} \Rightarrow$ 12 mA @ 5V; 8 mA @ 3.3V

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5 to 10 pF loading, depending on package type.

Table 14. Typical Current Drain Values

Frequency	Capacitive Load	Current (mA)	
		5 Volts	3.3 Volts
LOW	LOW	15	10
HIGH	LOW	40	26
HIGH	HIGH	65	44

When in Power-Down Mode 1, and using a 14.31818 MHz reference crystal, the power consumption will not exceed 7.5 mA @ 5V or 5 mA @ 3.3V. In Power-Down Mode 2, the power consumption will not exceed 50 µA @ 5V or 35 µA @ 3.3V.

3.3 Volt and 5 Volt Issues

The ICD2063 can function in mixed 5V/3.3V systems. The following discussion will attempt to address the various issues involved in mixed supply usage of the ICD2063.

V_{DD} and AV_{DD}

The ICD2063 has two isolated power leads: V_{DD} and AV_{DD}. Each supply may be independently run at either 3.3V or 5V. The V_{DD} rail supplies power to the I/O pad ring and core. All outputs and inputs are referenced to this voltage input. The device has a 4-Volt Detector which determines the pin's operating voltage and adjusts the threshold for the input pins. This guarantees that at either voltage, the inputs maintain TTL compatibility. If the voltage dynamically changes on the V_{DD} line (for instance going from 5V to 3.3V), the thresholds will be maintained properly.

The AV_{DD} pin supplies power to the VCO core. Since the VCO needs to know what the supply voltage is, a second 4-Volt Detector is placed on AV_{DD} to set the VCO operation properly. If the voltage dynamically changes on the AV_{DD} line (again, say from 5V to 3.3V), the VCOs will lose lock momentarily when the 4-Volt Detector triggers, and will re-lock to the desired value after a brief settling time. (See *Figure 6*.) This time should be less than 5 msec. This period of instability could cause a glitch in the output.

If a system requires dynamically changing from 5V to 3.3V and back (for example, some docking stations), and proper glitch-free output must be maintained during the transition period, then the AV_{DD} supply line should remain at 3.3 Volts while the V_{DD} pin can float to the desired levels. If this split mode is to be used, then the Split Supply Mode bit should be properly set in the Control register. (See the *Control Register Definition* section for more details.) Also note that, in this mode, the frequency range is limited to the narrower 3.3V values

Mixed Voltage Interfaces

The other issue which must be addressed is interfacing the ICD2063 into mixed-voltage systems. *Tables 15* and *16* depict the various configurations.

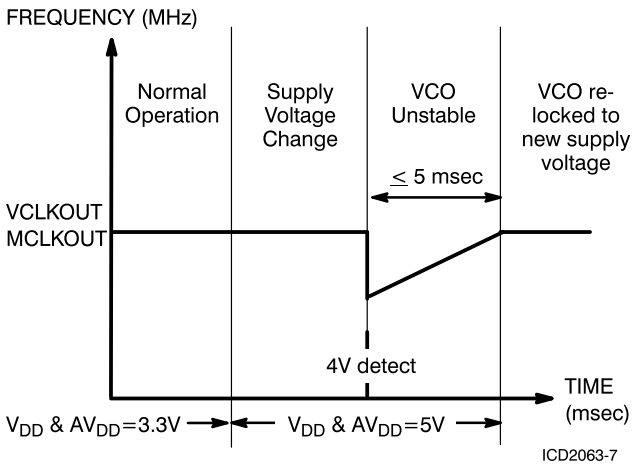


Figure 6. Effect of Supply Voltage Change to Clock Output

Table 15. Driving other Devices with the ICD2063

ICD2063 → Other Device		Status
5V	5V	OK
3.3V	5V	OK if driving TTL inputs; if driving CMOS inputs, then ICD2063 output will appear to have a low duty cycle.
5V	3.3V	Potential latch-up problems with other devices; will work if other device's input will accept $V_{IH}=V_{DD}+2V$.
3.3V	3.3V	OK

Table 16. Driving the ICD2063 with Other Devices

Other Device → ICD2063		Status
5V	5V	OK
3.3V	5V	OK
5V	3.3V	TTL outputs only; input to ICD2063 must not exceed $V_{DD}+0.3V$
3.3V	3.3V	OK

Frequency Transition Options

The ICD2063 may be configured for one of two frequency transition options: the Smooth Transition Option or the MUXREF Option (for compatibility with the ICD2061A).

Smooth Transition Option

Upon changing VCLK or MCLK, either by reprogramming the active register or by selecting a new register, the output will transition in one of two basic ways, depending on the post-divide values (Post-divide is used to divide down the VCO output to frequencies below the normal VCO operating range):

- **Normal Operation**—If the post-divide value (M) is the same for both frequencies (original and target), then the output will transition smoothly and linearly from the original to the target frequency, with no overshoot (see *Figure 7*).
- **Post-Divide Operation**—If the post-divide value (M) differs between the original and target frequencies, then the output behaves somewhat differently, but will never exceed the greater of the original and target frequencies.
  1. If the post-divide value decreases then, first, a smooth transition occurs to an intermediate frequency (equal to target frequency ÷ post divider value); second, the post-divide is changed to the new value, resulting in an instantaneous transition to the target frequency (see *Figure 8*).
  2. If the post-divide value increases then, first, the post-divide value is changed to the new value, resulting in an instantaneous transition to an intermediate frequency (equal to the target frequency ÷ post divider value); second there is a smooth transition from this frequency to the target frequency (see *Figure 9*).

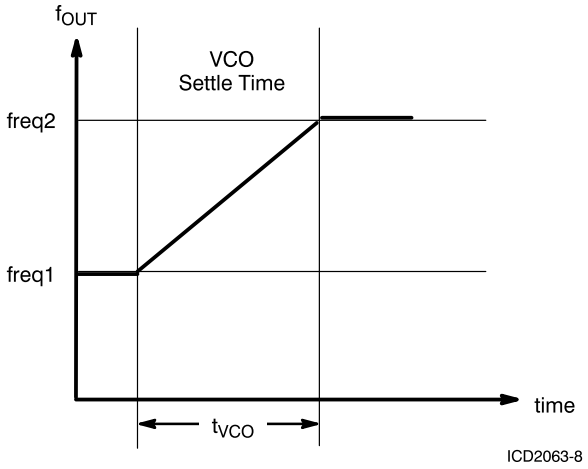


Figure 7. Frequency Transition—Smooth Mode: Normal Operation

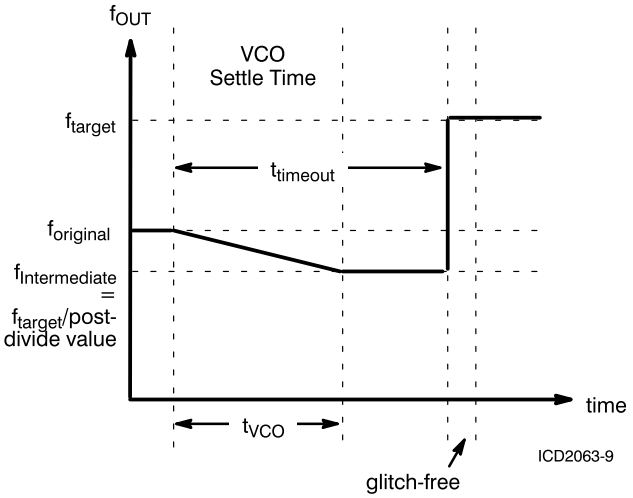


Figure 8. Frequency Transition—Post-Divide Value Decreases

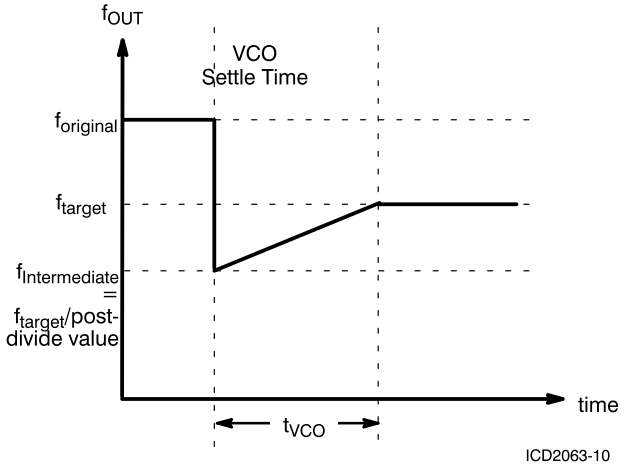


Figure 9. Frequency Transition—Post-Divide Value Increases

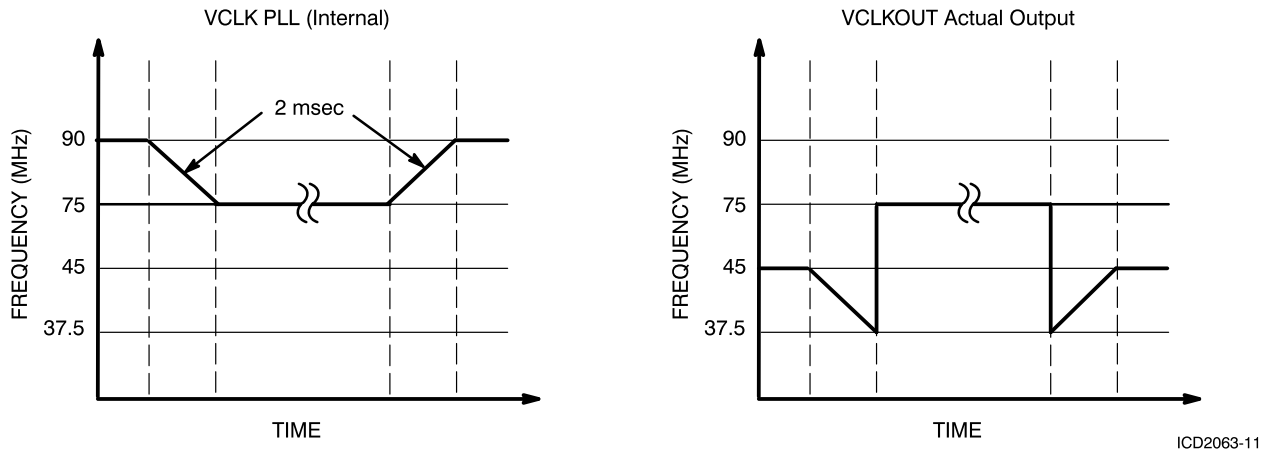


Figure 10. Smooth Frequency Transition Example

MUXREF Option

The other option for frequency transition is to multiplex the output of the VCO undergoing change to some alternate stable frequency until the VCO has settled to the new frequency value. This option preserves compatibility with the earlier ICD2061A.

In general, any changes to the VCLK VCO will result in the Reference Frequency ($f_{(REF)}$) being multiplexed to the output. However, since most video controllers now use the MCLK output as their principal clock source, and since an $f_{(REF)}$ of 14.31818 MHz is in many cases too slow for proper operation of the VGA chip, changes to the MCLK VCO will result in the VCLKOUT signal being multiplexed to the MCLK output.

The following five cases detail specifics about operation with the MUXREF option during frequency transitions.

Case 1: MCLK PLL Transition—Reprogramming of the Active Register

When a new frequency is being set for the active MCLK register, then a glitch-free multiplexing to the VCLKOUT signal is performed. For more details, see the *Active MCLK and VCLK Register Programming Timing (MUXREF Mode)* waveform in the *Switching Waveforms* section.

Case 2: VCLK PLL Transition—Reprogramming of the Active Register

When a new frequency is being set for the active VCLK register, then a glitch-free multiplexing to the reference signal $f_{(REF)}$ is performed. For more details, see the *Active MCLK and VCLK Register Programming Timing (MUXREF Mode)* waveform in the *Switching Waveforms* section.

Case 3: MCLK PLL Transition—Changing Register Selects

When a new MCLK frequency is being set by the register selects, then a glitch-free multiplexing to the VCLKOUT signal is performed. For more details, see the *Selection Timing (MUXREF Mode)* waveform in the *Switching Waveforms* section.

Case 4: VCLK PLL Transition—Changing Register Selects

When a new VCLK frequency is being set by the register selects, then a glitch-free multiplexing to the reference signal $f_{(REF)}$ is performed. For more details, see the *Selection Timing (MUXREF Mode)* waveform in the *Switching Waveforms* section.

Case 5: VCLK and MCLK PLL Transition—Changing Register Selects

If the Reset Option is configured and the select sequence is chosen which results in a coincident change in both MCLK and VCLK registers (i.e., selects go *from* being 11 or go *to* being 11), then first a new MCLK frequency is set with a glitch-free multiplexing to the current VCLKOUT signal, followed by the new VCLK frequency being set with a glitch-free multiplexing to the reference signal $f_{(REF)}$ being performed. For more details, see the *VCLK and MCLK Selection Timing* waveform in the *Switching Waveforms* section.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential . . . . . −0.5V to +7.0V
DC Input Voltage . . . . . −0.5V to V_{DD} +0.5V
Storage Temperature . . . . . −65°C to +150°C
Max soldering temperature (10 sec) . . . . . 260°C
Junction temperature . . . . . 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5% 3.3V ± 10%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD} & AV_{DD}	Supply Voltage Relative to GND[5] 390 kHz – 100 MHz 390 kHz – 120 MHz 390 kHz – 135 MHz	 VCLK specs shown (MCLK low end = 312 kHz)	 3.0 4.5 4.75		 3.6 5.5 5.5	V
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0mA	V_{DD}−0.5			V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input HIGH Voltage	Except on Crystal Pins	2.0		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	Except on Crystal Pins	−0.3		0.8	V
I_{IH}	Input HIGH Current	V_{IH} = V_{DD}−0.5			150	µA
I_{IL}	Input LOW Current	V_{IL} = +0.5V			−250	µA
I_{OZ}	Output Leakage Current	(Three-state)			10	µA
I_{DD}	Power Supply Current	5V/3.3V, Inputs @ V_{DD} or GND	15/10		65/44	mA
I_{DD-TYP}	Power Supply Current	5V/3.3V (60 MHz)		35/24	80/50	mA
I_{ADD}	Analog Power Supply Current				10	mA
I_{PD1}	Power-Down Current (Mode 1)	5V/3.3V		6/4	7.5/5.0	mA
I_{PD2}	Power-Down Current (Mode 2)	5V/3.3V		25/20	50/35	µA

Notes:
4. Input capacitance is typically 10 pF, except for the crystal pins.
5. For transition between 3.3V and 5V operation, refer to the *3.3 Volt and 5 Volt Issues* section.

Switching Characteristics Over the Operating Range

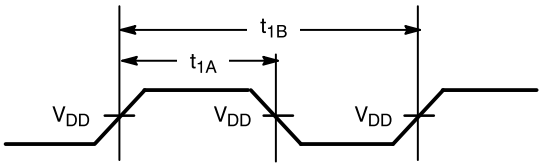
Parameter	Name	Description		Min.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference Oscillator nominal value Typical = 14.318[6]		1	60	MHz
$t_{(REF)}$	Reference Clock Period	$t_{(REF)} = 1/f_{(REF)}$		16.6	1000	ns
t_1	Input Duty Cycle	Duty cycle for the inputs defined as $t_{1B} \div t_{1A}$		25%	75%	
t_2	Output Clock Periods	VCLK Output values	V_{DD}=5V	7.41 (135 MHz)	2564 (390 kHz)	ns
			V_{DD}=3.3V	10.0 (100 MHz)		
		MCLK Output values	V_{DD}=5V	10.0 (100 MHz)	3205 (312 kHz)	
			V_{DD}=3.3V	12.5 (80 MHz)		
t_3	Output Duty Cycle	Duty cycle for the outputs defined as $t_{1A} \div t_{1B}$[7]		40	60	%
t_4	Rise Times	Rise time for the outputs into a 25-pF load			4	ns
t_5	Fall Times	Fall time for the outputs into a 25-pF load			4	ns
t_{freq1}	freq1 Output	Old frequency output				
t_{freq2}	freq2 Output	New frequency output				
t_A	$f_{(REF)}$ Mux Time	Time clock output remains LOW while output muxes to reference frequency		$t_{(REF)}/2$	$3(t_{(REF)}/2)$	ns
$t_{timeout}$	Timeout Interval	Internal interval for special programming and for VCO changes to settle[8]		2	10	msec
t_B	t_{freq2} Mux Time	Time clock output remains LOW while output muxes to new frequency value		$t_{freq2}/2$	$3/(t_{freq2}/2)$	ns
t_6	Three-state Time	Time for the outputs to go into three-state mode after OE signal assertion		0	12	ns
t_7	CLK Valid Time	Time for the outputs to recover from three-state mode after OE signal goes HIGH		0	12	ns
t_8	Power-Down Delay	Time for Power-Down Mode of operation to take effect			12	ns
t_9	Power-Up Delay	Time for recovery from Power-Down Mode of operation			12	ns
t_{10}	MCLKOUT HIGH	Time for MCLKOUT to go LOW after $\overline{\text{PWRDWN}}$ is asserted HIGH		0	$1/t_{PWR\text{-}DWN}$	ns
t_{11}	MCLKOUT delay	Delay of MCLKOUT prior to f_{MCLK} signal at output		$t_{MCLK}/2$	$3/(t_{MCLK}/2)$	ns
t_{serclk}		Clock period of serial clock		2 x $t_{(REF)}$	2	msec
t_{HI}		Minimum HIGH time		$t_{(REF)}$		ns
t_{LO}		Minimum LOW time		$t_{(REF)}$		ns
t_{SU}		Set-Up time		20		ns
t_{HD}		Hold time		10		ns
t_{ldcmd}		Load command		0	$t_{(REF)}+30$	ns

Notes:

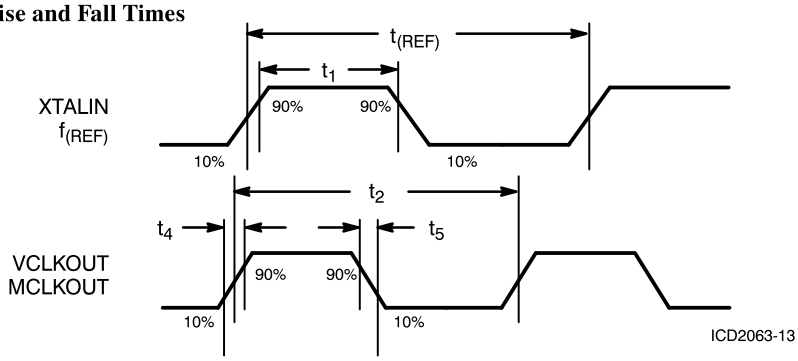
6. For references other than 14.31818 MHz, the pre-loaded ROM frequencies will not be accurate.
7. Duty cycle is measured at CMOS threshold levels ($V_{DD} \div 2$). At 5V, V_{TH}=2.5V.
8. If the interval is too short, see the Timeout Interval paragraph of the *Control Register Definition* section..

Switching Waveforms

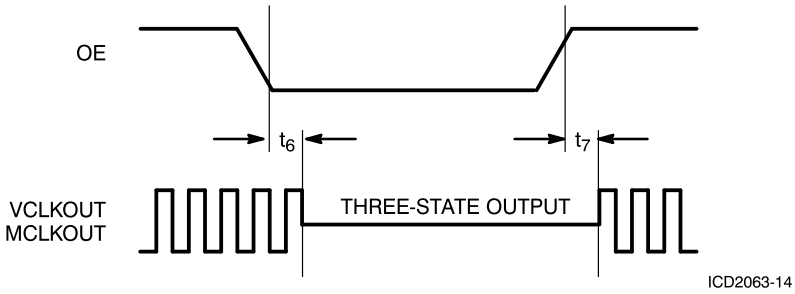
Duty Cycle Timing



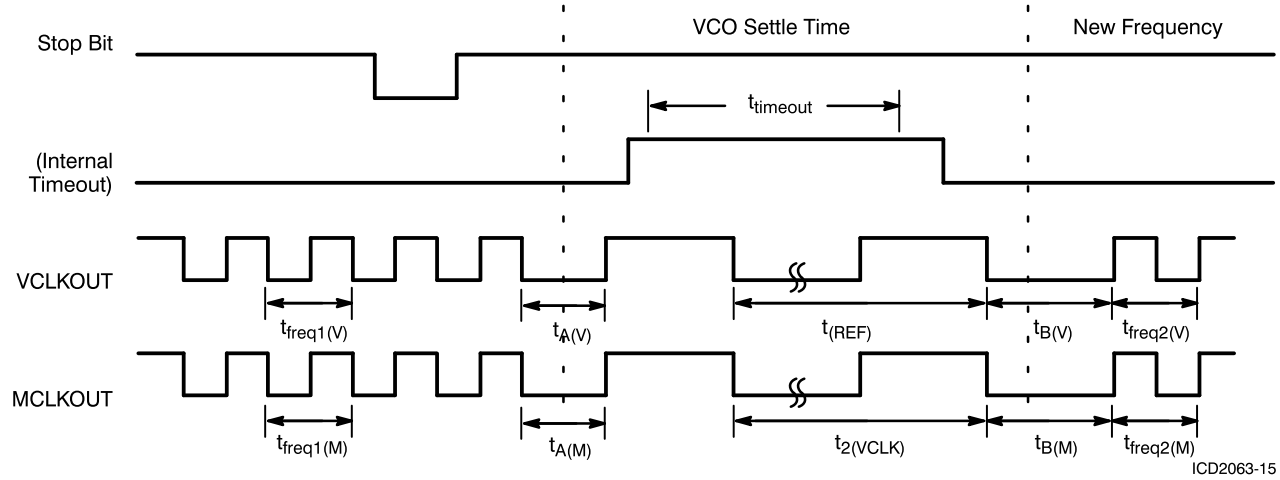
Rise and Fall Times



Three-State Timing

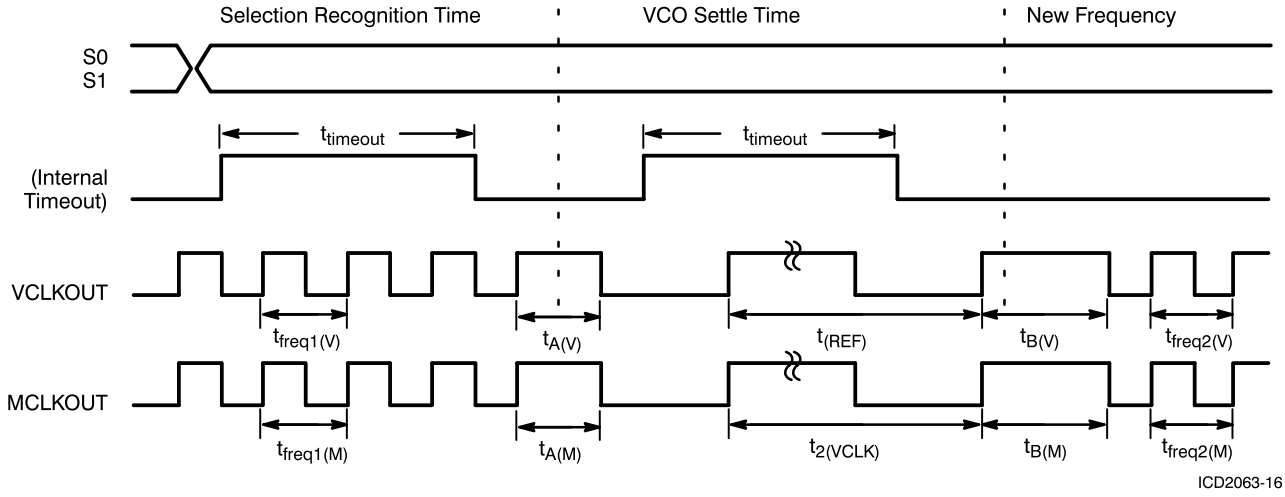


Active MCLK and VCLK Register Programming Timing (MUXREF Mode)

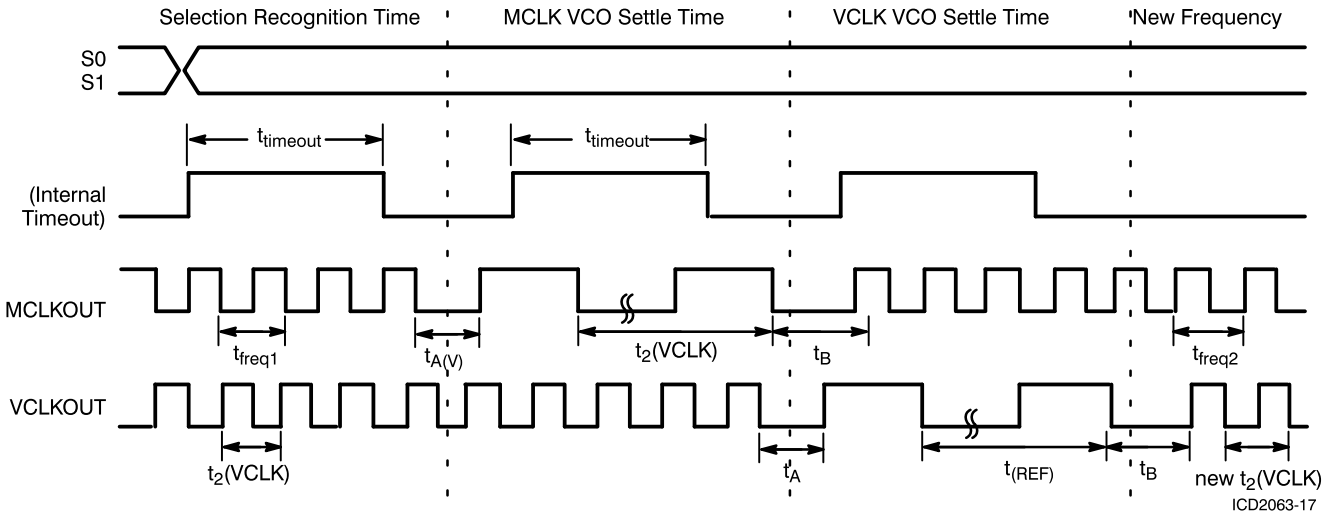


Switching Waveforms (continued)

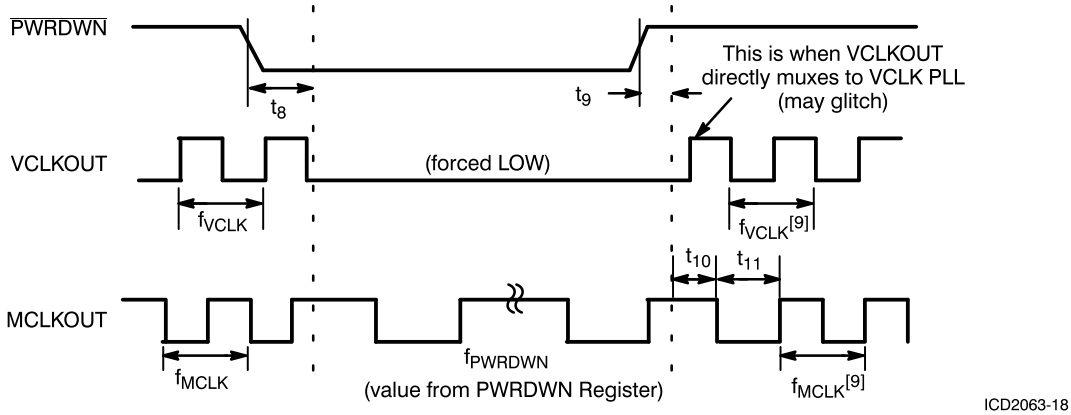
Selection Timing (MUXREF Mode)



VCLK and MCLK Selection Timing (Concurrent Change)



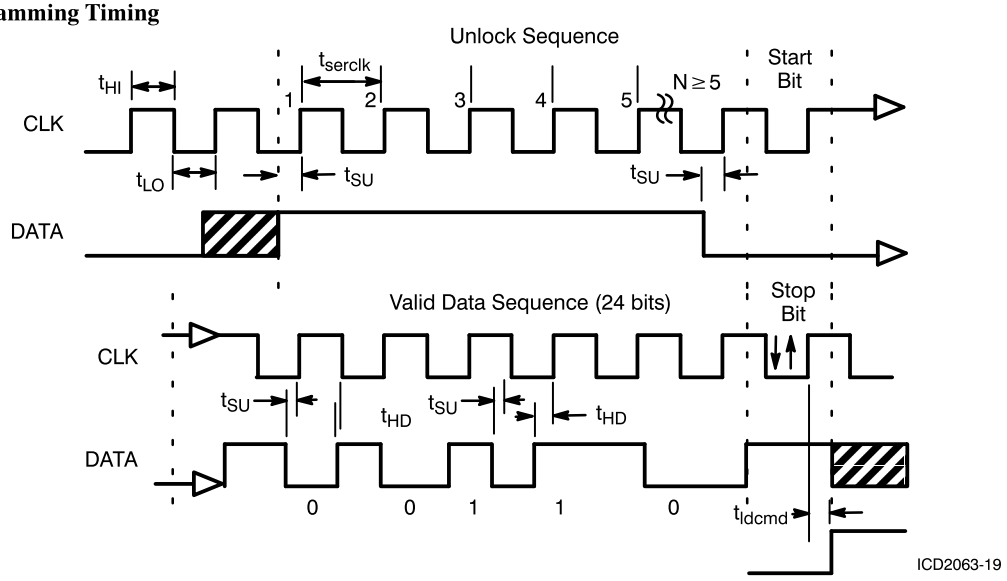
Soft Power-Down Timing (Mode 2)



Note:
9. It takes 5 msec after Soft Power-Down to guarantee lock of VCLKOUT and MCLKOUT PLLs.

Switching Waveforms (continued)

Serial Programming Timing



Configuration Options

Option	Choices	−1	−2	−3
Pin 10 Function	$\overline{\text{ERROUT}}$ or XBUF	XBUF	$\overline{\text{ERROUT}}$	$\overline{\text{ERROUT}}$
Pin 14 Function	$\overline{\text{RESET}}$ or SELM	SELM	$\overline{\text{RESET}}$	SELM
Frequency Transition	Smooth or MUXREF	Smooth	MUXREF	Smooth

Ordering Information[10]

Ordering Code	Package Name	Package Type	Operating Range	Chip Options
ICD2063	S1	16-Pin SOIC	Commercial[11]	−1, −2, −3

Notes:
10. Please call your local Cypress representative.
11. 0°C to +70°C

Example: order ICD2063SC−1 for the ICD2063, 16-pin plastic SOIC, commercial temperature range device with the initial frequencies shown in *Table 3.*

Document #: 38−00405

Package Diagram

16-Lead Molded SOIC S1