ICD2093

"Super Buffer" Clock Generator

Features

- **Selectable CPU clock provides eight 2X or 1X outputs which handle all 486 processor clocking requirements**
- **Less than 250 ps total skew between Hi-Drive (48 mA) , Hi-Load (50 pF) CPU clock outputs**
- **Four fixed outputs: 14.31818 MHz (2), 16 MHz, and 24 or 32 MHz handle all other system clocking requirements**
- **CPU clock frequency range: 10 MHz to 100 MHz with 50% duty cycle**
- **Optional power-down mode**
- **Three-state oscillator control disables outputs for test purposes**
- **Phase-locked loop oscillator input derived from single 14.31818 MHz crystal**
- **Sophisticated internal loop-filter requires no external components**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 24-pin SOIC package configuration**

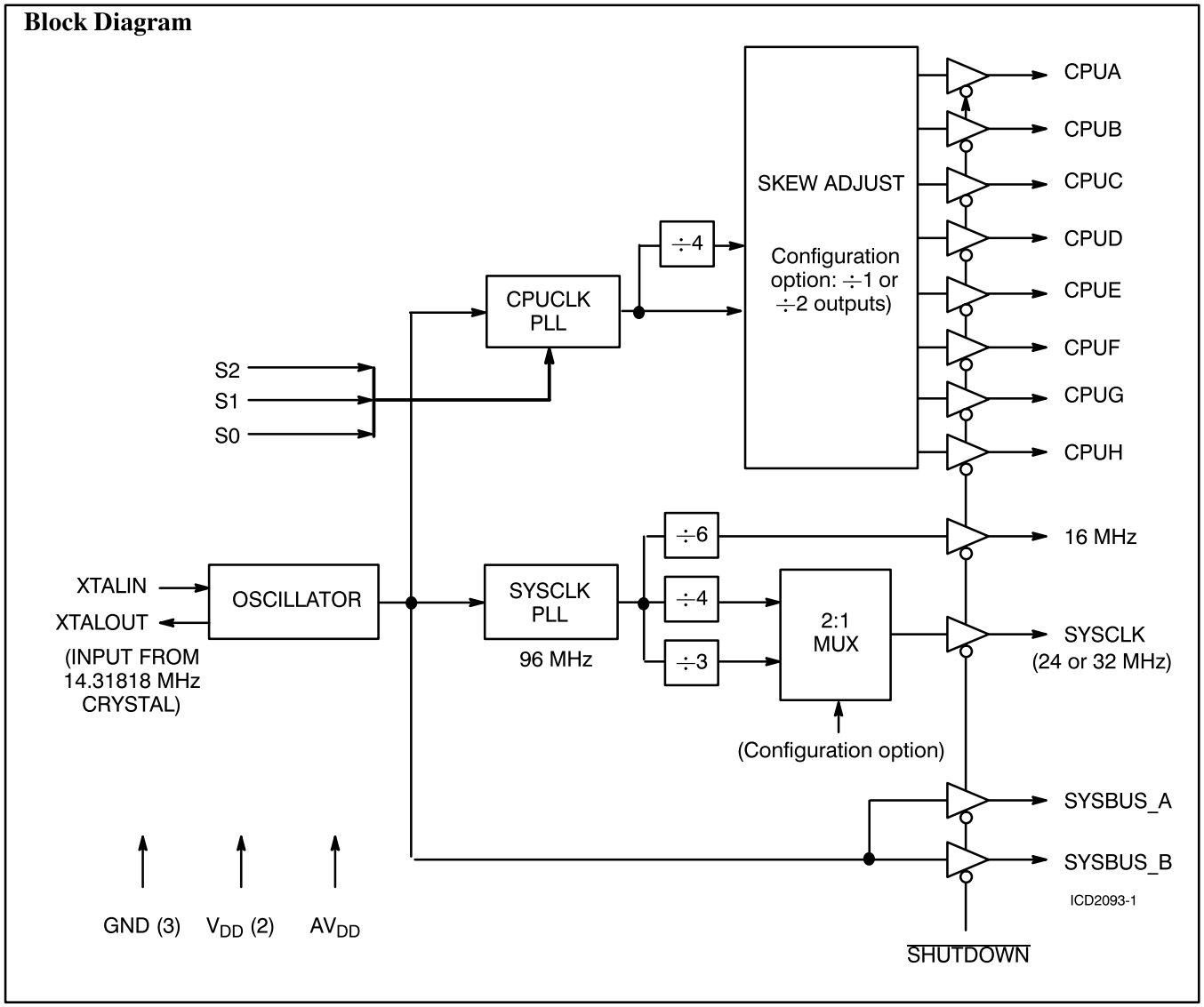
Functional Description

Today's high-end personal computers require a CPU system clock which exhibits a large drive capability (high fanout) without degradation in rise and fall times. The classical solution has been to distribute and buffer this clock. The ICD2093 alleviates this problem by providing eight 1X or 2X Clock outputs with extremely low skew between outputs.

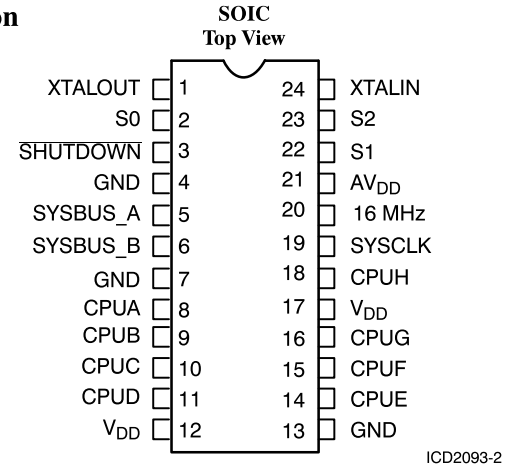
The ICD2093 also supplies other clocks required in a high-performance system: the system I/O and bus clocks.

The ICD2093 consists of one crystal controlled oscillator, two phase-locked loops, and twelve different outputs in a single package.

Block Diagram



Pin Configuration



Pin Summary

Name	Number	Description
XTALOUT[1]	1	Oscillator output to a 14.318 MHz parallel-resonant crystal
S0	2	CPU Clock ROM Select Line—Bit 0 (LSB)
$\overline{\text{SHUTDOWN}}$ (OE)	3	When pulled LOW, shuts down oscillator, PLL, and all dynamic logic. Can be made three-state Output Enable via configuration option. Internal pull-up allows for no-connect if shutdown operation is not needed.
GND	4	Ground
SYSBUS_A	5	14.31818 MHz Output
SYSBUS_B	6	14.31818 MHz Output
GND	7	Ground
CPUA	8	CPU Clock Output A (1X or 2X)[2]
CPUB	9	CPU Clock Output B (1X or 2X)[2]
CPUC	10	CPU Clock Output C (1X or 2X)[2]
CPUD	11	CPU Clock Output D (1X or 2X)[2]
V_{DD}	12	+5V to I/O Ring
GND	13	Ground
CPUE	14	CPU Clock Output E (1X or 2X)[2]
CPUF	15	CPU Clock Output F (1X or 2X)[2]
CPUG	16	CPU Clock Output G (1X or 2X)[2]
V_{DD}	17	+5V to I/O Ring
CPUH	18	CPU Clock Output H (1X or 2X)[2]
SYSCLK	19	24 MHz or 32 MHz Output (factory configurable)
16 MHz	20	16 MHz Output
AV_{DD}	21	+5V to Analog Core
S1	22	CPU Clock ROM Select Line—Bit 1
S2	23	CPU Clock ROM Select Line—Bit 2 (MSB)
XTALIN[1]	24	Oscillator input from a 14.31818 MHz crystal

Notes:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.
2. All the CPU outputs can be 1X, 2X, or any mix of the two (the outputs of each type are contiguous).

Clock Operation

CPUCLK PLL

The output frequency of the CPU clock PLL (CPUCLK) is selected by the Clock Selection Inputs S0−S2. This lets the ICD2093 support different microprocessor speed configurations.

The selection lines can be changed at any time to select a new frequency. When this occurs, the internal phase-locked loop immediately seeks the new frequency in the 33.333-MHz to 80-MHz range.

Table 1. CPUCLK ROM Selection Outputs

S2	S1	S0	Desired Freq. (MHz)	Actual CPUCLK (MHz)	Actual CPU/2 (MHz)	VCO Freq. (MHz)	Error (PPM)
0	0	0	20.000	20.003	10.002	80.013	167
0	0	1	33.333	33.322	16.661	66.645	331
0	1	0	60.000	60.000	30.000	120.000	0
0	1	1	40.000	40.006	20.003	80.013	167
1	0	0	50.000	50.114	25.057	100.227	2267
1	0	1	66.667	66.818	33.409	133.636	2270
1	1	0	80.000	80.013	40.006	160.026	167
1	1	1	100.000	100.227	50.114	100.227	2267

Fixed Frequency Oscillator Operation

Table 2 lists the available fixed frequency outputs.

Table 2. CPUCLK ROM Selection Outputs

Desired Frequency (MHz)	Actual Frequency (MHz)		Error (PPM)	
	Option −1	Option −2	Option −1	Option −2
24.000	23.993	23.967	1359	307
32.000	31.990	31.957	1359	307

Design Considerations

Skew Issues

The ICD2093 offers eight CPUCLK ÷1 or ÷2 outputs, CPUA−CPUH. These outputs have been optimized to minimize skew between any two CPUA−CPUH outputs.

The standard drive on all CPU outputs is 48 mA, with a 3-ns rise and fall time when driving 50 pF.

To minimize skew, output loads should be balanced and the printed circuit board trace lengths should be equal. The high-performance output driver of the ICD2093 requires the engineer to observe proper transmission line techniques, including termination, when designing for the ICD2093. (See the *Termination* section for suggestions on proper termination.)

Table 3 estimates the incremental skew (in addition to worst-case specification) caused by unbalanced loading. The table includes data for driving both TTL loads and CMOS threshold loads. There are two normalized measurements given: all loads normalized to 0 pF, and all loads at 30 pF (the latter being a more realistic operating assumption).

Table 3. CPUCLK ROM Selection Outputs

Load	Threshold Volts	Rising Edge (ns)		Falling Edge (ns)	
		Normalized at 0 pF	Normalized at 30 pF	Normalized at 0 pF	Normalized at 30 pF
50 pF	2.5	1.10	0.38	1.03	0.33
	1.4	0.72	0.22	1.31	0.44
40 pF	2.5	0.92	0.20	0.88	0.18
	1.4	0.62	0.12	1.09	0.22
30 pF	2.5	0.72	0.00	0.70	0.00
	1.4	0.50	0.00	0.87	0.00
20 pF	2.5	0.52	−0.20	0.50	−0.20
	1.4	0.35	−0.15	0.62	−0.25
10 pF	2.5	0.30	−0.42	0.28	−0.42
	1.4	0.20	−0.30	0.32	−0.55
0 pF	2.5	0.00	−0.72	0.00	−0.70
	1.4	0.00	−0.50	0.00	−0.87

Termination

The ICD2093 provides fast rise and fall times on its outputs to drive large loads, which require the PCB designer to observe proper transmission line techniques. There are three principal techniques for proper termination. The optimum choice depends on individual requirements.

Series Termination

The main drawback of this technique is that C_L adversely affects rise and fall times (see *Figure 1*).

Parallel Termination

The main drawback of this technique is that it consumes power.

$V_T = V_{DD} \div 2$ for minimum power. (Note that V_T should not equal receiver threshold. TTL systems often set V_T at 3V using Thévenin equivalent circuit.) See example divider in *Figure 2*.

AC Termination

The main drawback of this technique is that it is not as good at high frequencies (see *Figure 3*).

Power Calculation

Actual current drain is a function of frequency and circuit loading. The operating current of a given output is given by the

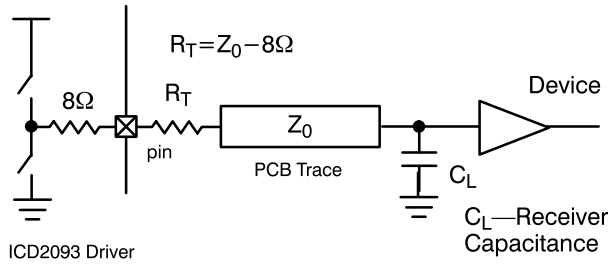


Figure 1. Series Termination

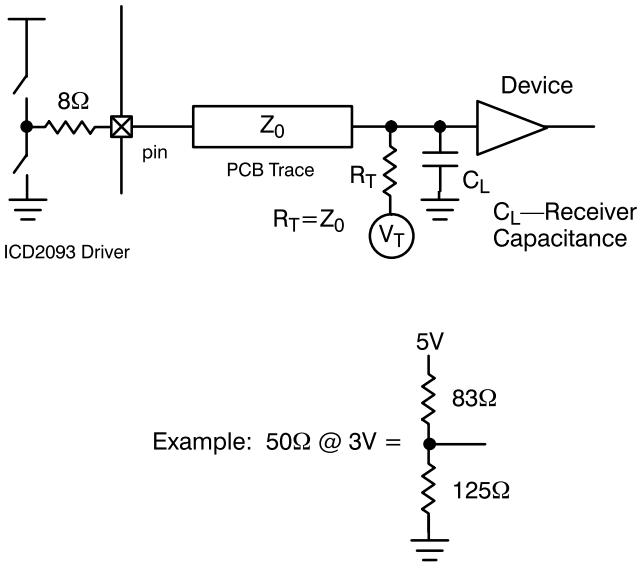


Figure 2. Parallel Termination

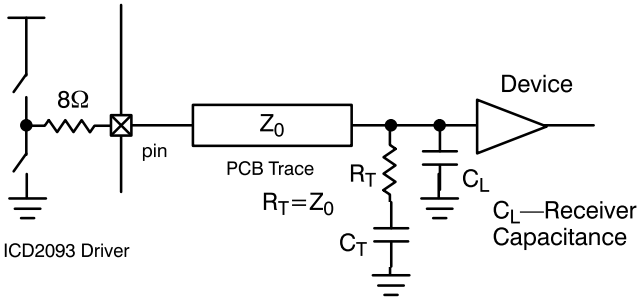


Figure 3. AC Termination

equation I = C • V • f, where I=current, C=load capacitance, V=output voltage in Volts (usually 5V for rail-to-rail CMOS pads) and f=output frequency in MHz.

To calculate total operating current, sum the following:

$I_{SYSBUS\_A} \Rightarrow C_{14} \bullet V \bullet 14.318$
$I_{SYSBUS\_B} \Rightarrow C_{24} \bullet V \bullet 14.318$
$I_{CPUA} \Rightarrow C_{CLKA} \bullet V \bullet f_{CLKA}$
$I_{CPUB} \Rightarrow C_{CLKB} \bullet V \bullet f_{CLKB}$
$I_{CPUC} \Rightarrow C_{CLKC} \bullet V \bullet f_{CLKC}$
$I_{CPUD} \Rightarrow C_{CLKD} \bullet V \bullet f_{CLKD}$
$I_{CPUE} \Rightarrow C_{CLKE} \bullet V \bullet f_{CLKE}$
$I_{CPUF} \Rightarrow C_{CLKF} \bullet V \bullet f_{CLK}F$
$I_{CPUG} \Rightarrow C_{CLKG} \bullet V \bullet f_{CLKG}$
$I_{CPUH} \Rightarrow C_{CLKH} \bullet V \bullet f_{CLKH}$
$I_{(Internal)} \Rightarrow .06$ A (60 mA)

This yields an approximation of the actual operating current. For unconnected output pins, one can assume 5−10 pF loading, depending on the package type.

Some typical values are displayed in *Table NO TAG*.

Table 4. Operating Current Typical Values

Frequency	Capacitive Load	Current (in mA)
66.6 MHz	30 pF	115

General Considerations

Power-Down Operation

In the power-down state, the oscillator, PLL, and all dynamic logic is shut down.

Note that, during shutdown, the internal PLLs are turned off. Upon restarting, there will be a 5-msec interval during which the VCOs stabilize. See *Power-Down Timing* in the *Switching Waveforms* section for further timing information.

Three-State Output Operation

If the OE configuration is chosen, then the $\overline{\text{SHUTDOWN}}$ pin becomes an OE pin, which, when pulled LOW, will three-state all the clock output lines. This supports Wired-OR connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The OE signal contains an internal pull-up; it can be left unconnected if three-state operation is not required. The output pads contain weak pull-down resistors.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential . . . . . −0.5V to +7.0V
DC Input Voltage . . . . . −0.5V to V_{DD} +0.5V
Storage Temperature . . . . . −65°C to +150°C
Max soldering temperature (10 sec) . . . . . 260°C
Junction temperature . . . . . 140°C
Package power dissipation . . . . . 1000 mW

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −48 mA[3]	V_{DD}−0.5		V
V_{OL}	Output LOW Voltage	I_{OL} = 48 mA[3]		0.5	V
V_{IH}	Input HIGH Voltage	Except crystal inputs	2.0		V
V_{IL}	Input LOW Voltage	Except crystal inputs		0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}−0.5V		150	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V		−250	µA
I_{OZ}	Output Leakage Current	(Three-state)	−10	150	µA
I_{DDA}	Power Supply to Core	1 CPU @ 66 MHz 7 CPU @ 33 MHz Inputs @ V_{DD} or GND		18	mA
I_{DD}	Power Supply Current			130	mA
C_L	Total Cap. Load/CPU Output			50[3, 4]	pF

Notes:
3. Option −2 has half the output drive capability: I_{OH}=−24 mA, I_{OL}=24 mA, C_L=25 pF.
4. Maximum load on all CPU outputs can exceed the maximum specifications.

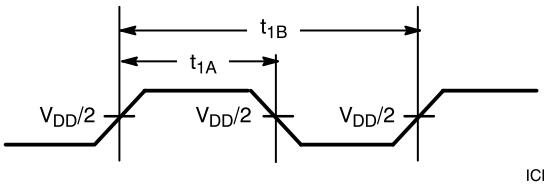
Switching Characteristics[5]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference input normal value		14.318		MHz
$t_{(REF)}$	Reference Clock Period	$1 \div f_{(REF)}$		69.84		ns
t_1	Input Duty Cycle	Duty cycle for the input oscillator defined as $t_1 = t_{1A} \div t_{1B}$	25%	50%	75%	
t_2	Output Period		10 100 MHz		100 10 MHz	ns
t_3	Output Duty Cycle	Duty cycle for the outputs, measured @ CMOS V_{TH} of $V_{DD} \div 2$ (special screening required for 100 MHz) $t_3 = t_{1A} \div t_{1B}$	40%		60%	
t_4	Rise Times	Rise time of clock outputs (50-pF load @ 10 MHz)			3.5	ns
t_5	Fall Times	Fall time of clock outputs (50-pF load @ 10 MHz)			4	ns
t_6	Skew	Leading edge skew between 1X and 2X outputs and C_L=50 pF			500	ps
t_8	Skew	Leading edge skew between 1X and 1X or 2X and 2X outputs and C_L=50 pF			250	ps
t_{VCO}	VCO Settle Time	Time for VCO to transition smoothly and monotonically from the original to the new frequency			3	msec
t_{10}	Three-state Time	Time for the outputs to go into three-state mode after OE signal goes LOW			20	ns
t_{11}	Clock Enable Time	Time for the outputs to recover from three-state mode after OE signal goes HIGH			20	ns
t_{12}	SYSBUS Skew	Leading edge skew between SYSBUS outputs			500	ps
t_{13}	SYSBUS Skew	Trailing edge skew between SYSBUS outputs			500	ps
t_{14}	Power-Down	Time to invoke power-down option			20	ns
t_{15}	Power-Up	Time to revoke power-down option			20	ns

Note:
5. Input capacitance is typically 10 pF, except for the crystal pads.

Switching Waveforms

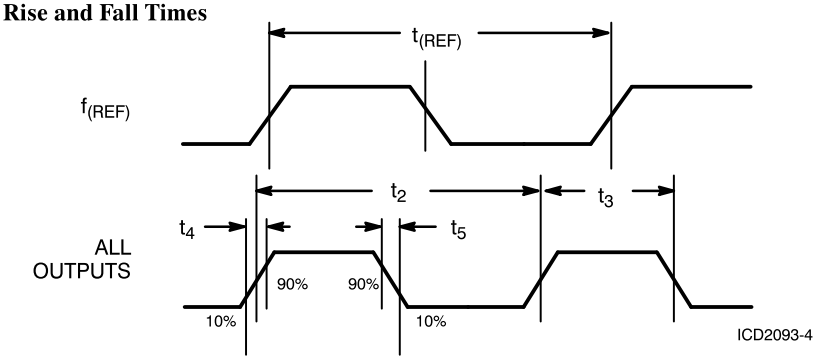
Duty Cycle Timing



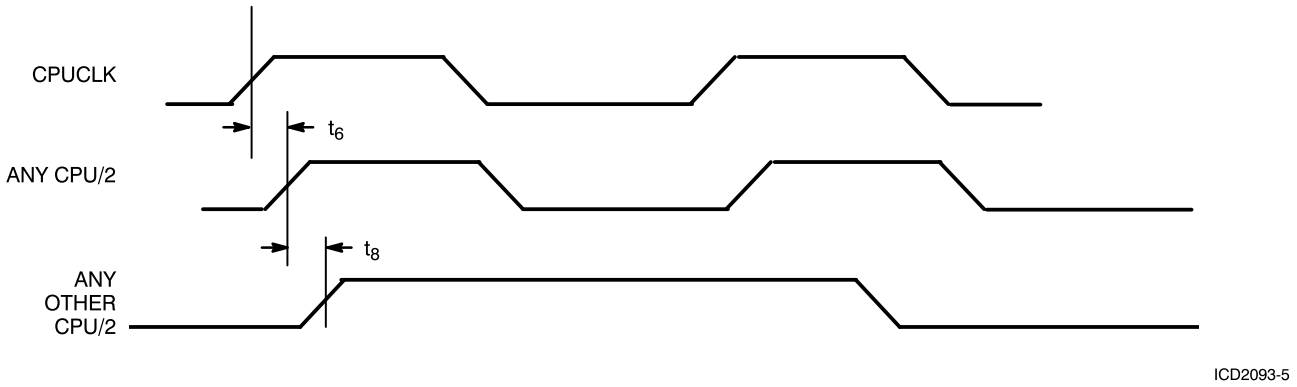
ICD2093-3

Switching Waveforms (continued)

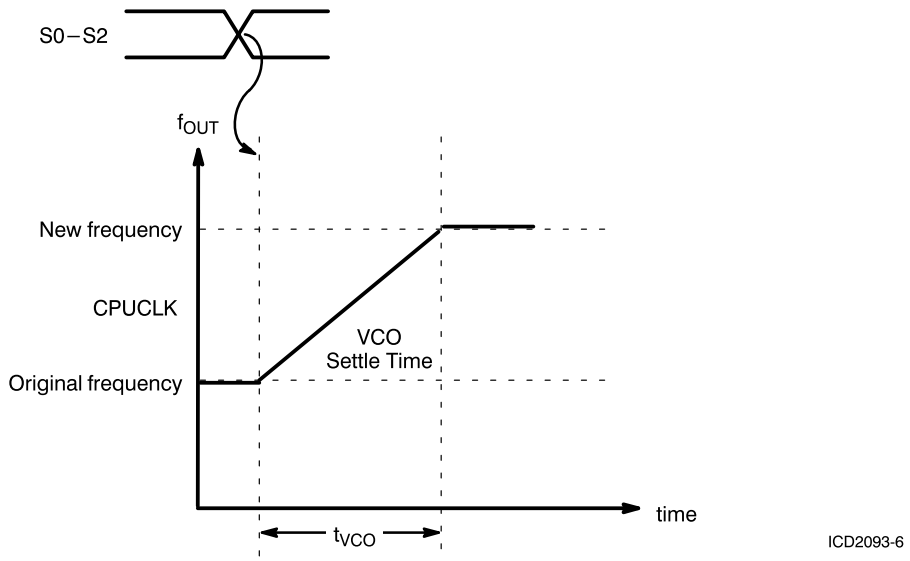
Rise and Fall Times



CPUCLK Skew



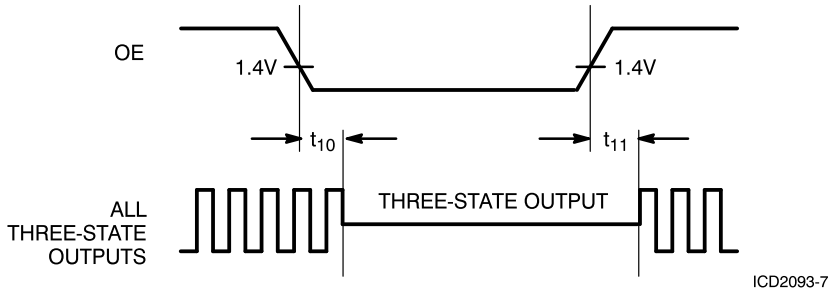
Selection Timing



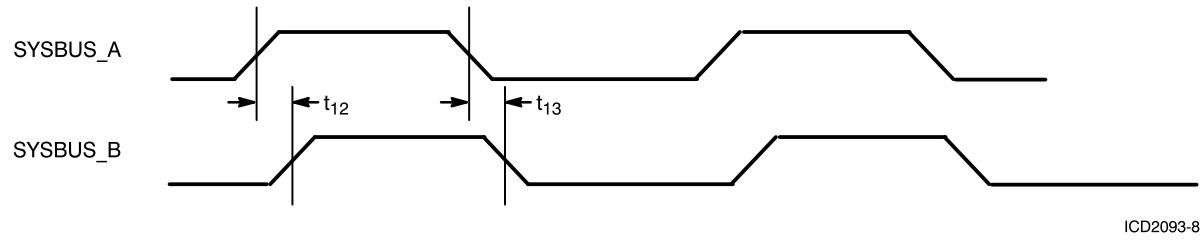
(Valid for all transitions except CPUCLK = 10 MHz ⇒ 100 MHz)

Switching Waveforms (continued)

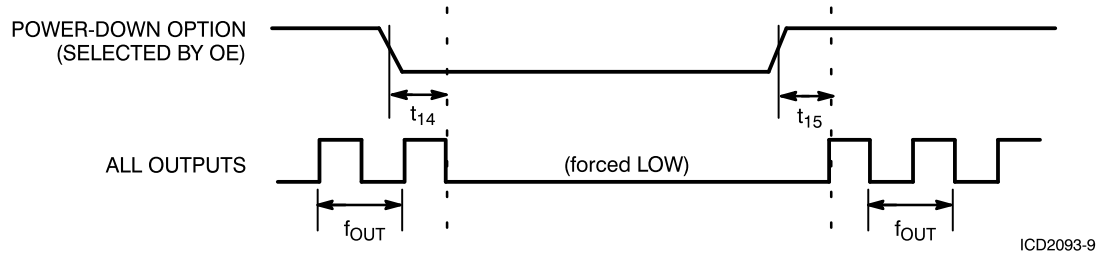
Three-State Timing



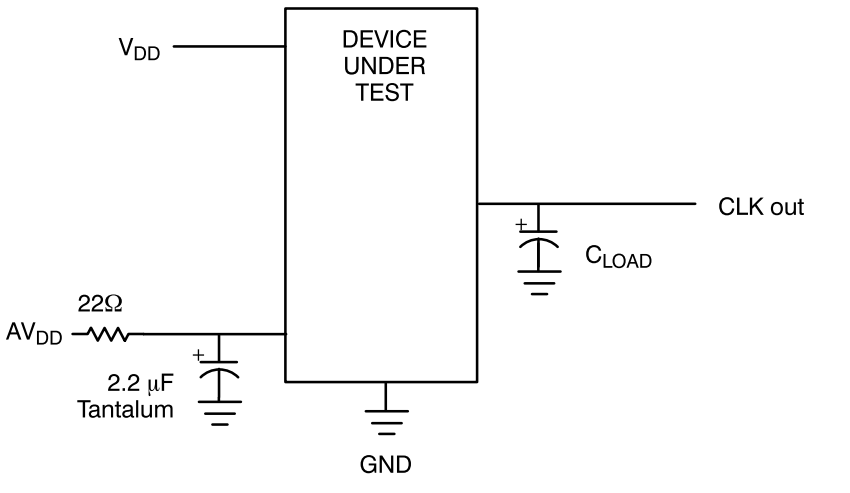
SYSBUS Skew



Power-Down Timing

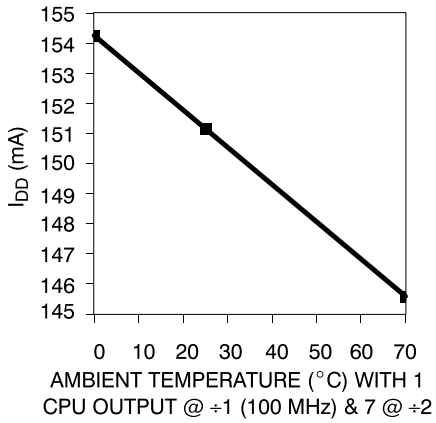


Test Circuit

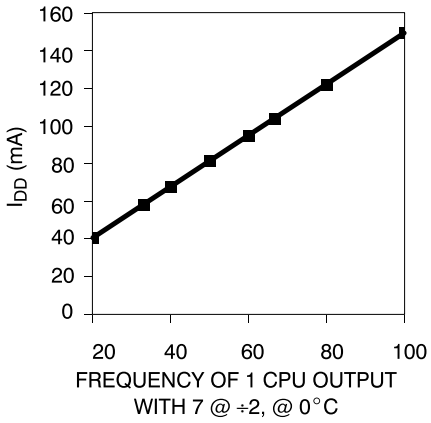


Typical AC and DC Characteristics

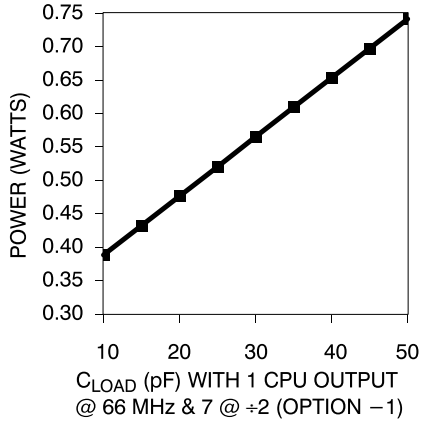
I TOTAL



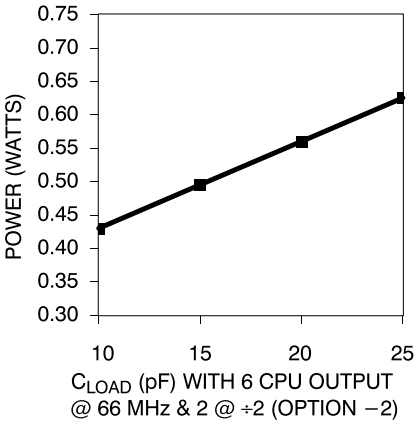
I TOTAL



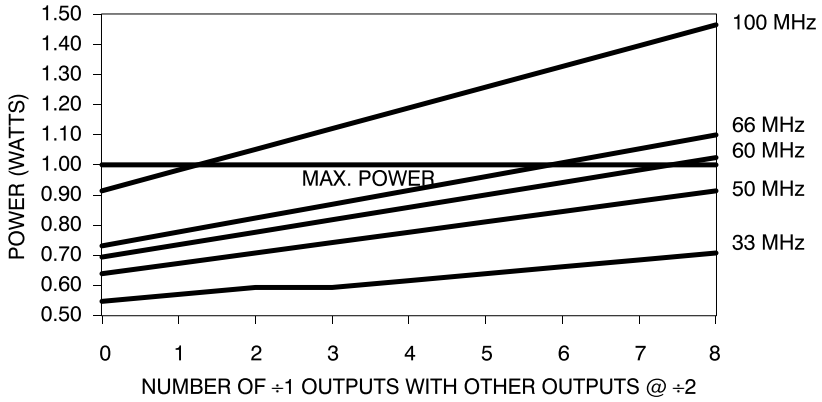
CALCULATED POWER DISSIPATION



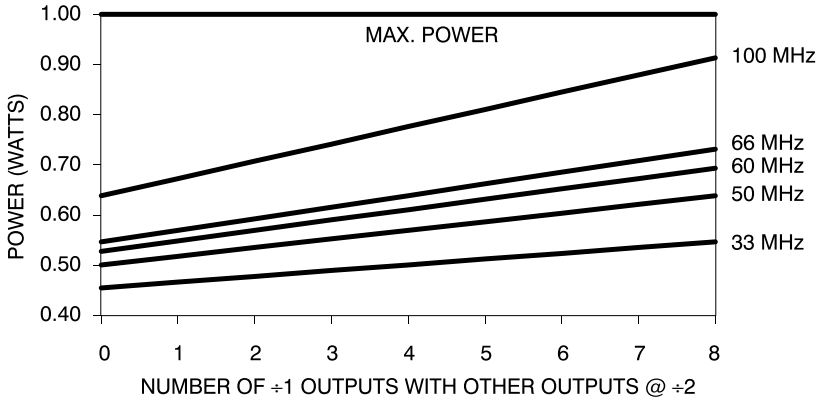
CALCULATED POWER DISSIPATION



WORST-CASE POWER, V_{DD}=5.25V, C_{LOAD}=50 pF (SIMILAR TO −1 OPTION)



WORST-CASE POWER, V_{DD}=5.25V, C_{LOAD}=25 pF (SIMILAR TO −2 OPTION)



Configuration Options

Signal/Pin	Option −1	Option −2
CPUA	÷2	÷2
CPUB	÷2	÷2
CPUC	÷2	÷1
CPUD	÷2	÷1
CPUE	÷2	÷1
CPUF	÷2	÷1
CPUG	÷2	÷1
CPUH	÷1	÷1
Pin 3	OE	$\overline{\text{SHUTDOWN}}$
SYSCLK	24 MHz	24 MHz

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Clock Output Options
ICD2093	S13	24-Pin SOIC	C=0°C to +70°C @ V_{DD}=5V	Standard Configuration −1

Example: Order ICD2093SC−1 for the ICD2093, 24-pin plastic SOIC, commercial temperature range device which uses the standard configuration code −1 (SYSCLK=24 MHz, Power-Down not enabled, one ÷1 CPU clock and seven ÷2 CPU clocks).

Custom configurations are also available. To order a custom configuration, please contact your Cypress representative.

Document #: 38−00401

Package Diagram

24-Lead (300-Mil) Molded SOIC S13