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Layout and Termination Techniques For Cypress Clock Generators

Cypress Semiconductor makes a variety of PLL-based clock generators. This application note provides a set of recommendations to optimize usage of Cypress clock devices in a system. The application note begins with recommended termination techniques for clock generators. Subsequently, power supply filtering and bypassing is discussed. Finally, the application note provides some recommendations on board layout.

Summary of Transmission Line Theory

Typically, Cypress clock generators have low output impedances. When these devices drive loads with large input impedances, there is an impedance mismatch between the low-impedance source and high-impedance load. Under certain conditions, this causes voltage reflections to occur from the load, thus resulting in overshoot and undershoot of the signal. Ultimately, this results in less-than-optimum system operation.

When do Voltage Reflections Occur?

Simply put, voltage reflections can occur when the PCB trace starts behaving as a transmission line and there is an impedance mismatch between the trace and the load. Expressing the first condition mathematically, reflections will occur when:

$$L > \frac{t_r}{2t_{pd}} \qquad \text{Eq. 1}$$

where L is the length of the trace, t_r is the rise time of the signal and t_{pd} is the propagation delay of the signal through the trace.

Under these conditions, a trace starts behaving as a transmission line. Once this occurs, signals will be reflected from the load if the energy of the signal is not completely dissipated along the trace. Such reflections result in signal overshoot and undershoot. *Our objective is to reduce this overshoot and undershoot to within acceptable limits, such that system noise margins are not affected, and spurious clocking does not occur.*

Table 1 shows the various trace lengths at which reflections begin to occur. Values in *Table 1* assume a 50Ω intrinsic line characteristic impedance, a multilayer PCB using stripline construction on G-10 glass epoxy material with a dielectric constant of 5. These conditions result in an unloaded line propagation delay of 2.27 ns/ft. The rise time is specified between 10% and 90% of the signal swing.

Note that if the capacitive loading on the trace is higher (for example, a trace drives multiple loads), or if the signal rise time is faster, reflections will start occurring on shorter traces.

Table 1. Trace Length for Voltage Reflections

t_r (ns)	C_D (pF)	L (inches)
2	10	4.73
2	20	4.32
2	40	3.74
2	80	3.05
1	10	2.16
1	20	1.87
1	40	1.53
1	80	1.18
0.5	10	0.93
0.5	20	0.76
0.5	40	0.59
0.5	80	0.44

How to Reduce Voltage Reflections ?

Properly terminating the trace will reduce voltage reflections. There are two general strategies for transmission line termination:

- Match the load impedance to the line impedance
- Match the source impedance to the line impedance

From a systems design perspective, the first strategy is preferred, since it eliminates any reflections travelling back to the source, thus resulting in less noise, electromagnetic interference (EMI), and radio frequency interference (RFI). However, from a practical standpoint, either of the two techniques can be used, depending on the system under design.

Common Types of Transmission Lines

Microstrip lines and strip lines are two types of transmission lines used in multilayer boards. They are described below. For a complete analysis on other kinds of transmission lines, please refer to the application note, "System Design Considerations" available from your Cypress representative.

Microstrip Lines

A microstrip line (*Figure 1*) is a strip conductor (signal line) on a PCB separated from a ground plane by a dielectric. If the line's thickness, width, and distance from the ground plane are controlled, the line's characteristic impedance can be predicted with a tolerance of ±5 percent.

The formula given in *Figure 1* has proven to be very accurate for width-to-height ratios between 0.1:1 and 3.0:1 and for dielectric constants between 1 and 15.

The inductance per foot for microstrip lines is

$$L = (Z_O)^2 C_O \quad \text{Eq. 2}$$

where Z_O is the characteristic impedance and C_O is capacitance per foot.

The propagation delay of a microstrip line is

$$t_{pd} = 1.017\sqrt{0.45e_r + 0.67} \ (ns/ft) \quad \text{Eq. 3}$$

Note that the propagation delay depends only upon the dielectric constant and is not a function of the line width or spacing. For G-10 fiberglass epoxy PCBs (dielectric constant of 5), the propagation delay is 1.74 ns per foot.

Strip Lines

A strip line consists of a copper strip centered in a dielectric between two conducting planes (*Figure 2*). If the line's thickness, width, dielectric constant, and distance between ground planes are all controlled, the tolerance of the characteristic impedance is within ±5 percent. The equation given in *Figure 2* is accurate for $W/(b - t) < 0.35$ and $t/b < 0.25$.

The inductance per foot is given by the formula

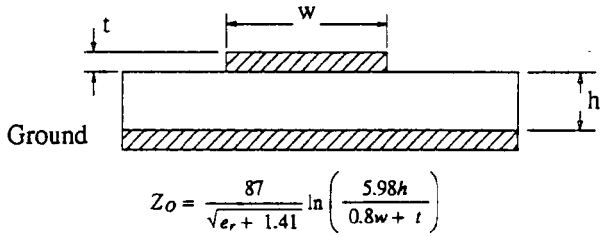


Figure 1. Microstrip Line

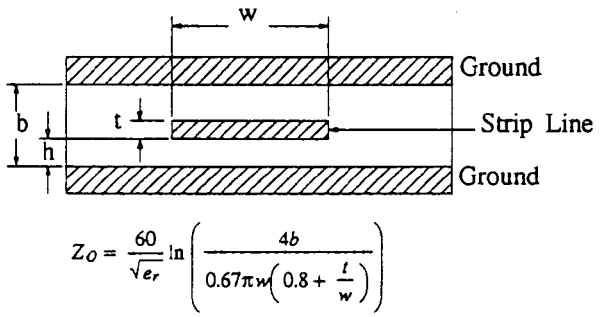


Figure 2. Strip Line Construction

$$L = (Z_O)^2 C_O \quad \text{Eq. 4}$$

The propagation delay of the line is given by the formula

$$t_{pd} = 1.017\sqrt{e_r} \ (ns/ft) \quad \text{Eq. 5}$$

For G-10 fiberglass epoxy boards, the propagation delay is 2.27 ns per foot. The propagation delay is not a function of line width or spacing.

Unloaded and Loaded Line Impedances

Adding loads to the transmission line increases the propagation delay of the signal travelling on it. The following formula shows the relationship between the unloaded and load characteristic impedances of a transmission line.

$$Z_L = \frac{Z_O}{\sqrt{1 + \frac{C_L}{lC_O}}} \quad \text{Eq. 6}$$

where Z_L is the impedance of a capacitively loaded transmission line, Z_O is the characteristic impedance of an unloaded transmission line, C_L is the load capacitance placed at the end of the transmission line, l is the length of the transmission line, and C_O is the capacitance per unit length of the transmission line.

Additionally, the characteristic (intrinsic) capacitance of a transmission line per unit length is expressed as:

$$C_O = \frac{t_{pd}}{Z_O} \quad \text{Eq. 7}$$

where *tpd* is the propagation delay through a lossless transmission line. *Table 2* shows the values of intrinsic capacitances for strip lines and microstrip lines on PCBs using G-10 Fiberglass epoxy, with a dielectric constant of 5.

Table 2. Intrinsic Capacitances of Lines

	Stripline		Microstrip	
Z_O (Ω)	50	75	50	75
t_{pd} (ns/ft)	1.74	1.74	2.27	2.27
C_O (pF/ft)	35	23	45	30

Using the values of capacitances calculated in *Table 2* and *Equation 7*, we can calculate the characteristic impedance of a transmission line loaded with 10 pF. This is shown in *Tables 3* and *4*. Values for different loads and characteristic impedances can be calculated in the same manner.

Table 3. Loaded Impedances for 50Ω Lines

	Stripline		Microstrip	
l (inch)	**Z_O (Ω)**	**Z_L (Ω)**	**Z_O (Ω)**	**Z_L (Ω)**
4	50	38.73	50	36.69
8	50	43.29	50	41.83
12	50	45.21	50	44.1

Table 4. Loaded Impedances for 75Ω Lines

	Stripline		Microstrip	
l (inch)	**Z_O (Ω)**	**Z_L (Ω)**	**Z_O (Ω)**	**Z_L (Ω)**
4	75	53.04	75	49.41
8	75	61.22	75	58.35
12	75	64.94	75	62.62

Termination Techniques

As mentioned before, we need to properly terminate the trace to reduce voltage reflections.

There are three basic types of terminations: series, pull-up/pull-down, and parallel AC. Each has its ad-

vantages and disadvantages. Parallel AC termination is usually not recommended for clock generators, since it degrades the rise time of the output clock. However, it can be used with series termination to reduce EMI.

Except for series termination, the termination network should be attached to the input (load) that is electrically the greatest distance from the source. Component leads should be as short as possible to prevent reflections due to lead inductance.

Series Termination

Series termination is accomplished by inserting a small resistor (typically 10Ω to 75Ω) in series with the transmission line, as close to the source as possible (*Figure 3*). Series termination is a special case of damping in which the series resistor value plus the clock generator output impedance equals the transmission line impedance. In this case, since there is no energy absorbed at the load (typically, loads have high input impedance) the wave will be reflected back. Using series termination resistors will prevent reflection of this reflected wave from the source. *Equation 8* shows the relationship between the output impedance of the clock generator (R_O), the series terminating resistance (R_S), and the characteristic impedance of the loaded transmission line (Z_L).

$$R_S \geq Z_L - R_O \qquad \text{Eq. 8}$$

The series terminating resistance can be greater than the difference of the characteristic impedance of the line and the output impedance of the clock generator, resulting in a slightly overdamped condition, which will still prevent reflections from the source. *Note that you will need to observe the actual clock waveform and experimentally determine the optimal value of series terminating resistance to be used.*

A disadvantage of the series-damping technique, as illustrated in *Figure 4*, is that during the two-way propagation delay time of the signal edges, the voltage at the input to the line is halfway between the logic levels, due to the voltage divider action of R_S. The "half voltage" propagates down the line to the load and then back from the load to the source. This means that no inputs can be attached along the line, because they would respond incorrectly during this time. However, you can attach any number of devices to the load end of the line because all the reflections are absorbed at the source.

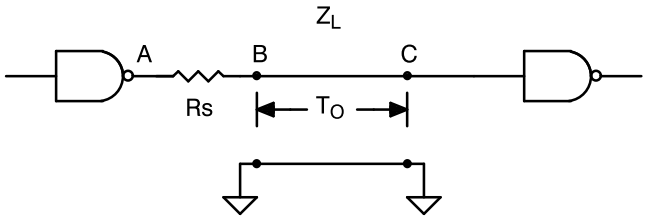


Figure 3. Series Termination

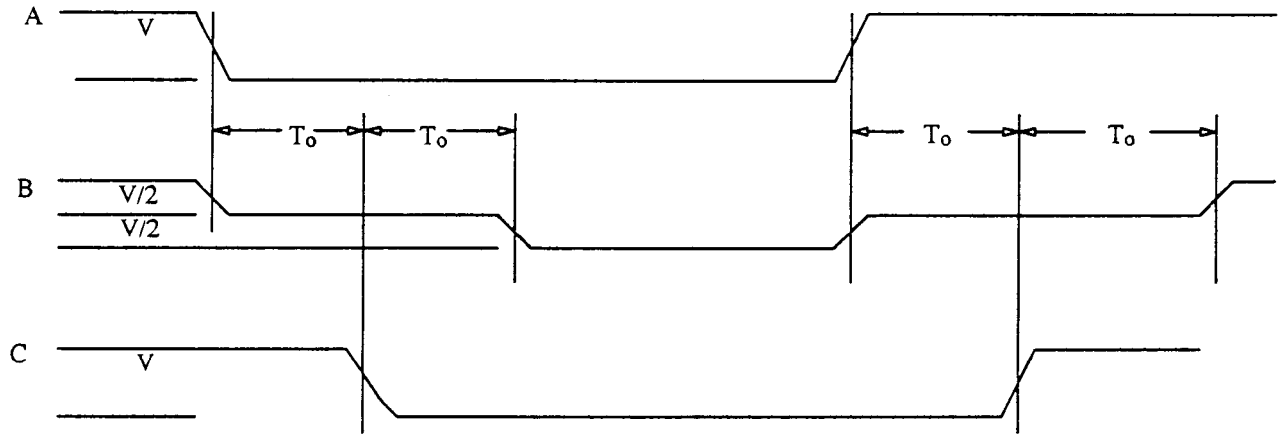


Figure 4. Series Termination Timing

The advantages of series termination are:

- Requires only one resistor per line
- Consumes little power
- Permits incident wave switching at the load after a T_O propagation delay
- Provides current limiting when driving highly capacitive loads; the current limiting also helps reduce groundbounce, and therefore, improve jitter.

The disadvantages of series termination are:

- Degrades rise time at the load due to increased RC time constant, arising from the increased resistance in series with the transmission line. Hence, choosing too high a value of series terminating resistance can cause the rise time of the signal to be very high, resulting in incomplete rail to rail swing.
- Should not be used with highly distributed loads.

The low input current required by Cypress CMOS ICs results in essentially no DC power dissipation in the series terminating resistor. The only AC power required is to charge and discharge parasitic capacitances.

Series Termination For Multiple Loads

If the clock generator is driving multiple loads, series termination can be performed in two ways, as shown in *Figures 5* and *6*. If the trace length between the two loads is less than 2" at 50 MHz, the loads can be daisy chained as shown in *Figure 5*. If the distance between the loads is more than 2" at 50 MHz, two separate traces must be driven from the source, each having its own series termination. In this case, the series termination value for each of the traces satisfies *Equation 8*. This set-up is shown in *Figure 6*.

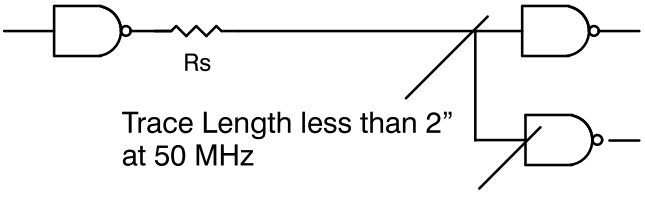


Figure 5. Series Termination, Multiple Loads

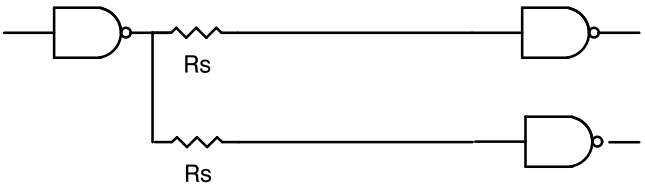


Figure 6. Series Termination, Multiple Loads

Pull-Up/Pull-Down Termination

Pull-up/pull-down resistor termination is shown in *Figure 7*. The equivalent Thévenin resistance is

$$R_T = \frac{R_1 R_2}{R_1 + R_2} \quad \text{Eq. 9}$$

The value of R_T is equal to the transmission line's characteristic impedance. To achieve an overdamped condition, R_T can be slightly less than the characteristic impedance of the transmission line.

The value of *R1* and *R2* are chosen depending on the current sourcing and sinking characteristics of the clock generator. Additionally, point B in *Figure 7* must be biased at the threshold voltage of the load, either TTL or CMOS levels.

If both resistors are used, DC power is dissipated all the time. If only a pull-down resistor (R_2) is used, DC power is dissipated when the input is in the logic HIGH state. Conversely, if only a pull-up resistor (R_1) is used, power is dissipated when the input is in the LOW state. Due to these power dissipations, this termination is not recommended.

If an unterminated control signal on a PCB is suspected of causing a problem, a resistor whose value is slightly less than the characteristic impedance of the line (e.g., 47Ω) can be connected between the input pin of the load and ground. Be sure that the driv-

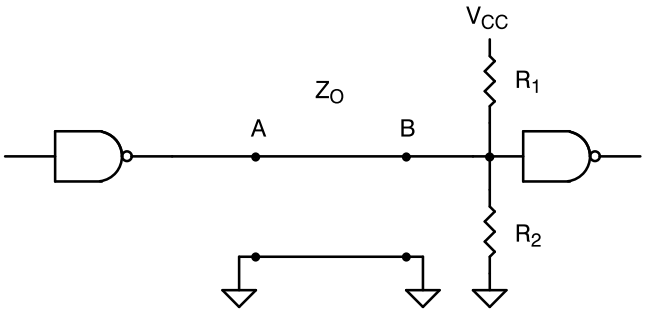


Figure 7. Pull-Up/Pull-Down Termination

er can source sufficient current to develop a TTL high voltage level (2.0V) across the resistor.

External Components

Figure 8 shows the connections of external components to a Cypress clock generator. External components such as decoupling capacitors, bulk capacitors, and ferrite beads are required to optimize system operation.

Decoupling

All decoupling capacitors must be placed on the same side as the component on the PCB. High quality, low-ESR, monolithic, ceramic, surface mount capacitors must be used, as they provide best performance. These capacitors must be connected as close to the power supply pins as is physically possible, preferably within 0.25" of the pins.

Typically, a 0.1-µF capacitor for every power supply pin of the clock generator will provide adequate decoupling. However, in certain cases, capacitors in the range of 470 pF to 2.2 nF may be required to filter high frequency noise typically caused by odd harmonics of the clock frequency. In this case, select a capacitor which will present an impedance of 1Ω at the problem frequency.

Bulk (Bypass) Capacitors

A bulk (bypass) tantalum capacitor of value between 10 µF and 100 µF can be used to prevent power supply droop when the clock generator is switching all outputs at the same time with maximum capacitive load. This capacitor can be connected to the power supply island supplying the part. Addi-

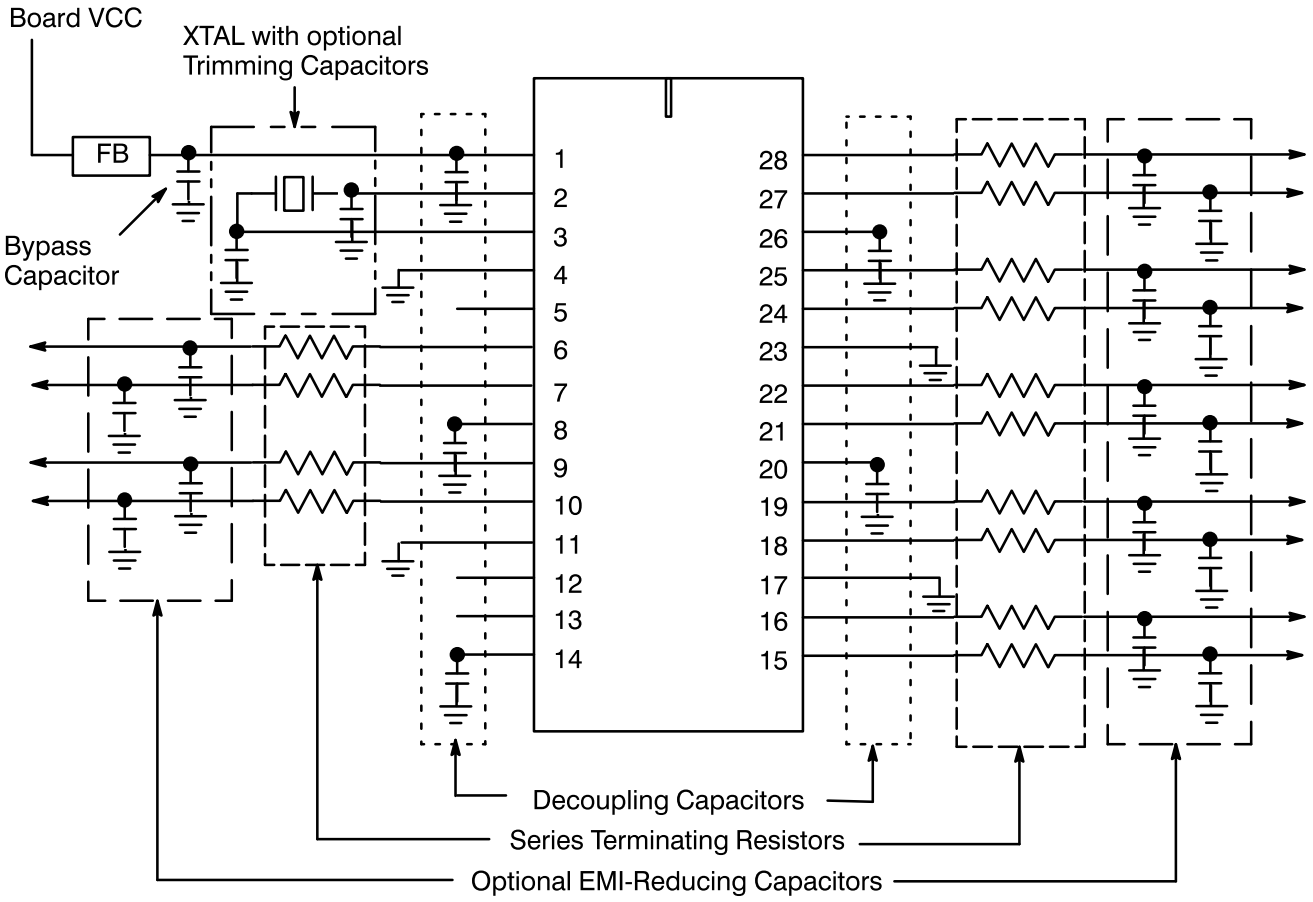


Figure 8. External Circuit for CY225X, CY226X Family

tionally, if a ferrite bead is used in the system, this bulk capacitor must be placed on the clock generator side of the ferrite bead, as close to the bead as is physically possible.

Ferrite Beads

Ferrite beads are tricky to use. You may not need to use ferrite beads on the power supply if layout, termination, and filtering are done properly. However, provide pads for ferrite beads on the board, and use a 0Ω resistor if it is not required.

Ferrite beads can be used to isolate the power supply island of the clock generator from the board power supply. Use only those ferrite beads which can provide the rated DC current to the V_{CC} island. In addition, the DC impedance of the ferrite bead must be as low as possible, preferably between 0Ω and 5Ω. At the clock frequency, the impedance of the ferrite bead must be relatively high, typically greater than 50Ω under *loaded conditions with DC current flowing through it*. (Ferrite beads from Fair-Rite Corp. (P/N 2743021447 and 2743019447) meet the above requirement. Other vendors may have similar products.) The ferrite bead will then present a large impedance at the clock frequency, and will prevent noise due to clock harmonics from spreading in the PCB.

The ferrite bead provides noise isolation only. It does not enhance or degrade the performance of the clock generator.

EMI Reducing Capacitors

On some integrated clock generators/buffers, EMI reducing capacitors may be required on the output clocks. These capacitors round the rising and falling edges of clock, and therefore, reduce the EMI radiated from the clock generator. Typically, these capacitors range in value from 4.7 pF to 22 pF. The capacitors to ground can be placed close to the terminating resistor, between the resistor and the load, or directly between the load and ground, close to the load.

Crystal Circuitry

Cypress clock generators have on-chip crystal oscillator circuitry, and therefore, can accept an external crystal as a reference source. Cypress datasheets will indicate what kind of crystal or external clock can be uses with the clock generator. Please refer to the application note, “Crystal Oscillator Topics” for more details on reference clocks.

Power and Ground Planes

There are essentially three techniques for laying out power and ground planes on a board. They are described below.

Isolated Power Plane for Clock Generator

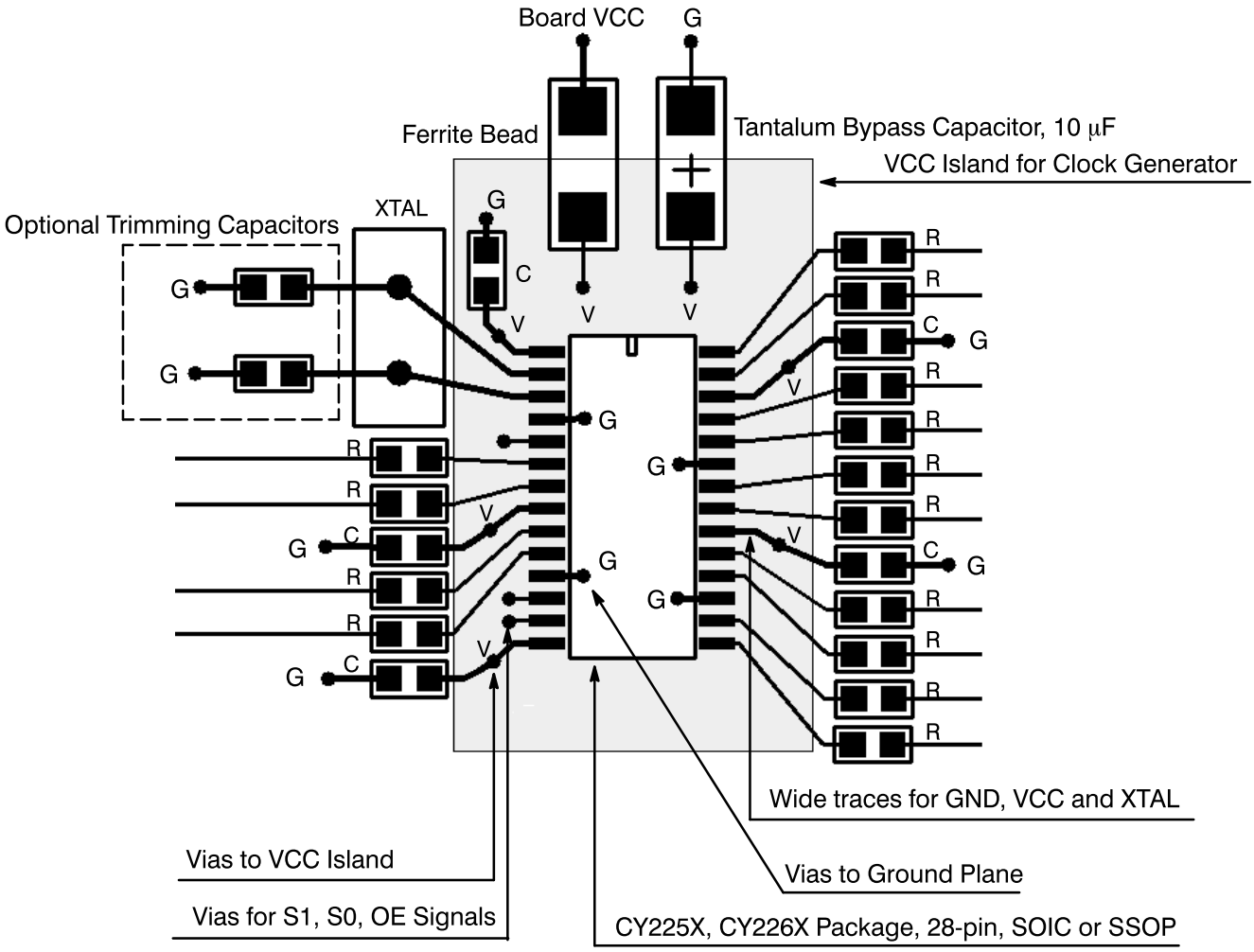
Figure 9 shows the layout diagram for the CY225X and CY226X family of clock generators. In this case, the power plane for the clock generator is isolated from the board power plane by means of a ferrite bead. Additionally, the entire board contains a common ground plane for all parts. This technique provides the maximum isolation for the clock generator’s power supply, and also prevents the clock generator noise from being distributed through the board power plane.

Power Plane for High-Speed Components

In this case, group all the high-frequency components (processor, clock generator, chipset etc.) and place them on an isolated power plane. The layout recommendations are exactly similar to the previous case.

Localized Ground Plane for Clock Generator

Alternatively, a common ground plane can be used for the entire board. However, a *continuous* localized ground plane for the clock generator is created on the *component (top)* layer of the board. This localized plane then connects directly to the board ground plane by means of the pin connections of the clock generator *and* at least two additional vias to the board ground plane. *Figure 10* shows a clock layout with the localized ground plane on the top layer, and vias to the system ground plane. An isolated power plane for the clock generator is optional in



Legend

G = Vias to Ground Plane

V = Vias to VCC Island for Clock Generator

R = Series Terminating Resistors.

C = Supply decoupling capacitors, typically 0.1 μF

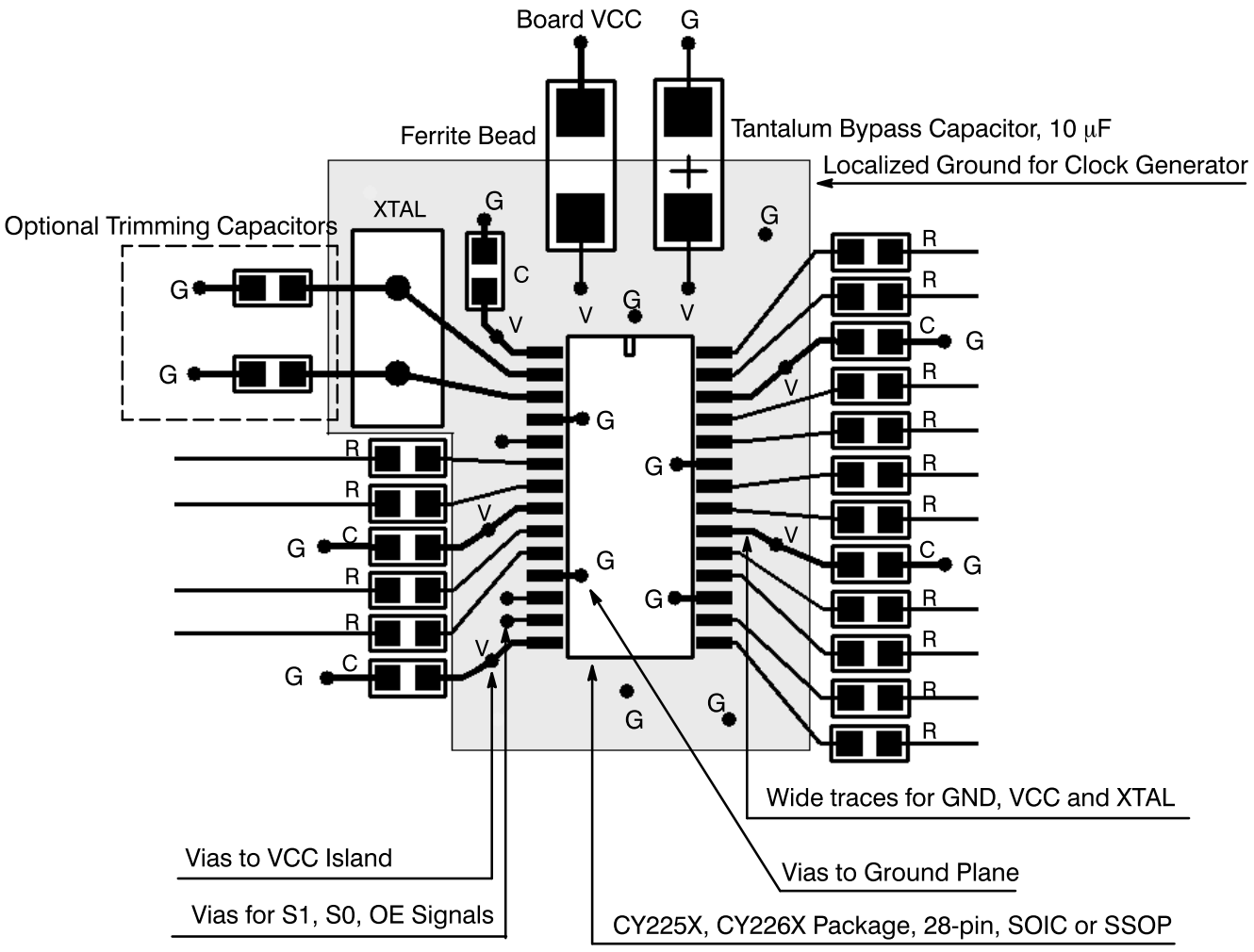
Figure 9. Layout Diagram for CY225X, CY226X Family with Isolated Power Plane for Clock Generator

this case, although it is shown in *Figure 10. Do not run traces through the localized ground plane, as it will cause small ground loops, and may result in EMI problems at higher frequencies.*

The main reason for placing a localized ground plane under the clock generator is that it provides an efficient path for RF currents to ground. The ground layer inside the PCB is two or three layers away, and hence may be an inefficient path for these RF currents.

Placement and Routing

All clock traces must be hand-routed before any other signal. Under no circumstances must the clock traces be auto-routed. Additionally, placement of the clock generator on the board is very important.



Legend

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Figure 10. Layout Diagram for CY225X, CY226X Family with Localized Ground Plane

The following are some tips on placement of the clock generator, and routing of the clock signals.

Placement

- Place the clock generator near the center of the board, and near a chassis ground.
- Place the clock generator in a manner to ensure that clock traces do not intersect each other.
- Do not use sockets. Place clock components directly on the PCB.

Routing

- Route the clock signals such that the traces do not intersect each other.
- Ensure that a minimum number of vias are used on clock signals. Vias change the trace impedance, and thus cause reflections. This could result in EMI or jitter issues. Hence, route clock traces on one layer as far as possible. If clock sig-

nals cannot be routed on one layer, ensure that they stay one layer away from either the power or ground plane, as it will cause minimal changes in trace impedance.

- Ensure that a solid ground plane is on the layer adjacent to the clock trace routing layer. Also ensure that there are no discontinuities created by vias.

- Do not route any other signals below the clock generator.

- Do not use 90˚ angles when routing clock traces. If possible, use smoothly curving traces.

- When driving multiple loads on a single clock signal, either daisy-chain the loads if the trace distance between them is less than 2" at 50 MHz, or route individual traces to each load. In the latter case, all traces should meet as close to the source as is possible, and traces must be terminated individually. Do not use "T" connections.

- Use wider traces for VCC, GND, and XTAL pins. Wider traces reduce trace inductance.

- For related clock signals which need to have a skew relationship with each other, ensure that their traces are of equal length.

- No signals should be routed in the ground plane.

Conclusion

This application note made recommendations on optimal layout, termination, and decoupling techniques for Cypress clock generators. Using the information presented in this application note will result in reliable system design and operation.

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