Everything You Need to Know About CY7B991/CY7B992 (RoboClock) But Were Afraid to Ask

Introduction

The following application note provides a detailed description of the CY7B991 and CY7B992 Programmable Skew Clock Buffers (PSCB). It also provides an overview of clock distribution and transmission line analysis. This application note is divided into the following sections:

- General Description
- Clock Distribution
- System Design Considerations
- Detailed Device Description
- AC Specifications
- AC Characterization
- DC Specifications

General Description

Figure 1 is a general block diagram of Cypress's Programmable Skew Clock Buffer (internally called RoboClock). RoboClock employs a phase-locked-loop architecture to provide output clocks that are aligned both in phase and in frequency with a reference input clock. Each of the four output pairs is controlled by two dedicated three-level function select inputs that allow the outputs to be phase adjusted by as much as ±18 ns, divided, multiplied, or inverted. In all, over 26,000 different output combinations are possible.

A three-level frequency select (FS) input selects one of three PLL operating ranges that allow the outputs of the PSCB to operate from 3.75 to 80 MHz. All of these device configurations are possible while still maintaining an output-to-output skew and a propagation delay no greater than 500 ps.

The following section discusses the effects of skew on system performance, showing why RoboClock is ideally suited for solving clock distribution problems.

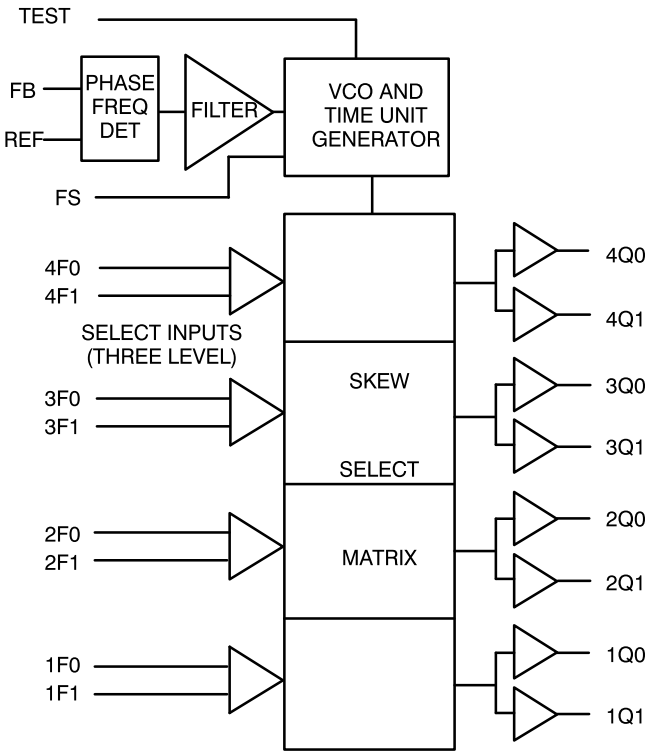

Figure 1. Logic Block Diagram

Clock Distribution

Skew is the variation in arrival time of two signals specified to occur at the same time. Skew is composed of the output skew of the driving device and variation in the board delays caused by the layout variation of the output traces.

Skew affects synchronous systems primarily in the form of clock skew. Since the clock signal drives many components of the system, and since all of these components should receive their clock signal at precisely the same time in order to be synchronized, any variation in the arrival of the clock signal at its destination will directly impact system performance. Skew directly affects system margins by eroding the predictability of the arrival of a clock edge. Because elements in a synchronized system require clock signals arrive at the same time, clock skew reduces the cycle time within which information can be passed from one device to the next.

As system speeds increase, clock skew becomes an increasingly large portion of the total cycle time. When cycle times were 50 ns, clock skew was rarely a design priority. It could be as much as 20% of the cycle time. As cycle times approach 15 ns and less, however, clock skew requires an ever-increasing amount of design resource. Typically, these high-speed systems can have only 10% of their timing budget dedicated to clock skew, so obviously, it must be reduced. The following sections will look at the two types of clock skew and how each affects system performance. The first type of skew is caused by the clock driver itself. It is referred to as intrinsic skew. The second type of clock skew is caused by the PCB layout and design and is referred to as extrinsic skew.

Clock Driver Skew (Intrinsic Skew)

Intrinisic clock skew is the amount of skew caused by the clock driver or buffer by itself. Intrinsic skew is not caused by board layout or any other design issues except for the specification stated on the clock driver data sheet. There are two main types of clock driver architectures: a buffer-type device and a feedback-type device.

Buffer Devices

In a buffer-style clock driver the input waveform propagates through the device and is “redriven” by the output buffers. This output signal directly follows the input signal. The output skew of these devices is caused by the differences in propagation delay between the input signal through the device and the precision of the matching and tuning of the internal circuit elements.

A member of this type of clock driver is the 74F244, which is available from several manufacturers. This device contains eight inputs that individually drive their respective outputs, and it is made into a clock distribution device by tying its inputs together to minimize the contribution of input skew to the device skew. The output skew of this device, if it is not listed on the datasheet, can be calculated by subtracting the minimum propagation delay from the maximum propagation delay. This calculated skew can be up to 3 ns.

This 3 ns clock driver skew does not even take into account the affects the board layout and design. In a 20- or 25-MHz system this is an acceptable amount of skew, but for systems running at 33 MHz and beyond, another method is needed.

To eliminate the device propagation delay variation that contributes to skew, manufacturers have designed devices that are specifically tuned to drive clock traces with low skew outputs. These manufacturers have specified the maximum variation in propagation delay through the device. In these devices, three types of skew parameters are usually listed. Output skew specifies the maximum amount of propagation delay variance between output pins. Duty cycle variation indicates a measure of the propagation delay difference between a LOW-to-HIGH output edge transition and a HIGH-to-LOW output edge transition. And part-to-part skew indicates the difference in output skew from device to device. Output skew of these devices has, in many cases, been reduced from the 3 ns mentioned above to 500 ps.

These devices still face the problems of device propagation delay. The propagation delay through these devices is about 5 ns. This delay will cause skew in systems where both the reference clock to the buffer and the outputs of the buffer need to be aligned.

These devices also have the drawback that the output waveform is directly based on the input waveform. If the input waveform is a non-50% duty-cycle clock, the output waveform will also have a less-than-ideal duty cycle. Expensive crystal oscillators are needed when using this type of buffer in systems requiring near 50/50 outputs.

These devices also lack the ability to phase or frequency adjust their outputs. Phase adjustment allows the clock driver to compensate for trace propagation delay mismatches and set-up and hold time differences, and frequency adjustment allows the distribution of high- and low-frequency clocks from the same common reference. Expensive additional components and time-consuming board routing techniques must be used to compensate for the functional shortcomings of these buffer-style clock driver devices.

PLL Clock Driver Devices

The second type of clock distribution device uses a feedback input that is a function of one of the outputs. This type of device is usually based upon one or more phase-locked loops (PLL) that are used to align the phase and frequency of the feedback input and the reference input. In this way the propagation delay through the device can be virtually eliminated. Cypress's Programmable Skew Clock Buffer family is based on this architecture, and will be explained in greater detail in the following sections.

In addition to very low device propagation delay, this type of architecture enables output signals to be phase shifted to compensate for board-level trace-length mismatches, and outputs can be selectively divided, multiplied, or inverted while still maintaining very low output skew.

Board Design Skew (Extrinsic Skew)

Just as the clock driver had to be evaluated to contribute minimal clock skew, the board layout and design must also be evaluated. Issues that affect board-level clock skew include trace length, capacitive loading, transmission line termination, and threshold voltages at the loads.

The time that it takes for a signal to propagate down the trace is dependent on factors such as the material that the PCB is constructed from, the length of the signal trace, the width of the trace, and capacitive loading. Variations in these factors from trace to trace will cause signals to arrive at their destination at different times.

In addition to this, threshold voltage variation on the receiving devices can play a significant role in the time of the recieved clock signals at various loads. If one load device has a threshold of 1.2V and another load device has a threshold of 1.7V and the rising edge rate is 1V/ns, there will be 500 ps of skew caused by the point at which the load device switches based on the input signal.

The most obvious way to reduce board design clock skew is to make the physical length of all clock traces the same. The propagation delay of an electrical signal down a trace is about 2 ns per foot. If one clock trace is just 3″ longer than the next, this will cause 500 ps of clock skew; which is as much skew as the clock driver itself contributes. But this is not enough. Impedance variation causes signal velocity variation, so physically matched lines may not be electrically identical.

Capacitive loading also contributes to clock skew. The differences in capacitive loading will cause differences in clock edge rate at the load. The variation between the edge rate of a lightly loaded trace and a heavily loaded trace will directly affect the time at which the clock edge crosses the input threshold and therefore the affect clock skew of these two devices.

Transmission line termination also plays a significant role in board-induced clock skew. Remember that a transmission line is any trace that has a propagation delay longer than one-half the driving device edge rate. With the extremely fast edge rates of today's clock drivers approaching 500 ps, traces with lengths of only 2″ must be considered transmission lines. Without proper termination, the clock signals

present on these traces will exhibit transmission-line effects such as voltage reflections that will, in the best case, cause a variability in clock-edge position and, at worst, might cause multiple clocking of the load.

Many of the issues mentioned in this section will be discussed in more detail in the System Design Considerations section.

System Design Considerations

Board Decoupling

Figure 2 shows the pinout for the PSCB family of devices. These parts are offered in both 32-pin PLCC and LCC packages. Each device contains 6 power pins (Vcc) and 5 ground pins. Each output pair (e.g., 1Q0 and 1Q1) have a dedicated power and ground pin immediately adjacent to them. For example, the 1Q0 and 1Q1 output pair have pins 25 and 22 as their dedicated power and ground supplies, respectively. These dedicated power pins are only used for the output driver pair. This provides the RoboClock outputs with very high drive while maintaining very high crosstalk immunity from adjacent outputs.

The other two pairs of power and ground pins are used to supply the internal PLL and associated circuitry. These power pins are completely separated from the power pins supplying the output buffers. This minimizes the output switching noise effects on the PLL and, therefore, minimizing output jitter.

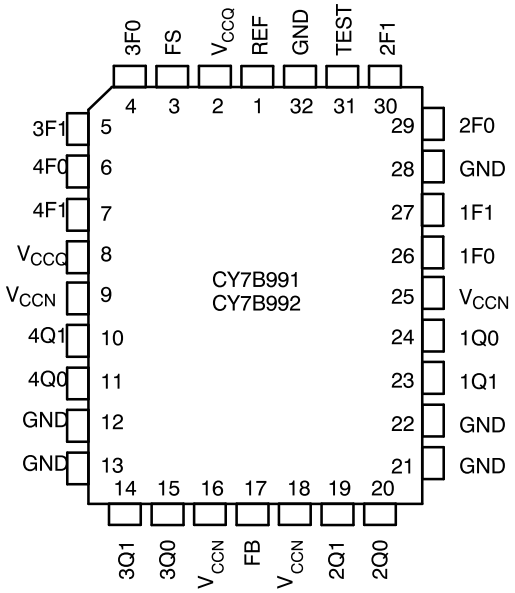

Figure 2. RoboClock PLCC/LCC Pinout

The CY7B99x family requires common high-speed power-supply decoupling and bypassing. Power-supply bypassing requires adding capacitance between the power and ground supply of a device in order to supply instantaneous current for its rapidly changing signals. This capacitor prevents the device from becoming current starved by providing the "instantaneous" transient current and thus preventing the local power-supply-voltage dip during current demands.

If all capacitors were ideal, this would be a trivial task. Capacitors, however, are not ideal. They are made up, in a first-order approximation, of an effective series inductor (ESL), effective series resistor (ESR), and a capacitor, as shown in *Figure 3.* Their response, therefore, is not constant over the frequency spectrum. At some frequencies this circuit (the bypass capacitor) will look most like a capacitor, at some frequencies an inductor, and at a particular frequency it will behave as nothing more than a resistor. This point is called series resonance and occurs when

$$\omega = \frac{1}{\sqrt{LC}} \qquad \text{Eq. 1}$$

In general, for a given capacitor construction, the series resonant frequency increases as the capacitance decreases. It would seem simple to choose a capacitor that has a series resonance at a higher frequency than the frequency of the current it needed to supply: To select a capacitor with a resonant point beyond 80 MHz, for example, if that were the operating frequency of the clock outputs. The selection process is not that simple.

Figure 4 shows the spectrum analysis of an 80 MHz clock signal with 1 ns edge rates. Notice that the fre-

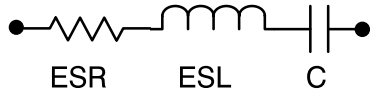

Figure 3. Equivalent Capacitor Diagram

quency components necessary to build this near ideal square wave have significant energy all the way out to 2 GHz. This means that in order to supply the current demands of these frequency components, a capacitor would have to have a series resonant frequency beyond 2 GHz. Generally available capacitors, however, have series resonant frequencies of about 400 MHz or less. These devices will be sufficient for supplying the majority of the instantaneous current.

At least two or three capacitors representing different capacitance ranges should be used for circuit bypassing. The first type of capacitor should be a 100- to 500-pF capacitor made of an NPO dielectric. This capacitor should be rated for operation at frequencies equal to or greater than 350 MHz. The second type of capacitor should be a 0.1-µF capacitor made from an X7R or a similar dielectric. This capacitor will supply the majority of the low frequency current requirements. If space permits, a third capacitor can be chosen that has a capacitance between that of the .1-µF and the 100- to 500-pF capacitors. This will provide a broad range of noise filtering and current supply.

The series resonant frequency can be decreased in two ways; lowering the capacitance or lowering the inductance. The major contributor to the inductance of a capacitor is the leads themselves. Surface-mount capacitors have a much smaller inductance than leaded capacitors and therefore have a higher resonant point. The benefits of a surface-

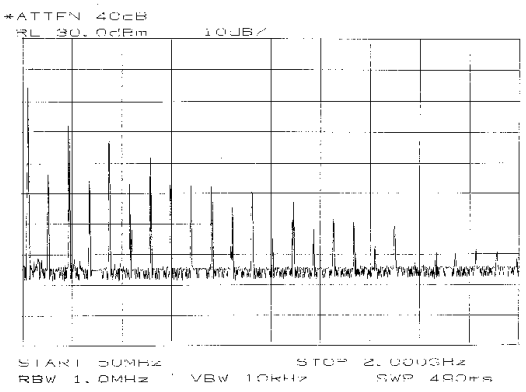

Figure 4. Frequency Components of an 80-MHz Clock Signal

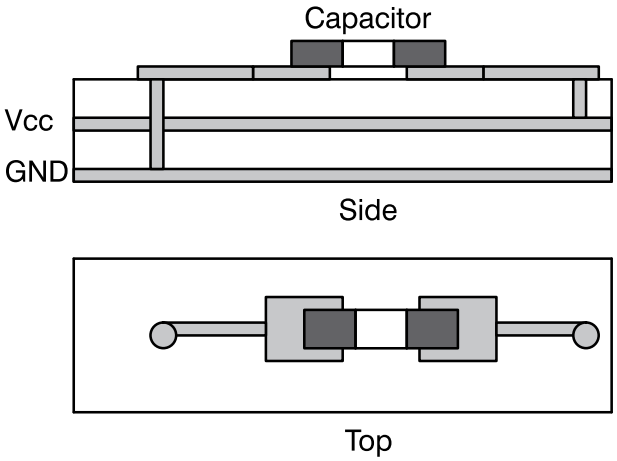

Figure 5. Typical Capacitor Layout

mount capacitor can be completely nullified, however, if it is not properly integrated into the PCB environment.

Figure 5 shows a typical method of integrating a surface-mount capacitor into a PCB environment. A surface-mount capacitor is used because of its low lead inductance, but no attention to reducing power connection trace inductance is made. In this case a leaded capacitor would provide less total inductance. The surface-mount capacitor, in this case, may not provide any high-frequency bypassing.

A better method of laying out surface-mount capacitors is shown in *Figure 6.* Here the multiple short leads are made to the power planes. The trace

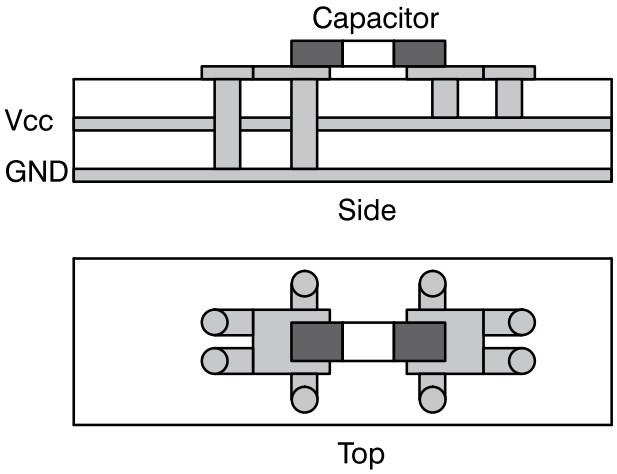

Figure 6. Better Capacitor Layout

widths and via hold sizes are also increased. These methods reduce the inductance of the power connections of the capacitor. Only when proper attention is paid to the selection and layout of the capacitor will the true benefits of circuit bypassing be realized.

Figure 7 shows a sample layout of RoboClock on a multilayer printed circuit board. This figure assumes that an internal V_{CC} and GND plane exist. The internal board V_{CC} and GND planes are connected to the device V_{CC} and GND planes through multiple via holes shown as black dots in the figure. Multiple via holes and connection of the chip power pins to local power planes reduces the amount of inductance that these pins have to their respective power connections.

Two sets of capacitors are used. They are placed on the same side of the board as the device. Each set consists of a 0.1-µF and a 100-pF high-frequency capacitors. Mutliple via holes are also included for the bypass capacitor connections to reduce the inductance that the V_{CC} pins see in series with their capacitor. The FB pin is connected to the 2Q1 pin in this diagram as an example of how easy the FB pin can be connected to either the 3Q0 and 2Q1 pins in order to reduce trace length and minimize potential problems associated with voltage reflections on transmission lines.

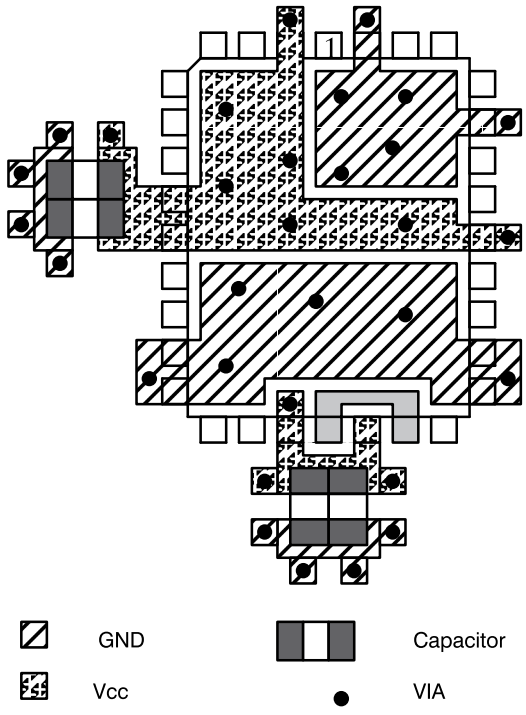

Figure 7. Sample RoboClock Layout

This layout is not the only way that these devices can be laid out, but this figure shows examples of good high-performance layout techniques. It is assumed that the board in which RoboClock will be placed will contain at least one dedicated V_{CC} plane and one dedicated ground plane and that the device will be surface mounted directly to the PCB without the use of a socket. The reason for the last constraint is that the additional lead inductance of the socket directly impacts the output skew of the device.

A more detailed discussion of series resonant frequency and other capacitor characteristics can be found in the materials supplied by capacitor manufacturers such as American Technical Ceramics [(516) 547-5700] and AVX [(803) 448-9411].

Transmission Lines

Transmission line theory states that a signal sent down a transmission line that has a constant characteristic impedance will propagate undistorted along the line. At the end, a voltage reflection will occur if the load impedance is not equal to the characteristic impedance of the transmission line. These voltage reflections are always present in electrical interconnections between devices and have traditionally been ignored. With the lengthening of Printed Circuit Board (PCB) traces and the decreasing of the edge rates of the driving element of these electrical signals, however, these effects become more pronounced. Transmission line effects cause many undesirable results in high-speed systems, such as delays and ringing. These effects will be discussed in greater detail.

In general, the effects of voltage reflections should be considered when laying out clock lines and any other PCB trace, if the propagation delay of the trace is greater than twice the faster of the rise time or fall time of the driving signal (*Equation 2*).

$$MIN[t_r, t_f] \; < \; 2\, t_{pd} \qquad \text{Eq. 2}$$

In other words, if the rise time (or fall time) of the source is less than the two-way propagation delay, then the rising signal will not hide the effects of the signal propagating down a transmission line. In this case, the switching wave will have enough time to propagate down the transmission line, reflect off of the load, and be seen at the source. These voltage reflections can cause decreased signal integrity, that will manifest itself, in the case of clock traces, as increased rise and fall times, non-ideal duty cycle performance, and possibly even unwanted clock pulses due to voltage reflections that cross the threshold of the load device.

The first step, then, in determining if a trace should be considered a transmission line, is to evaluate the propagation delay and characteristic impedance. The propagation delay is needed in order to determine when a trace must be considered a transmission line and the characteristic impedance is needed in order to determine how to reduce voltage reflections on these traces as will be shown in the section entitled Transmission Line Termination. The following discussion will focus on calculating the propagation delay and characteristic impedance on various PCB traces. This analysis, however, can be easily extended to include other types of transmission media such as coax, twisted pair, and wire-wrapped environments.

The analysis of transmission line effects on PCB traces begins with a simplified circuit analysis of the trace itself (*Figure 8).* This figure models the trace as a distributed intrinsic resistance (R_O), inductance (L_O), and capacitance (C_O). For the purposes of this discussion, a lossless transmission line will be assumed, that implies that the intrinsic series resistance will be equal to 0. The effect of this resistance on the characteristic impedance is extremely small, and only on very long traces will the effects of this component result in a noticeable drop in the voltage realized at the load.

The characteristic impedance, therefore, can be expressed as:

$$Z_0 = \sqrt{\frac{L_0}{C_0}}\ \Omega \qquad \text{Eq. 3}$$

And the propagation delay can be expressed as:

$$t_{pd} = \sqrt{(L_0 \times C_0)} = Z_0 C_0\ \ ns/length \qquad \text{Eq. 4}$$

In many cases it may be hard to measure the intrinsic inductance and capacitance of the trace in order to determine the magnitude or even the existence of transmission line effects. In this case, equations are needed in order to determine these values.

The following two sections will give equations for the characteristic impedance and propagation delay of two typical types of PCB trace construction; microstrip and strip line. Many sources exist that give an analysis of the equations listed below. Some sources give an even a more detailed analysis, but the minor differences are overshadowed by errors caused by factors not related to the analysis such as

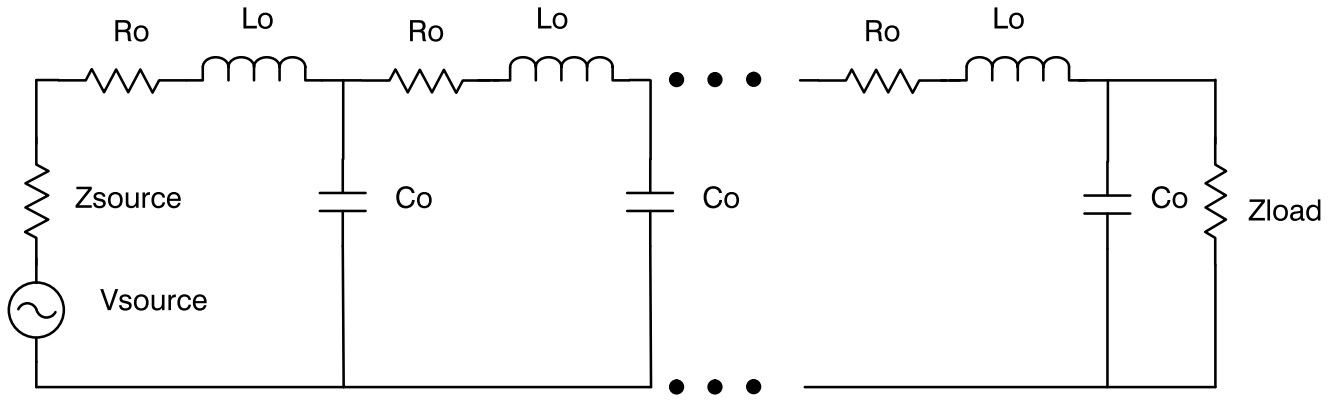

Figure 8. Simplified PCB Trace Model

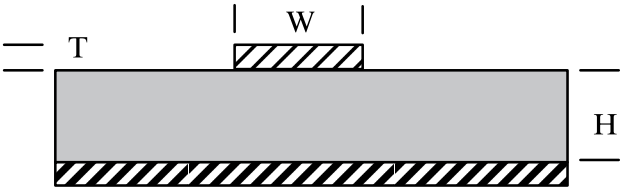

Figure 9. Microstrip

component variation and manufacturing uncertainties.

Microstrip

A microstrip trace is a signal separated from the ground plane by a dielectric, as shown in *Figure 9*. This type of trace is most commonly found as the top or bottom traces on a multilayer printed circuit board. The formula for calculating the characteristic impedance is given as:

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln\left(\frac{5.98H}{0.8W + T}\right) \quad \text{Eq. 5}$$

and the propagation delay can be expressed as

$$t_{pd} = 1.017\sqrt{0.475\epsilon_r + 0.67} \quad \text{Eq. 6}$$

where

ε_r is the dielectric constant of the material used for the PCB construction

H is the distance the trace lies away from the ground plane (board thickness)

W is the trace width (wire width)

T is the trace thickness (wire thickness)

This formula will not yield the exact impedance of the trace, but is meant as a guideline for estimating the trace impedance. Differences between the calculated and real trace impedance will be caused by slight errors in the equation itself and in process and layout variability in parameters such as dielectric constant, ground plane continuity, capacitive loading, trace width and thickness, and board thickness.

All of these variables, except for possibly the dielectric constant and trace thickness, are under the control of the designer during board layout. Dielectric constants of material used in the construction of fiberglass PCBs have a value between 4.0 and 5.5. Board manufacturers should be able to provide this parameter upon request. *Figure 10* is a graph showing how trace impedance varies with trace width and dielectric thickness. The graph assumes a dielectric constant of 4.5 and a trace thickness of 1.4 mils.

For example, if the designer wishes to create a microstrip trace with a 50Ω impedance, the designer would first have to know the thickness of the dielectric. If the board is a four-layer board (two signal layers and two routing layers) and if the trace will be on the component side with the power plane directly beneath it, then the dielectric thickness is roughly

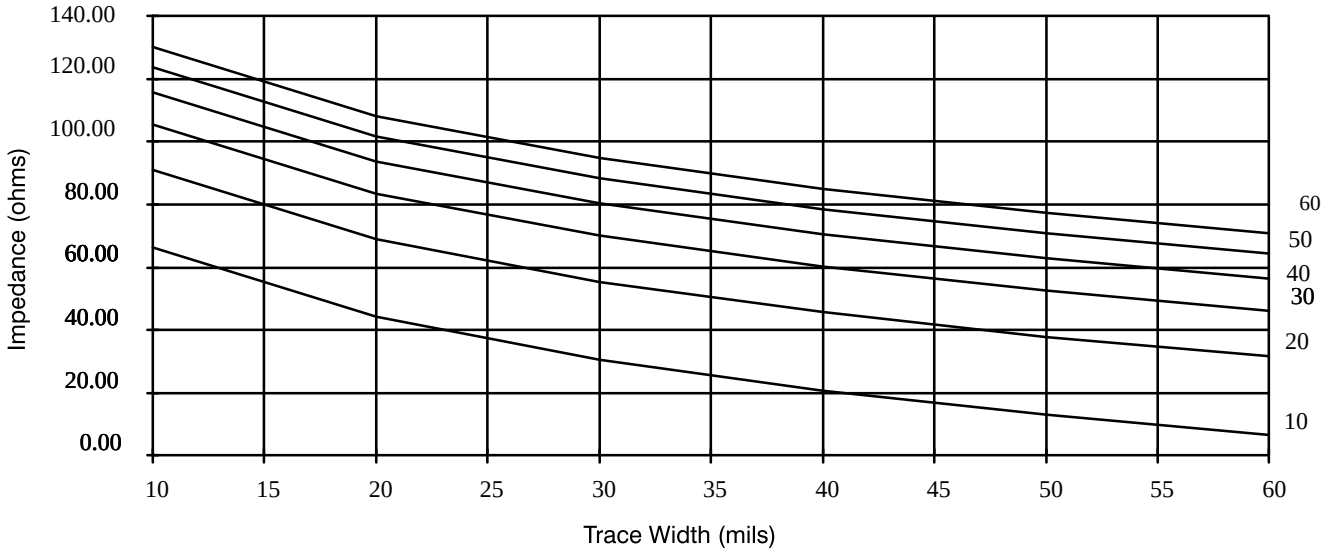

Figure 10. Impedance vs. Trace Width over Dielectric Thickness (Microstrip)

the board thickness divided by three. For a 62.5 mil board this would translate to a dielectric thickness of about 20 mils.

The designer would also have to know the thickness of the trace (approximately 1.4mils for standard 1 oz copper traces), and the dielectric constant (assume 4.4). All that is left now is the thickness of the trace, which can be directly controlled as part of the layout process. In this example, if the trace width is 36 mils, the characteristic impedance of the trace would be

$$Z_0 = \frac{87}{\sqrt{4.4 + .41}} \ln\left(\frac{5.98x20}{0.8 * 36 + 1.4}\right) = 49.68\Omega \quad \text{Eq. 7}$$

The propagation of a signal along this trace is independent of everything but the dielectric constant and is calculated in this case as:

$$t_{pd} = 1.017\sqrt{0.475 * 4.4 + 0.67} = 1.69\ ns/foot \quad \text{Eq. 8}$$

Both the equation for characteristic impedance and propagation delay will be useful for estimating the magnitude of voltage reflections and for determining the correct method of eliminating these reflections, which will be discussed in the Transmission Line Termination section.

Strip Line

Strip Line is analogous to a buried trace in a multilayered PCB between two power planes as shown in *Figure 11* .

The characteristic impedance for this type of trace can be expressed as

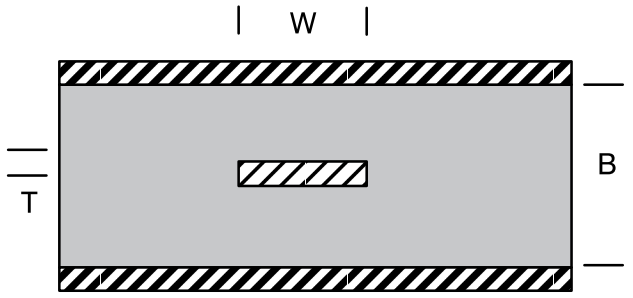

Figure 11. Strip Line

$$Z_0 = \frac{60}{\sqrt{\epsilon_r}} \ln\left[\frac{4B}{0.67\pi W\left(0.8 + \frac{T}{W}\right)}\right] \quad \text{Eq. 9}$$

For cases when

$$\frac{W}{B - T} < 0.35 \quad \text{and} \quad \frac{T}{B} < 0.25$$

With a propagation delay of

$$t_{pd} = 1.017\sqrt{\epsilon_r} \quad \text{Eq. 10}$$

Figure 12 shows how the impedance of a strip line trace varies with the trace width and dielectric thickness. The graph shows that to create a strip line trace with a 50Ω impedance in a multilayer board with 10 mils of epoxy between layers requires approximately a 7-mil trace. This assumes a trace thickness of 1.4 mils and a dielectric constant of 4.5.

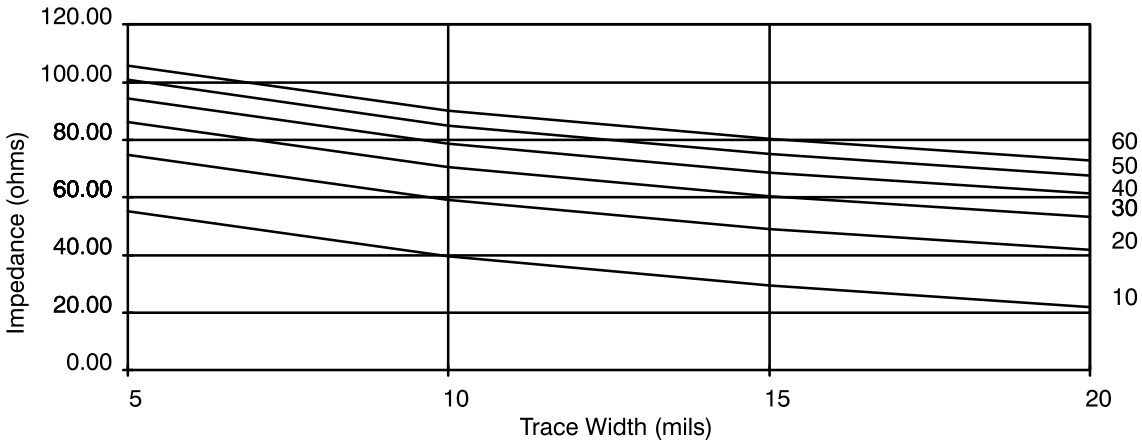

Figure 12. Impedance vs. Trace Width over Dielectric Thickness (Strip Line)

Transmission Line Effects

The previous section discussed how to calculate the characteristic impedance of a trace and the propagation rates of that signal along a trace. This section will briefly discuss the effects of transmission lines on signal integrity.

The cause of transmission line effects is impedance mismatches. These mismatches occur because of the impedance differences between the transmission line and the source and load. They are also caused by impedance discontinuities and unequal loading of the transmission line along its length. Transmission line stubs and vias are examples of impedance discontinuities otherwise known as impedance bumps.

Any time the impedance along a transmission line changes, a voltage reflection will occur. *Figure 13* shows a simplified diagram of the transmission line environment that will be used to illustrate the concept of voltage reflections.

At time 0, the voltage source provides a current source to the load equal to

$$I_S = \frac{V_S}{Z_S + Z_0'} \qquad \text{Eq. 11}$$

Since no voltage is dropped across the transmission line (assume a lossless transmission line as before), the total supplied current must be utilized by the load. If the load resistance is not equal to the characteristic impedance of the trace, a voltage reflection will occur. The reflection coefficient at the load is expressed as

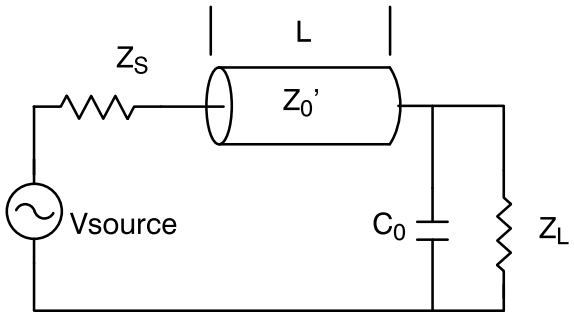

Figure 13. Simplified Transmission Line

$$\rho_L = \frac{\textit{reflected voltage}}{\textit{incident voltage}} = \frac{V_{S1}}{V_S} = \frac{Z_L - Z_0'}{Z_L + Z_{0'}} \qquad \text{Eq. 12}$$

and the reflection coefficient at the source is specified as

$$\rho_S = \frac{\textit{reflected voltage}}{\textit{incident voltage}} = \frac{V_{S2}}{V_{S1}} = \frac{Z_S - Z_0'}{Z_S + Z_{0'}} \qquad \text{Eq. 13}$$

If the load has a lower impedance than the characteristic impedance of the transmission line, then a negative voltage reflection will be sent back to the load, indicating that the load over used the available current. If the load has a higher impedance than the characteristic impedance of the transmission line, then a positive voltage will be sent back to the source, indicating that the load under used the amount of available current.

The following example shows the magnitude of these voltage reflections in a typical unterminated transmission line being driven by a CY7B991. For this example, assume the parameters have values listed in in *Table 1.*

Table 1. Sample Parameters

Param	Description	Value
ε_r	Dielectric Constant	4.4
H	Distance from ground	20 mils
T	Trace Thickness	1.4 mils
W	Trace Width	12 mils
Z_{PUS}	Source Pull-Up	25Ω
Z_{PDS}	Source Pull-Down	10Ω
L	Trace Length	6”
R_L	Load Impedance	12 KΩ
t_R	Output Rise Time	1.5 ns
t_F	Output Fall Time	1.5 ns

Solving the appropriate equations for Z_0, t_{PD}, and Z_0 yields

$$Z_0 = \frac{87}{\sqrt{4.4 + 1.41}} \ln\left(\frac{5.98 * 20}{0.8 * 12 + 1.4}\right) = 86.26\Omega \qquad \text{Eq. 14}$$

$$t_{pd} = 1.017\sqrt{0.475 * 4.4 + 0.67} = 1.66\ ns/foot \qquad \text{Eq. 15}$$

From this, the load and source reflection coefficients can be calculated:

$$\rho_{SLH} = \frac{25 - 86.26}{25 + 86.26} = -0.55 \quad \text{Eq. 16}$$

$$\rho_{SHL} = \frac{10 - 86.26}{10 + 86.26} = -0.79 \quad \text{Eq. 17}$$

$$\rho_{L} = \frac{120,000 - 86.26}{120,000 + 86.26} = 1.00 \quad \text{Eq. 18}$$

Two source reflection coefficients need to be calculated for the LOW-to-HIGH output transition and the HIGH-to-LOW output transition. The reason for this is that TTL-style output drivers have different resistances depending if they are driving HIGH or LOW. In the calculation of the source coefficients, the actual output impedances for the output drivers and the input impedance of the REF input of the PSCB were used. They are listed in *Table 1*.

This analysis assumes a transmission line exists. To confirm this, the propagation delay is used in *Equation 2:*

$$MIN[t_R, t_F] < 2 * t_{pd}'$$
$$1.5 < 2 * 1.69 \quad \text{Eq. 19}$$

A complete DC analysis of voltage reflections on this type of transmission line is not conducted here. Refer to Reference 4. at the end of this note for a sample analysis. It is important to note from this that the voltage reflection at the load is positive and the reflection at the source is negative. The opposite signs of these two reflection-coefficients and the magnitude of these two constants indicate that ringing along the transmission line could potentially cause unwanted clocks pulses to be seen at the load.

Figure 14 shows the effects of an unterminated transmission line. This plot is taken from a Tektronix DSA 602A Digitizing Signal Analyzer. This plot indicates that the the voltage scale is 1V/div and the time scale is 5 ns/div. The ground signal is indicated by the ground symbol found on the left-hand side of the figure, three voltage divisions from the bottom. The scope trigger, indicated by an arrow, is the 1.5V level of the source waveform.

This analyzer is capable of taking measurements on the waveforms. The bottom quarter of the plot displays the various measurements taken on the source waveform. The rise and fall measurements are taken between the 0.8V and 2.0V level, which is consistent with the measurement points of the CY7B991. The pulse width measurement is taken at the 1.5V level and is used to indicate the duration of time that the waveform spends above 1.5V. This is used to calculate the output duty cycle variation. The last measurement shown on this plot is the frequency. In this case, a 25-MHz source waveform is used as the trigger.

The source waveform shown in *Figure 14* is the 4Q0 output of a typical CY7B991-5. The load waveform is the end of 18″ of coaxial cable having a characteristic impedance of 50Ω In this particular example the load is completely unloaded except for the scope probe and associated connector (approximately 5 pF). As can be seen, both the source and the load are riddled with transmission line effects. This is caused by the positive voltage reflection from the load due to the infinite load impedance and the negative voltage reflection from the source due to the source impedance being less than the characteristic impedance of the coaxial cable. Notice that an additional clock pulse occurs (below the word “load” in the figure) due to voltage reflections.

A complete analysis of the voltage reflections causing this waveform would be extremely boring and

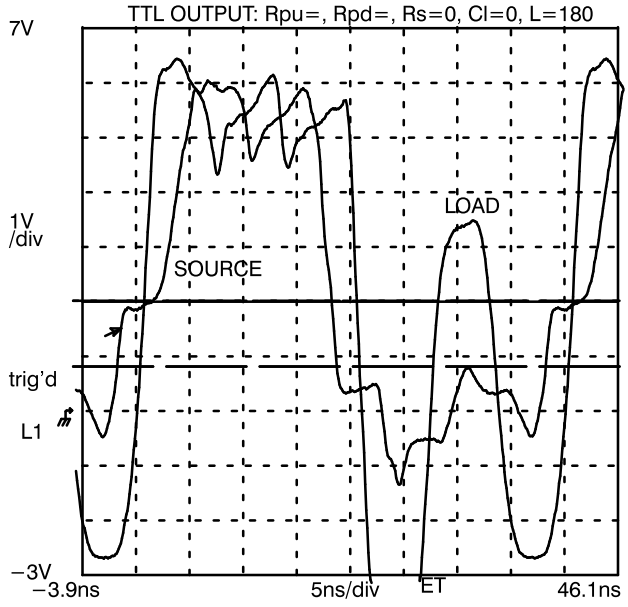

Figure 14. Unterminated Transmission Line

yield little additional information aside from the fact that this is an unacceptable clock waveform. The next section will give some methods for eliminating voltage reflections by terminating the transmission line.

Transmission Line Termination

The goal of transmission line termination is to make the source and/or load impedance match the characteristic impedance of the transmission line, insuring an optimal delivery of signal to the load. Two types of termination will be discussed: parallel termination and series termination.

Parallel Termination

Parallel termination, also known as Thevenin termination, attempts to match the load impedance with that of the transmission line. It is accomplished by placing a pull-up and pull-down resistor pair at the end of the transmission line nearest the destination as shown in *Figure 15*. The Thevenin equivalent resistance must be equal to Z_0 and the Thevenin voltage must be somewhere near the middle of the normal TTL voltage swing. Since typical CMOS inputs have steady-state impedances in the 100kΩ to 1MΩ the Thevenin resistance can be simplified to R_{PU} and R_{PD} in parallel. *Table 2* gives the recommended parallel termination resistor values for both the CY7B991 (TTL) and the CY7B992 (CMOS) devices for given transmission line impedances (Z_0).

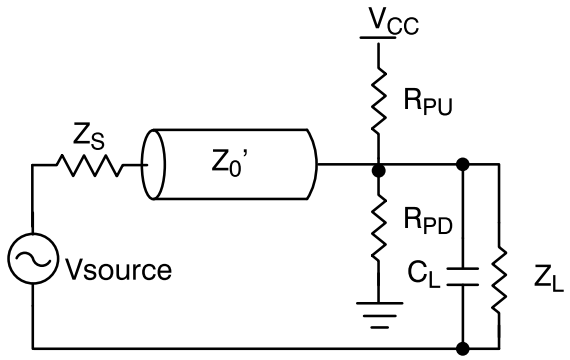

Figure 15. Parallel Termination

Table 2. PSCB Parallel Termination Recommendations

Z_0	TTL (R_{PU}/R_{PD})	CMOS (R_{PU}/R_{PD})
50Ω	130/91	100/100
65Ω	158/111	130/130
75Ω	182/128	150/150
100Ω	243/170	200/200

Figure 16 shows a 100Ω parallel termination of a transmission line with a 50Ω impedance. This figure is a plot taken from the same analyzer mentioned above. As before, the source waveform is taken at the RoboClock output pin and the load waveform is taken at the end of 18″ of coaxial cable with a 50Ω impedance. This figure shows the positive voltage reflection from the load because the load impedance is greater than the trace impedance. This reflection manifests itself as the source waveform stepping up to the 3.7V level as shown in *Figure 16*. The magnitude of the intitial source waveform in transmission line environment can be calculated by determining the the current in the transmission line before switching. The reflected voltage can be calculated by multiplying the incident voltage by the calculated reflection coefficient.

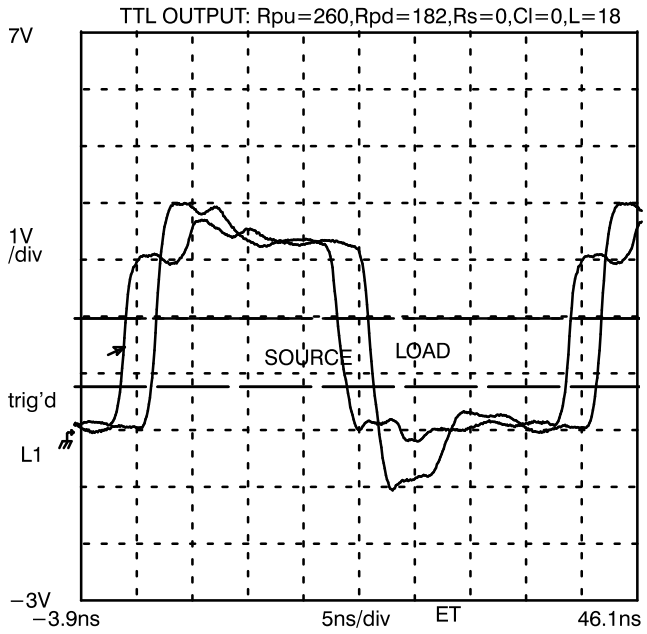

Figure 16. Unloaded 100Ω Parallel Termination

This waveform looks much better than in the previous unterminated case, but there is still a 1V undershoot at the falling edge of the waveform that may cause problems in some devices due to substrate current generation.

Figure 17 shows a 15Ω parallel termination. This transmission line is under terminated due to the fact that the load impedance is much less than the characteristic impedance of the trace. This manifests itself as a negative voltage reflection from the load. While the rising edge of this trace looks fairly good, the falling edge will cause problems. Notice that the negative voltage reflection ringing during the falling edge causes a positive-going transition in the threshold region of the load. This could cause spurious clocking.

Figure 18 shows a unloaded terminated transmission line. This transmission line, unlike in the other three cases, is terminated in its characteristic impedance. Both the source and the load waveforms are unaffected by voltage reflections. The only evidence of transmission line effects is the ringing during the HIGH and LOW time of the waveform, caused by slight impedance mismatches between the source, load, and transmission line, and the impedance "bumps" caused by the impedance differences at the various probe and coax connectors along this transmission line.

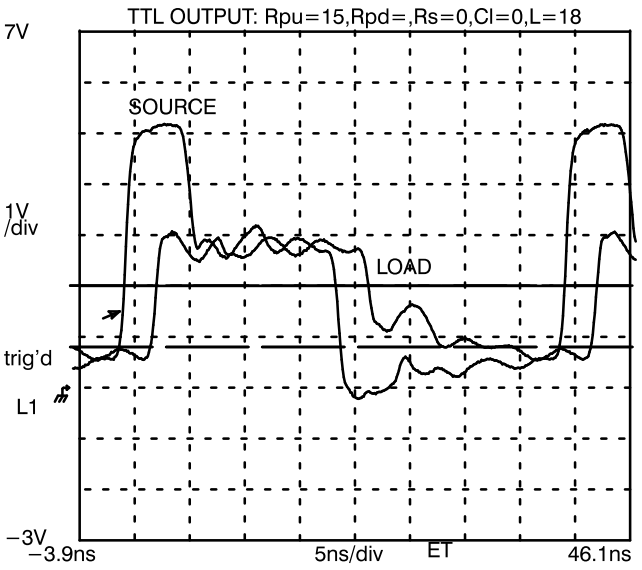

Figure 17. Unloaded 15Ω Parallel Termination

This ringing is also caused by the imperfect nature of terminating a transmission line with a complex load and source impedance. Each of the capacitances hanging on this transmission line have different impedances based on the input frequency. And, since the input waveform is a wideband signal containing many frequency components, a simple termination as given here will not eliminate all voltage reflections. The important thing to note is that this termination gives good results on the given transmission line.

Figure 19 shows a 50Ω parallel termination with a 22-pf load. Notice the voltage spikes on the source waveform. This is caused by the impedance of the load capacitor at a particular frequency being incorrectly terminated and causing a voltage reflection.

Figure 20 shows a 50Ω parallel termination with a 50-pF load. Again, the source waveform exhibits voltage glitches caused by brief negative voltage reflections, but in this case the voltage reflections come dangerously close to the input threshold region of a device that was placed on the transmission line somewhere between the source and the load shown in the figure. For this reason, it is recommended that all transmission lines drive either single loads or loads that are lumped at the end of the transmission line. If not, voltage spikes, even in

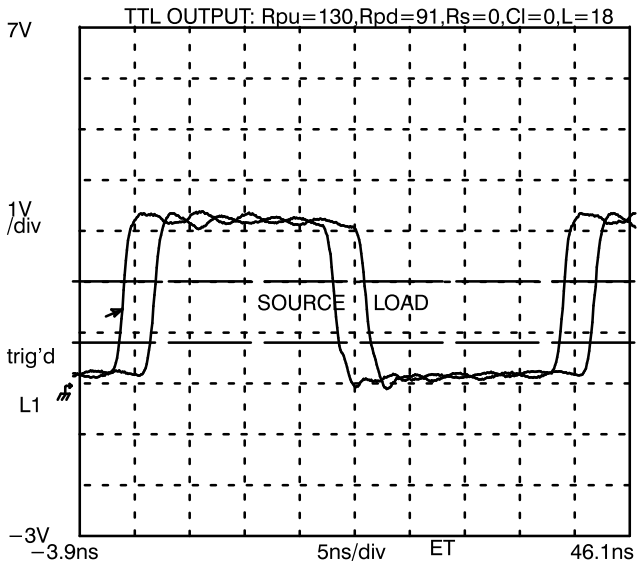

Figure 18. 50Ω Parallel Termination, Unloaded

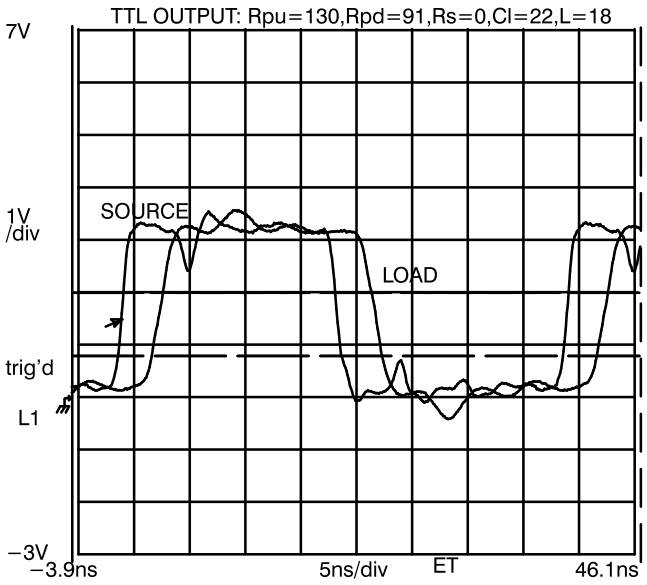

Figure 19. 50Ω Parallel Termination, 22-pF Load

reasonably well terminated transmission lines, can cause unwanted clocking.

Series Termination

The purpose of series termination is to match the source impedance with the transmission line impedance as shown in *Figure 21.* This will prevent voltage reflections occurring from the load will not reflect back from the source. The value of R_S is chosen such that the series combination of the output impedance

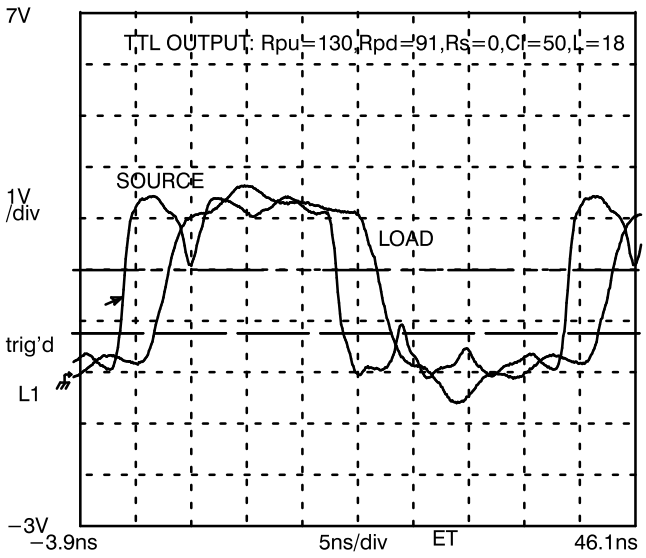

Figure 20. 50Ω Parallel Termination, 50-pF Load

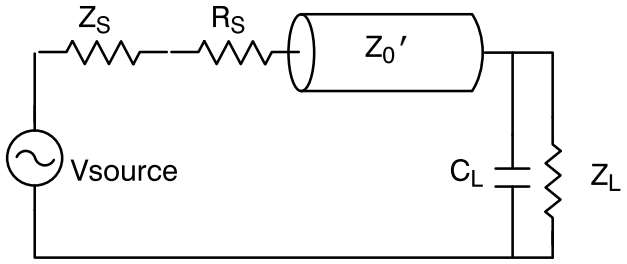

Figure 21. Series Termination

of the source devices and R_S is equal to Z_0. This series termination will absorb any voltage reflections from the load. This, however, is not a simple task.

TTL outputs have different LOW-to-HIGH and HIGH-to-LOW output impedances. The output drive has an asymmetrical output impedance. *Figure 22* shows the HIGH-to-LOW linearize Voltage vs. Current (V-I) curve for a typical CY7B991 output. The output impedance that should be used is the resistance when the output is LOW (less than 0.45V). *Figure 23* shows the LOW-to-HIGH linearized curve. The output impedance that should be used in this case is the resistance when the output is HIGH (greater than 2.4V). For these curves the output high resistance (27Ω) and the output LOW resistance (7Ω) can be determined.

Figure 24 shows an unloaded, 100Ω series terminated transmission line. This figure shows the classic "stair stepping" that occurs when a transmission line is terminated with series resistance that is too large. Several back-and-forth voltage reflections

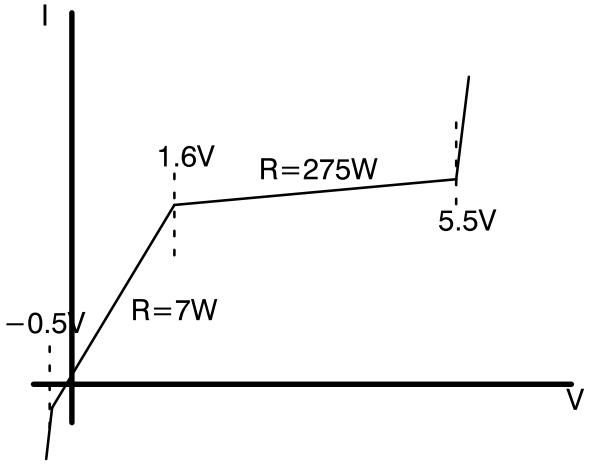

Figure 22. Output LOW Linearized V-I Curve

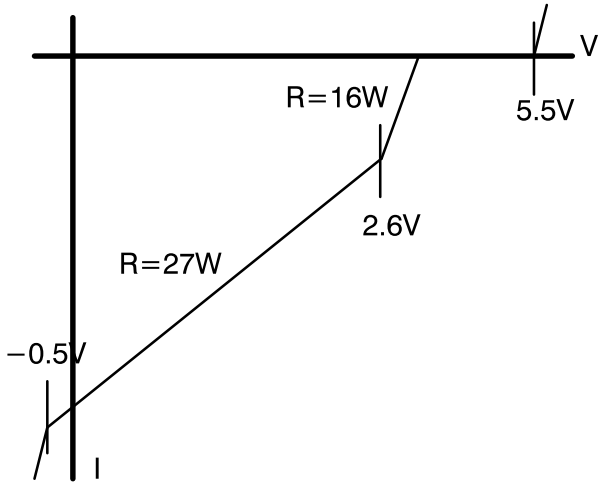

Figure 23. Output HIGH Linearized V-I Curve

are required before the load rests at its final voltage. This improper termination can cause duty-cycle distortion, increased rise and fall times, and unexpected clocking.

Figure 25 and *Figure 26* show unloaded and loaded 50Ω series terminated transmission lines, respectively. The resultant waveforms look much better in this case because the terminating resistor more closely matches the characteristic impedance.

Figure 27 shows a 27Ω terminated transmission line with a 22 pF load. The rising edge of this waveform looks much better than either of the previous two

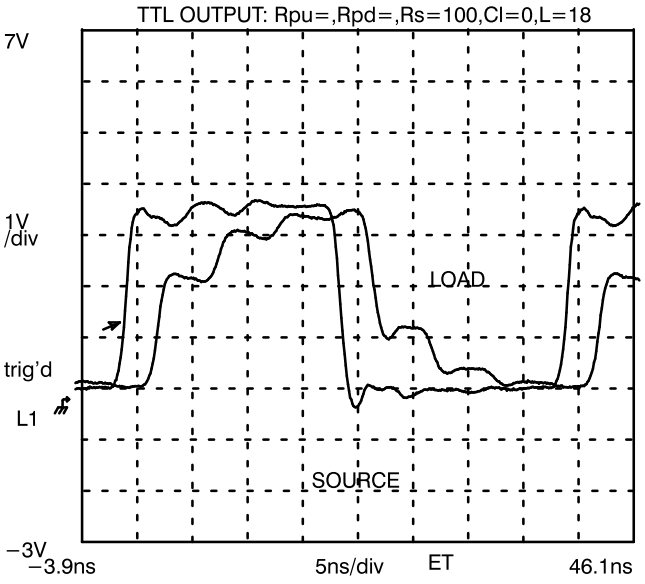

Figure 24. 100Ω Series Terminated, Unloaded

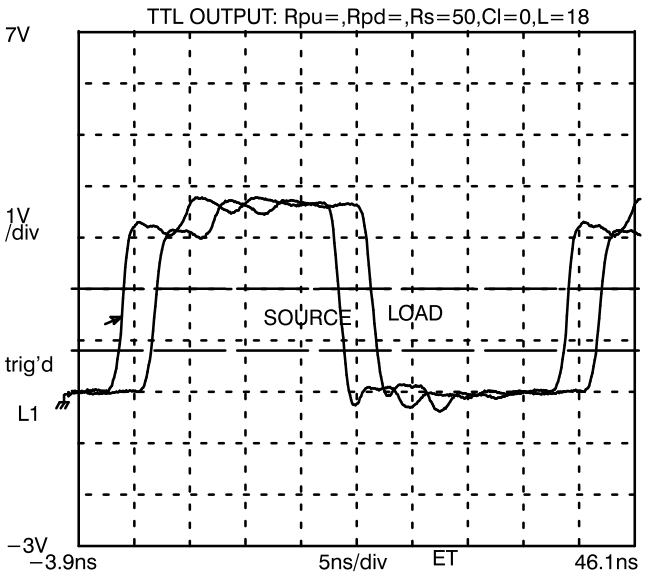

Figure 25. 50Ω Series Terminated, Unloaded

cases, but the falling edge has more undershoot than in the 50Ω termination example. The reason for this is that on the LOW-to-HIGH output transition the 27Ω terminating resistor plus the 27Ω output impedance closely match Z_0, but on the HIGH-to-LOW output transition the 27Ω resistor plus the 7Ω output impedance do not exactly match Z_0. With series termination a trade off has to be made between the LOW-to-HIGH transition and the HIGH-to-LOW transition.

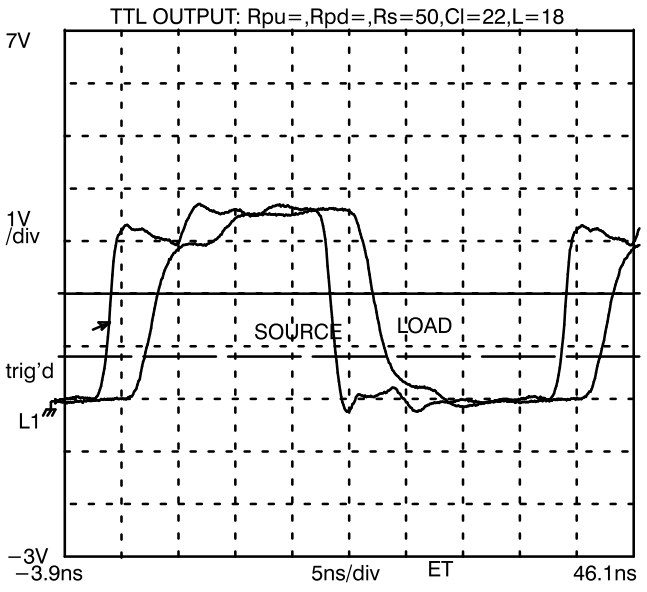

Figure 26. 50Ω Series Terminated, 22-pF Load

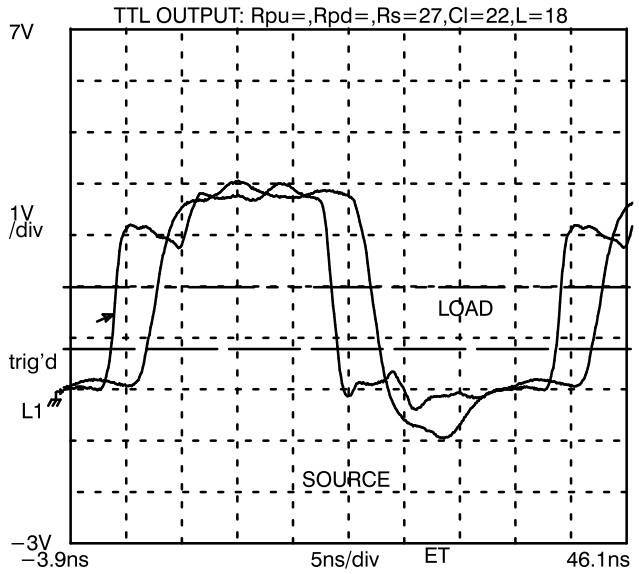

Figure 27. Series Terminated, 22-pF Load

When using series termination, no loads may exist along the transmission line. All loads have to be located at the end of the trace. The reason for this is that the series-terminating resistor acts like a voltage divider. Any loads not located at the end of the trace will see a voltage at some indeterminate level until the voltage reflection from the load builds the voltage level to its final resting value.

An advantage of series termination over parallel termination is that there is no DC power consumption. In a parallel termination, whether the output device is driving HIGH or LOW, there will always be current flow that does not drive the load but simply establishes the terminations.

Another note on transmission lines is that the rise time of the output waveform does not depend on any transmission-line loading considerations. By looking at the rise times of the source waveform in the previous example, it is clear that the method of transmission line termination and the output loading play a negligible role in the output rise time. In a properly terminated transmission line, the output rise and fall time will be a function of the characteristic impedance of the trace and the capacitive loading of the load.

The recommendation for terminating transmission lines is either a parallel termination with an $R_{TH} = Z_0$ and a $V_{TH} = 2.06V$ or a series termination where $R_S = Z_0 - 20\Omega$ If more than one load has to be driven by a single device output, make sure that all loads are located very near the end of the line, or create a “star” layout by having each load have its own trace starting at the RoboClock output. Terminate each trace as if it were the only load being driven. In the case of multiple loads being driven by a single output, the series resistor should be calculated with

$$R_S = Z_0 - \frac{20}{\#\ of\ Traces} \qquad \text{Eq. 20}$$

All lines must be matched or the loads will “talk” to each other through the voltage reflections.

Trace impedances below 50Ω can be driven by tying more than one output together. For example, a 25Ω trace can be driven by tying two outputs of the same output pair together.

Never “daisy-chain” loads together. This will not only immediately add load-to-load skew, but it will also cause unpredictable transmission line effects.

Detailed Description

RoboClock is an eight-output clock driver device. It differs from traditional clock drivers and buffers in that its outputs, while having very low output skew, can also be phase adjusted, inverted, divided, and multiplied. These capabilities would be impossible to implement in a device such as a simple redrive buffer like a 74F244. A 74F244, while potentially providing very low output skew, does not have the capability to dynamically phase adjust its outputs.

Phase adjustment allows outputs to shift in time relative to a reference point. The input clock to the device is usually taken as this reference point. Phase adjustment is useful for compensating for differences in trace delay from one load to the next, and also for equalizing differences in set-up and hold time between load devices. A 74F244 would have great difficulties shifting the arrival time of its outputs both in the positive sense (output edge arrives later that the reference edge) and in the negative sense (output edge arrives before the reference edge). In order for a 74F244 to accomplish this task, it would have to predict the time at which the next

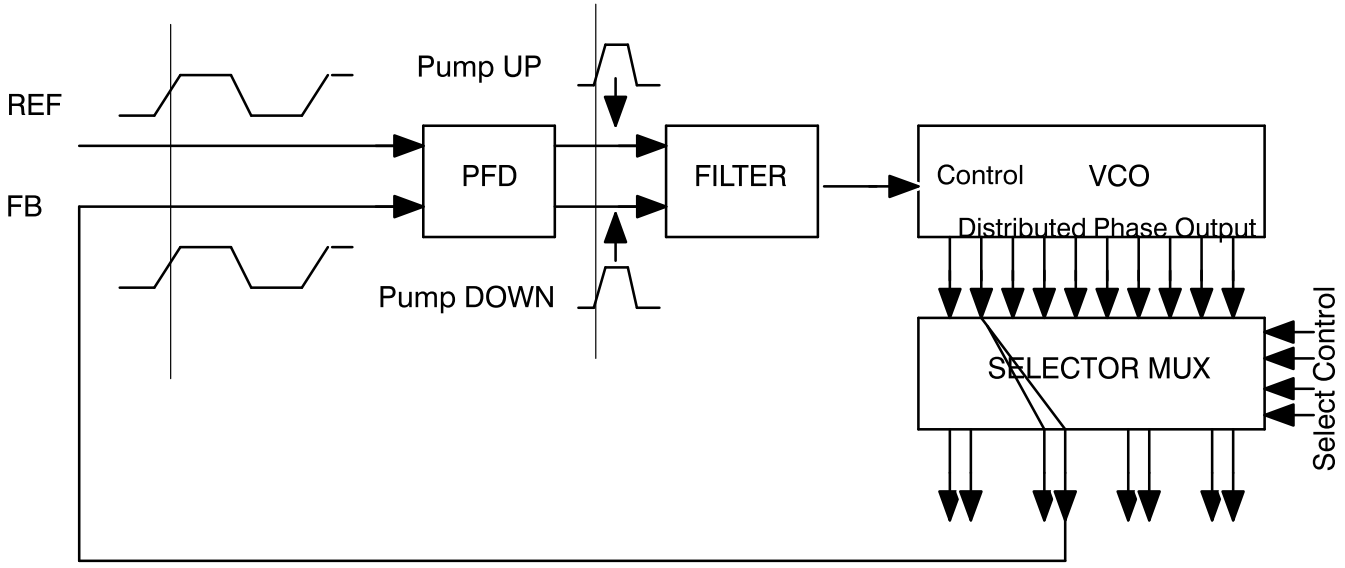

Figure 28. Simplified PLL Architecture

input edge would occur. Obviously, a new approach is needed.

PLL Operation

RoboClock includes a phase-locked loop (PLL) to achieve zero propagation delay. A completely integrated PLL allows you to align both the phase and the frequency of the reference (REF) inputs with an output. With this approach, the next occurrence of an input edge can be predicted with great accuracy while maintaining very low propagation delay through the device.

The PLL has three distinct parts; the phase/frequency detector, the filter, and the distributed-phase clock oscillator (more simply known as a voltage-controlled oscillator). In order for the PLL to align the REF input with any output, an output must be selected to be fed back to the input of the PLL. This input (FB) is then used as the alignment on which all other outputs are based. (See *Figure 1*).

Phase Detector and Filter

Figure 28 shows a simplified view of the RoboClock PLL architecture. The Phase Frequency Detector (labeled PFD) evaluates the rising edge of the REF input with respect to the FB input. If the REF input occurs before the FB input, indicating that the Voltage Controlled Oscillator (VCO) is running too slow, the PFD produces a Pump Up signal that lasts until the rising edge of the FB input. If the FB input occurs before the REF input, on the other hand, the PFD produces a Pump Down signal that is triggered on the rising edge of the FB input and lasts until the rising edge of REF. This Pump Down pulse forces the VCO to run slower. In this way, the PFD forces the VCO to run faster or slower based on the relationship of the REF and FB inputs. In the absence of a REF input, the device will function at approximately its slowest operating speed.

The Filter converts these Pump Up and Pump Down signals into a single control voltage. The magnitude of this voltage is dependent on the number of previous Pump Up and Pump Down pulses that have occurred. The range of the voltage produced by the filter is guaranteed to be able to force the VCO into any frequency within the selected frequency range.

Distributed-Phase Clock Oscillator

Figure 29 shows the Distributed-Phase Clock Oscillator ring and the Output Adjust Matrix. The RoboClock Distributed Phase Clock Oscillator (also known as a ring oscillator) has three frequency ranges of operation. These frequency ranges are se-

lected with the FS pin with range values shown in *Table 3.* At first glance, it may seem odd that a single pin (FS) has three possible selections. These three-state inputs are another feature of RoboClock. All function select inputs (FS, TEST, and xFn) have the ability to be connected to one of three states; HIGH, LOW, and MID. HIGH indicates a connection to VCC, LOW indicates a connection to Ground, and MID indicates an open connection. When a three-level input is left unconnected, internal resistors pull this input to approximately $V_{CC}/2$.

Table 3. Frequency Range Select and t_U Calculation

FS[1]	f_{NOM} (MHz) Min.	f_{NOM} (MHz) Max.	$t_U = \frac{1}{f_{NOM} \times N}$ where N =	Approximate Frequency (MHz) At Which t_U = 1.0 ns
LOW	15	30	44	22.7
MID	25	50	26	38.5
HIGH	40	80	16	62.5

The three different frequency ranges correspond to the number of stages in the oscillator. When FS is connected to ground, the oscillator contains its maximum number of stages: 22. When FS is left unconnected, the oscillator contains 13 stages. And when FS is connected to ground, the oscillator contains its minimum number of stages: 8. The operating frequency of the oscillator can be calculated with the following formula:

$$f = \frac{1}{N * t_U} \qquad \text{Eq. 21}$$

where N is the number of stages and t_U is the delay through each stage. The reason that N at the bottom of *Equation 21* is twice the number of stages in the oscillator is because, in order for the ring to oscillate, first the true and then the inverted signal must pass through each stage of the oscillator. This is accomplished through an inversion from the last stage to the first stage.

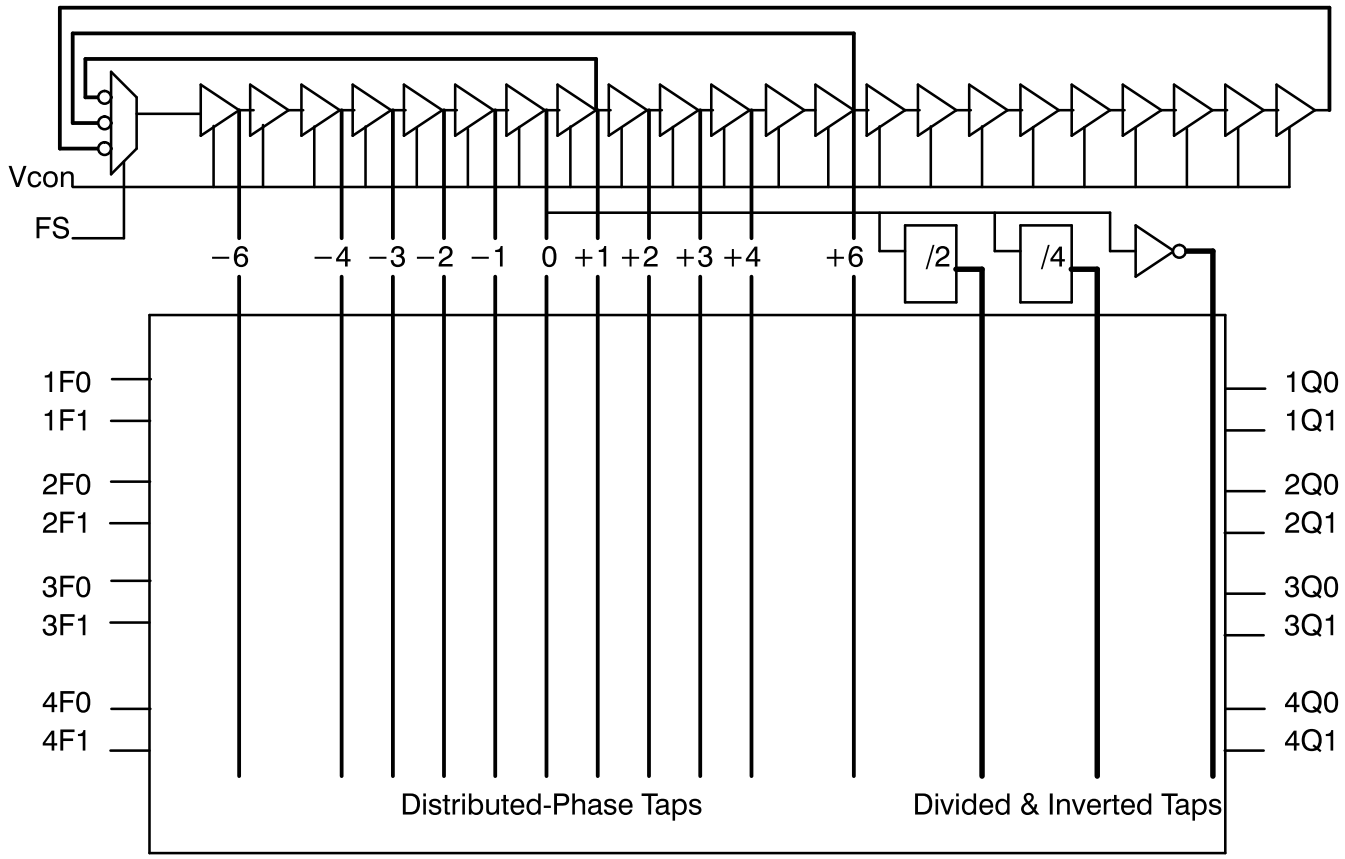

Figure 29. Distributed-Phase Clock Oscillator and Output Adjust Matrix

For example, if the delay through each stage is exactly 1 ns and the FS pin was tied to ground, then the operating frequency would be

$$f = \frac{1}{2 * 22 * 1ns} = 22.7\ MHz \qquad \text{Eq. 22}$$

The delay through each stage is controlled by the voltage on the V_{CON} line, which is simply the voltage generated by the PLL filter. From *Table 3* it is obvious that some overlap exists between the various frequency ranges. This allows a choice of stage delays within some frequency ranges, which in turn allows system designers a choice of two different increments of phase adjustment.

Within the first thirteen stages of the oscillator, 11 taps are sent to the Output Adjust Matrix. These taps represent various phase relationships to the center, or 0 time unit (t_U) position. The taps range from $-6\ t_U$ to $+6\ t_U$, as shown in *Figure 29.* This allows the outputs to shifted, either early or late, with respect to the FB input to adjust for various system requirements.

The value of t_U shown in *Figure 30* is determined by the operating frequency and the number of stages in the distributed phase oscillator. The formula for calculating t_U is shown in *Table 3* and given here:

$$t_U = \frac{1}{f_{nom} \times N} \qquad \text{Eq. 23}$$

For example, *Equation 24* calculates the stage delay (t_U) when the ring oscillator is running at 25 MHz and the FS pin is tied to ground

$$t_U = \frac{1}{25MHz \times 44} = 0.91\ ns \qquad \text{Eq. 24}$$

The value of t_U, on the other hand, if the FS pin were left unconnected, is

$$t_U = \frac{1}{25MHz \times 26} = 1.54\ ns \qquad \text{Eq. 25}$$

This shows that at the same operating frequency (f_{NOM}), two different stage delays are possible, depending on the connection of the FS pin.

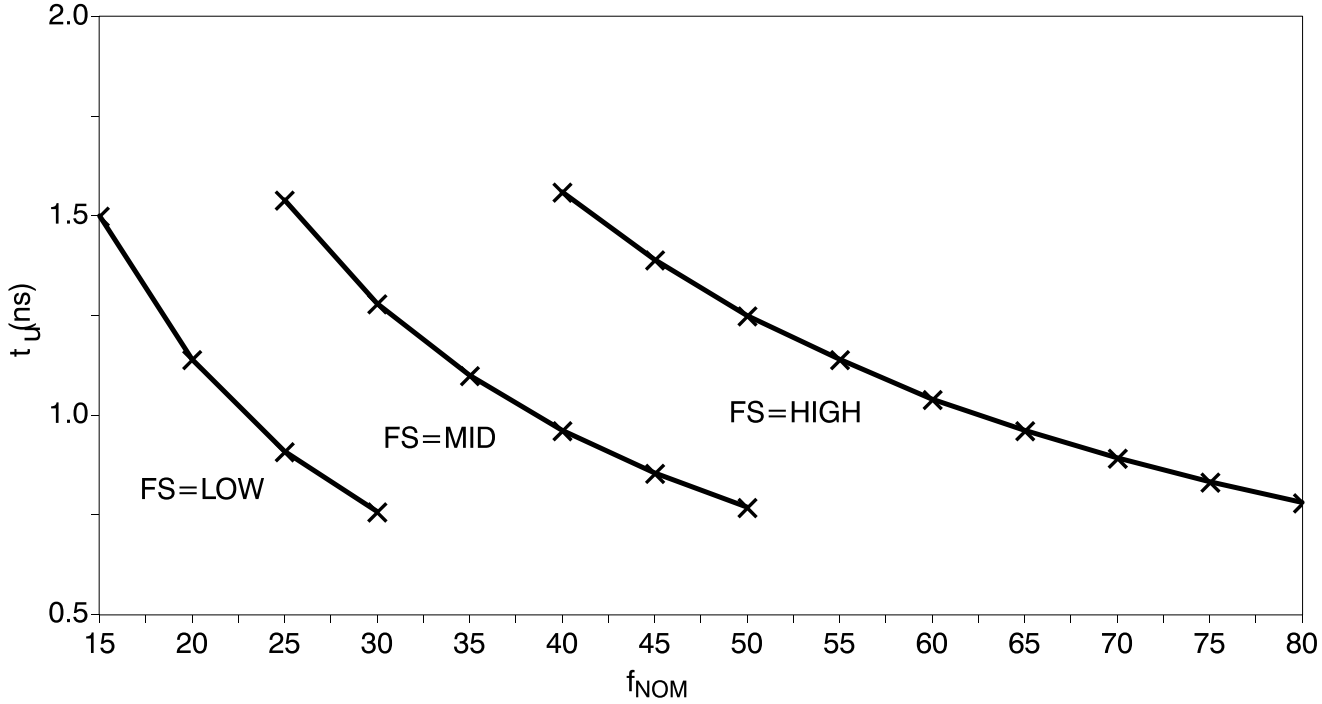

Figure 30. Time Unit (t_U) vs. Frequency

Output Adjust Matrix

The output adjust matrix allows the outputs to be configured in up to 26,000 ways (more on this later). The output options are generated by the Distributed Phase Clock Oscillator, and selected by the output function select (xFn) inputs.

In addition to the 11 taps from the distributed phase oscillator, the Output Adjust Matrix contains a divide-by-two option, a divide-by-four option, and an invert option.

The eight RoboClock outputs are configured as four output pairs. Each member of a pair of outputs operates identically to the other. The output adjustment for each output pair is controlled by its associated pair of function select inputs. For example, the 1Qn outputs are controlled by the 1Fn inputs.

The function select inputs are three-state inputs that operate in the same manner as the FS input. These inputs can be tied HIGH, tied LOW, or left unconnected (MID). The three-level input capabilities of the function select inputs allow each output to have nine different output selections with the use of only two pins.

Each pair of outputs has nine different possible output timing positions based on the appropriate connection of the function select input. The possible output combinations are shown in *Table 4*. These output adjustment configurations assume that an output with a 0 t_U configuration is used as the FB input. Output adjustment configurations with a non-0 t_U tap output selected as the FB input will be discussed in the section titled Change in Operation with FB selection.

The following example refers to *Figure 31. A*ssume that 2Q0 is used as the FB input and that 2F1 and 2F0 are both left unconnected. This will select both of the 2Qx outputs to have a 0-phase-adjusted output (0 t_U), and by connecting 2Q0 to the FB input it will also force these outputs to be phase and frequency aligned with the REF input.

Table 4. Output Adjustment Configurations

Function Selects		Output Functions		
1F1, 2F1, 3F1, 4F1	**1F0, 2F0, 3F0, 4F0**	**1Q0, 1Q1, 2Q0, 2Q1**	**3Q0, 3Q1**	**4Q0, 4Q1**
LOW	LOW	$-4t_U$	Divide by 2	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4	Inverted

If, in this scenario, 1F1 were tied to ground and 1F0 were left unconnected, then the 1Q0 and 1Q1 output edges would precede the output used as the FB input (2Q0 in this case) by three time units. Alternately, if 1F1 were tied HIGH and 1F0 were again left unconnected, then the 1Q0 and 1Q1 output edge would follow the 2Q0 output by three time units.

If 3F1 and 3F0 were both tied HIGH, then the 3Qn outputs would both operate at one-quarter the frequency of the 2Qn outputs. And if the 4Fn function select inputs were both tied LOW, the 4Qn outputs would both operate at one-half the frequency of the 2Qn outputs.

An important point to note is the frequency and phase relationship between the 1/2 and 1/4 outputs

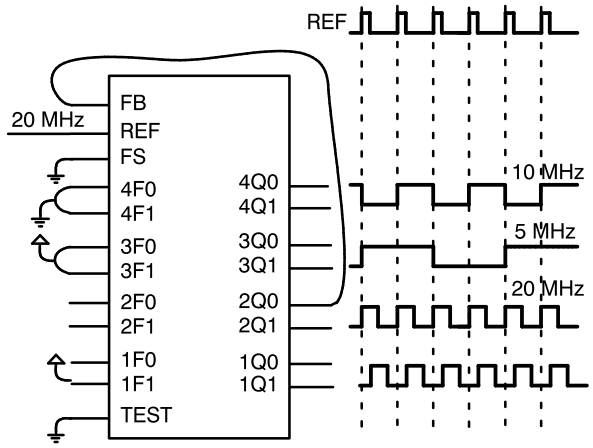

Figure 31. Frequency Divider Connections

(3Qn and 4Qn). The divide-by-two and divide-by-four outputs fall at the same time, but never rise at the same time. This feature of RoboClock makes it possible to use the rising edges of the 1/2 frequency and 1/4 frequency outputs without concern for skew mismatch. It also provides the ability to clock different parts of the system on different phases of the master clock.

The previous example showed the phase shifting and frequency division capabilities of RoboClock. Another output feature available on the 4Qx outputs is phase inversion. This output adjustment is configured by tying both 4F1 and 4F0 inputs HIGH. In this mode the 4Qx outputs will have and inverted sense with respect to the FB input.

Change in Operation with FB Selection

The previous discussion assumed that an output with a 0 t_U phase adjustment was used as the FB input. With this assumption, RoboClock has nearly 3000 different configurations. This is calculated by taking the number of possible configurations of each output pair (9) to the number of outputs pairs not being used as the FB input (3) times the number of choices of output pairs to be used as the FB input.

$$Combos = 9^3 * 4 \qquad \text{Eq. 26}$$

If the output used as the FB input is also phase or frequency adjusted, then RoboClock offers over 26,000 different configurations.

Phase Adjusted Output Used as FB Input

By feeding back an output that was selected for 0 t_U, all of the other outputs were referenced from the 0 tap position shown in *Figure 29*. This is due to the fact that the PLL aligns the REF input and the FB input in both phase and frequency.

It is not necessary to use an output with a 0 t_U configuration as the FB input. An output with any configuration can be used as the FB input. For example, if an output with a -3 t_U tap was used as the FB input, the PLL would align this output with the REF input. It would no longer exhibit a shift of -3 time units when compared with REF. The output used as the FB input is always aligned with REF.

By using an output with this configuration as the FB input, all other outputs are now referenced to this tap position within the ring oscillator. The possible tap selections for the other outputs are still the same as in the 0 tap used as FB case, but now they have a -3 tap time reference. The $+6$ tap can still be selected as an output configuration, but it will occur 9 time units after the FB output. The -6 tap can also be selected as an output configuration, but instead of occurring 6 time units before the corresponding edge of FB, it will occur 3 time units before the output used as the FB input.

Tables 5 through *7* illustrate the various possible output configurations with different FB selections. *Table 5* gives the 2Qn, 3Qn, and 4Qn output configurations when a 1Qn output is used as the FB input. It also gives the 1Qn, 3Qn, and 4Qn output configurations when a 2Qn output is used as the FB input. The reason for this is that the 1Qn and 2Qn outputs have the same possible configurations. If either is used as the FB input, the other outputs will have the same output configuration options.

Table 5 is broken into three parts corresponding to the configurations for each of the three pairs of outputs not used as the FB input. The leftmost two columns of each table indicate the various configurations of the FB input, and the right portion of the table gives the output possibilities for the given output.

For example, the first part of *Table 5* gives the possible output configurations for the 2Qn outputs assuming that a 1Qn output is used as the FB input. Alternately, this table gives the output configurations for the 1Qn outputs assuming a 2Qn output is used as the FB input. This is true because the 1Qn and 2Qn outputs have the same possible output configurations as shown in *Table 4*. For the remainder of this example, a 1Qn output is assumed to be the FB input.

The left side of the table gives the function select input settings for the FB output. L represents a connection to ground, M represents an input left open, and H represents an input connected to V_{CC}. Once a selection is made for the function select inputs of

the FB output, all of the other outputs will be referenced to that tap.

For example, if the 1F1 input is tied to ground and the 1F0 input is left unconnected, then all of the other outputs will be referenced to the -3 t_U tap used as the FB input. The available configurations on the remaining outputs will remain the same as given in *Table 4*, but the values in this table will all be shifted by $+3$ because this is the number of stage delays between the new reference point and 0 t_U, the reference point of *Table 4*.

All of the possible output configurations can be found in the same row in the following tables as the selection made for the FB output. If 1Fn = LM (1F1 tied to ground, and 1F0 left unconnected), then the possible selections for the 2Qn output are from -1 t_U to $+7$ t_U. This is shown in the first part of *Table 5* as a shaded row. By connecting 2Fn = HM, the 2Qn outputs will have outputs that lag the FB outputs by 6 time units or by connectng 2Fn = LL the 2Qn outputs will precede the reference by 1 time unit (-1t). Once the output configurations for the FB input are made, all other outputs will be referenced to this new reference point.

The second part of *Table 5* gives the possible output configurations for the 3Qn outputs. Assuming a 1Qn (2Qn) output is used for the FB input, the 3Qn outputs can be phase shifted with a granularity of 2 time units from -3 to $+9$ with respect to the FB input. Additionally, the 3Qn outputs can be divided by two and divided by four, but since the reference point for the dividing circuit for these configurations is the 0 tap (as shown in *Figure 29*), these outputs are shifted by three time units with respect to the FB input.

The third part of *Table 5* gives the possible output configurations for the 4Qn outputs, again assuming that a 1Qn output is used as the FB input. This table looks much the same as the second part with the only exception being the last column. The only difference between the 3Qn and 4Qn outputs is the ability to divide by four or invert respectively. The last column shows how RoboClock can be configured to phase shift and invert an input signal.

Table 5. 1Qx or 2Qx Output Connected to FB Input (Part 1)

1Qn(2Qn)➧FB		2Qn(1Qn) Outputs with respect to FB										
		Input Select	2F1 (1F1)	L	L	L	M	M	M	H	H	H
1F1 (2F1)	1F0 (2F0)		2F0 (1F0)	L	M	H	L	M	H	L	M	H
L	L	Output Configuration		0t	+1t	+2t	+3t	+4t	+5t	+6t	+7t	+8t
L	M			−1t	0t	+1t	+2t	+3t	+4t	+5t	+6t	+7t
L	H			−2t	−1t	0t	+1t	+2t	+3t	+4t	+5t	+6t
M	L			−3t	−2t	−1t	0t	+1t	+2t	+3t	+4t	+5t
M	M			−4t	−3t	−2t	−1t	0t	+1t	+2t	+3t	+4t
M	H			−5t	−4t	−3t	−2t	−1t	0t	+1t	+2t	+3t
H	L			−6t	−5t	−4t	−3t	−2t	−1t	0t	+1t	+2t
H	M			−7t	−6t	−5t	−4t	−3t	−2t	−1t	0t	+1t
H	H			−8t	−7t	−6t	−5t	−4t	−3t	−2t	−1t	0t

Table 5. 1Qx or 2Qx Output Connected to FB Input (Part 2)

1Qx(2Qx)➧FB		3Qn Outputs with respect to FB										
		Input Select	3F1	L	L	L	M	M	M	H	H	H
1F1 (2F1)	1F0 (2F0)		3F0	L	M	H	L	M	H	L	M	H
L	L	Output Configuration		+4t f/2	−2t	0t	+2t	+4t	+6t	+8t	+10t	+4t f/4
L	M			+3t f/2	−3t	−1t	+1t	+3t	+5t	+7t	+9t	+3t f/4
L	H			+2t f/2	−4t	−2t	0t	+2t	+4t	+6t	+8t	+2t f/4
M	L			+1t f/2	−5t	−3t	−1t	+1t	+3t	+5t	+7t	+1t f/4
M	M			0t f/2	−6t	−4t	−2t	0t	+2t	+4t	+6t	0t f/4
M	H			−1t f/2	−7t	−5t	−3t	−1t	+1t	+3t	+5t	−1t f/4
H	L			−2t f/2	−8t	−6t	−4t	−2t	0t	+2t	+4t	−2t f/4
H	M			−3t f/2	−9t	−7t	−5t	−3t	−1t	+1t	+3t	−3t f/4
H	H			−4t f/2	−10t	−8t	−6t	−4t	−2t	0t	+2t	−4t f/4

Table 5. 1Qx or 2Qx Output Connected to FB Input (Part 3)

1Qn(2Qn)➧FB			4Qn Output with respect to FB									
		Input Select	4F1	L	L	L	M	M	M	H	H	H
1F1 (2F1)	1F0 (2F0)		4F0	L	M	H	L	M	H	L	M	H
L	L	Output Configuration		+4t f/2	−2t	0t	+2t	+4t	+6t	+8t	+10t	+4t INV
L	M			+3t f/2	−3t	−1t	+1t	+3t	+5t	+7t	+9t	+3t INV
L	H			+2t f/2	−4t	−2t	0t	+2t	+4t	+6t	+8t	+2t INV
M	L			+1t f/2	−5t	−3t	−1t	+1t	+3t	+5t	+7t	+1t INV
M	M			0t f/2	−6t	−4t	−2t	0t	+2t	+4t	+6t	0t INV
M	H			−1t f/2	−7t	−5t	−3t	−1t	+1t	+3t	+5t	−1t INV
H	L			−2t f/2	−8t	−6t	−4t	−2t	0t	+2t	+4t	−2t INV
H	M			−3t f/2	−9t	−7t	−5t	−3t	−1t	+1t	+3t	−3t INV
H	H			−4t f/2	−10t	−8t	−6t	−4t	−2t	0t	+2t	−4t INV

Tables 6 and *7* have slightly different output configurations. These tables represent the possible output configurations when a 3Qn or 4Qn output is used as the FB input.

The first part of *Table 6* gives the possible output configurations for the 1Qn (2Qn) outputs when a 3Qn output is used as the FB input. When the 3Qn outputs are configured from $-6\ t_U$ (3Fn = LM) to $+6\ t_U$ (3Fn = HM) the 1Qn outputs have a range of $+10\ t_U$ (1Fn = HH) to $-10\ t_U$ (1Fn = LL). This, again, is because if the 3Qn outputs have a −6 tap reference and the +4 tap is selected for the 1Qn outputs, then the total time delay between the FB input and the 1Qn output is +10 time units. This feature gives RoboClock a tremendous phase adjustment range.

What if a divided output is used as the FB input? The last row of *Table 6* (Part 1) shows that if 3Fn = HH (3Qx in divide-by-four mode), then all of the outputs are multiplied by four. RoboClock has become a frequency multiplier. To understand why this happens, remember that the PLL aligns the FB with the REF input in both phase and frequency. Even though the 3Qn outputs were selected to divide by four, the PLL forces them to run at the same rate as the REF input. This means that, in order for these outputs to operate at this speed, the VCO itself must operate at four times the REF frequency.

The ability to multiply an input frequency is useful in board-level designs where the distribution of a low-frequency signal is needed to reduce EMI emissions or where a faster clock is needed to increase the operating frequency of state machine logic. *Figure 32* shows how RoboClock can be configured as a frequency multiplier and a phase adjuster. By selecting 3Fn = HH, RoboClock will multiply the

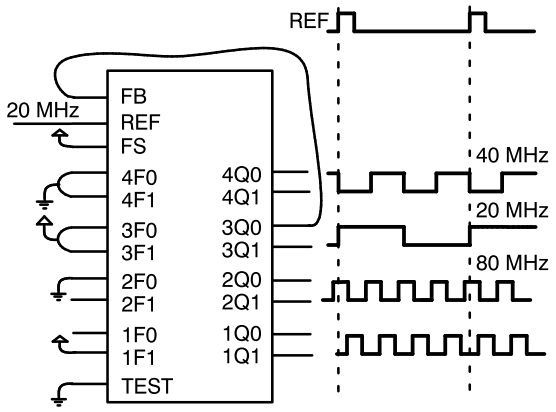

Figure 32. Frequency Multiplier with Phase Adjustment

REF frequency by four, by forcing its PLL to operate at four times the REF clock rate. 4Fn = LL selects the divide-by-two option at the 4Qn outputs. Since the PLL is operating at 80 MHz, the 4Qn outputs will operate at 40 MHz. Selecting 2Fn = ML configures the 2Qn outputs to precede the rising edge of the FB input by 1 time unit. And selecting 1Fn = HM makes the 1Qn outputs arrive 3 time units later than the FB input. Both the 1Qn and 2Qn outputs will run at 80 MHz. The xFn configurations for this example can be found in the shaded area of *Table 6*.

Table 7 appears very similar to *Table 6*. The first part gives the 1Qn and 2Qn output configurations when a 4Qn output is used as the FB input. The second part of the table gives the 3Qn output configurations when a 4Qn output is used as the FB input. The major variation is that if a 4Qn output is used as the FB input with 4Fn = HH, then all outputs will be inverted. Since the PLL phase aligns the REF and FB input, the 4Qn outputs will operate identically with the REF input. The other outputs will have a 180˚phase shift from the REF input. This is useful for applications requiring more inverted clock signals than non-inverted clock signals.

Table 6. 3Qx Output Connected to FB Input (Part 1)

3Qn ⧫ FB		1Qn (2Qn) Output with respect to FB										
		Input Select	1F1, (2F1)	L	L	L	M	M	M	H	H	H
3F1	3F0		1F0, (2F0)	L	M	H	L	M	H	L	M	H
L	L	Output Configuration		−4t f*2	−3t f*2	−2t f*2	−1t f*2	0t f*2	+1t f*2	+2t f*2	+3t f*2	+4t f*2
L	M			+2t	+3t	+4t	+5t	+6t	+7t	+8t	+9t	+10t
L	H			0t	+1t	+2t	+3t	+4t	+5t	+6t	+7t	+8t
M	L			−2t	−1t	0t	+1t	+2t	+3t	+4t	+5t	+6t
M	M			−4t	−3t	−2t	−1t	0t	+1t	+2t	+3t	+4t
M	H			−6t	−5t	−4t	−3t	−2t	−1t	0t	+1t	+2t
H	L			−8t	−7t	−6t	−5t	−4t	−3t	−2t	−1t	0t
H	M			−10t	−9t	−8t	−7t	−6t	−5t	−4t	−3t	−2t
H	H			−4t f*4	−3t f*4	−2t f*4	−1t f*4	0t f*4	+1t f*4	+2t f*4	+3t f*4	+4t f*4

Table 6. 3Qx Output Connected to FB Input (Part 2)

3Qn ⇻ FB		4Qn Output with respect to FB										
		Input Select	4F1	L	L	L	M	M	M	H	H	H
3F1	3F0		4F0	L	M	H	L	M	H	L	M	H
L	L	Output Configuration		0t	−6t f*2	−4t f*2	−2t f*2	0t f*2	+2t f*2	+4t f*2	+6t f*2	INV f*2
L	M			+6t f/2	0t	+2t	+4t	+6t	+8t	+10t	+12t	+6t INV
L	H			+4t f/2	−2t	0t	+2t	+4t	+6t	+8t	+10t	+4t INV
M	L			+2t f/2	−4t	−2t	0t	+2t	+4t	+6t	+8t	+2t INV
M	M			0t f/2	−6t	−4t	−2t	0t	+2t	+4t	+6t	0t INV
M	H			−2t f/2	−8t	−6t	−4t	−2t	0t	+2t	+4t	−2t INV
H	L			−4t f/2	−10t	−8t	−6t	−4t	−2t	0t	+2t	−4t INV
H	M			−6t f/2	−12t	−10t	−8t	−6t	−4t	−2t	0t	−6t INV
H	H			0t f*2	−6t f*4	−4t f*4	−2t f*4	0t f*4	+2t f*4	+4t f*4	+6t f*4	INV f*4

Table 7. 4Qx Output Connected to FB Input (Part 1)

4Qn ⇻ FB		1Qn (2Qn) Output with respect to FB										
		Input Select	1F1, (2F1)	L	L	L	M	M	M	H	H	H
4F1	4F0		1F0, (2F0)	L	M	H	L	M	H	L	M	H
L	L	Output Configuration		−4t f*2	−3t f*2	−2t f*2	−1t f*2	0t f*2	+1t f*2	+2t f*2	+3t f*2	+4t f*2
L	M			+2t	+3t	+4t	+5t	+6t	+7t	+8t	+9t	+10t
L	H			0t	+1t	+2t	+3t	+4t	+5t	+6t	+7t	+8t
M	L			−2t	−1t	0t	+1t	+2t	+3t	+4t	+5t	+6t
M	M			−4t	−3t	−2t	−1t	0t	+1t	+2t	+3t	+4t
M	H			−6t	−5t	−4t	−3t	−2t	−1t	0t	+1t	+2t
H	L			−8t	−7t	−6t	−5t	−4t	−3t	−2t	−1t	0t
H	M			−10t	−9t	−8t	−7t	−6t	−5t	−4t	−3t	−2t
H	H			−4t INV	−3t INV	−2t INV	−1t INV	0t INV	+1t INV	+2t INV	+3t INV	+4t INV

Table 7. 4Qx Output Connected to FB Input (Part 2)

4Qn ⇻ FB		3Qn Output with respect to FB										
		Input Select	3F1	L	L	L	M	M	M	H	H	H
4F1	4F0		3F0	L	M	H	L	M	H	L	M	H
L	L	Output Configuration		0t	−6t f*2	−4t f*2	−2t f*2	0t f*2	+2t f*2	+4t f*2	+6t f*2	0t f/2
L	M			+6t f/2	0t	+2t	+4t	+6t	+8t	+10t	+12t	+6t f/4
L	H			+4t f/2	−2t	0t	+2t	+4t	+6t	+8t	+10t	+4t f/4
M	L			+2t f/2	−4t	−2t	0t	+2t	+4t	+6t	+8t	+2t f/4
M	M			0t f/2	−6t	−4t	−2t	0t	+2t	+4t	+6t	0t f/4
M	H			−2t f/2	−8t	−6t	−4t	−2t	0t	+2t	+4t	−2t f/4
H	L			−4t f/2	−10t	−8t	−6t	−4t	−2t	0t	+2t	−4t f/4
H	M			−6t f/2	−12t	−10t	−8t	−6t	−4t	−2t	0t	−6t f/4
H	H			INV f/2	−6t INV	−4t INV	−2t INV	0t INV	+2t INV	+4t INV	+6t INV	INV f/4

Functional Implementations

Obviously, RoboClock has abilities to solve even the most complex problems. The challenge is to determine how to configure RoboClock to solve these problems. The following examples will give a brief overview of how to configure RoboClock to accomplish various tasks.

Low-Skew Clock Buffer

The easiest way to configure RoboClock is as a low-skew clock buffer, as shown in *Figure 33.* In this type of configuration, all xFn inputs are left open (unconnected) and the FB input can be taken from any output. The REF input waveform is shown with a very unequal duty cycle to illustrate the point that because RoboClock is a PLL-based clock buffer, the duty cycle of the outputs is 50/50 regardless of the duty cycle of the REF input. This feat would be impossible in a non-PLL based device.

If this implementation is used, either the 2Q1 or 3Q0 output is the most convenient choice to be used as the FB input because of their proximity. The shortest wire possible should be used to connect the xQn output to the FB input to avoid stub reflection effects on the actual clock line connected to the

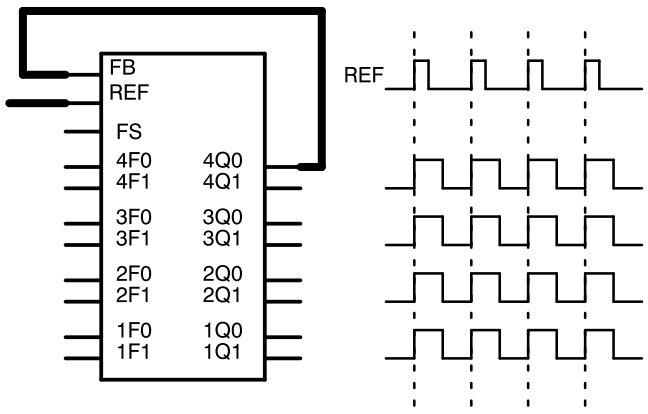

Figure 33. Low-Skew Clock Buffer

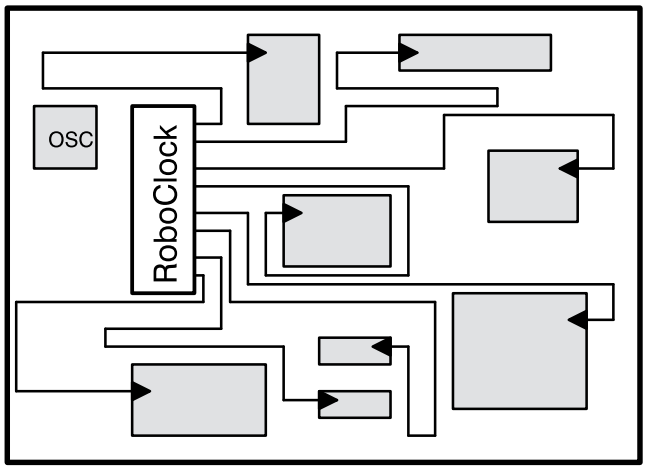

Figure 34. RoboClock in Low Skew Buffer Application

same xQn output *(Figure 2*). This short route will reduce noise and transmission line effects from affecting the FB input.

This configuration assumes that the clock routes to the various loads they are driving are all the same length, so that each of the clocks arrives at its load at virtually the same time. *Figure 34* shows how RoboClock might be used in an application requiring only a device with low output skew.

Programmable Phase Adjustment

This type of application requires the use of RoboClock's additional features. RoboClock provides phase shifting in ranges from −12 time units to +12 time units. *Figure 35* shows RoboClock configured to phase shift its 2Qn outputs so that they lag the FB input, and to phase shift its 1Qn outputs so that they lead the FB input. Any output can be used as the FB input to implement phase shifting, but the greatest unidirectional shift (12 time units) will be achieved by selecting either the 3Qn or 4Qn outputs to be used as the FB input.

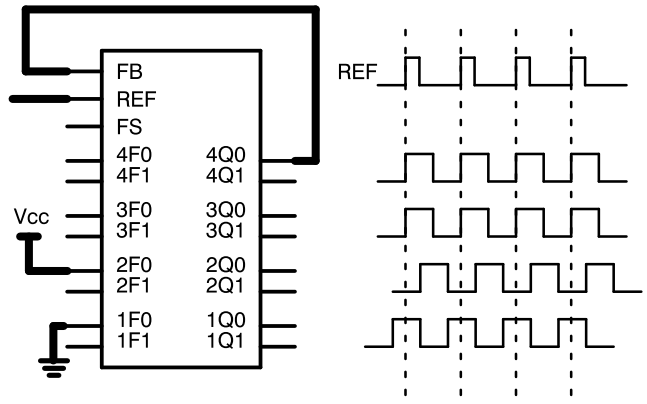

Figure 35. Programmable Phase Adjustment

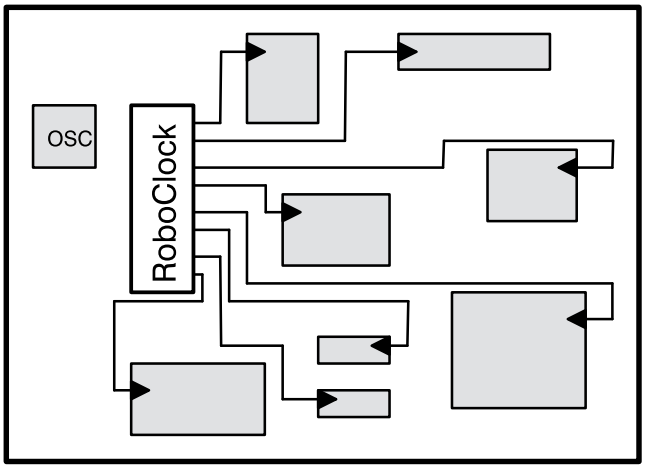

Figure 36. RoboClock in Programmable Phase Adjustment Application

Figure 36 shows RoboClock in a programmable phase adjustment application. This application differs from *Figure 34* in that the sophisticated phase adjustment abilities of RoboClock are used to compensate for trace delays and set-up and hold time mismatches.

Inverted Output Clock Driver

Figure 37 shows RoboClock configured as a inverted output clock driver. 4Fn = HH configures the 4Qn

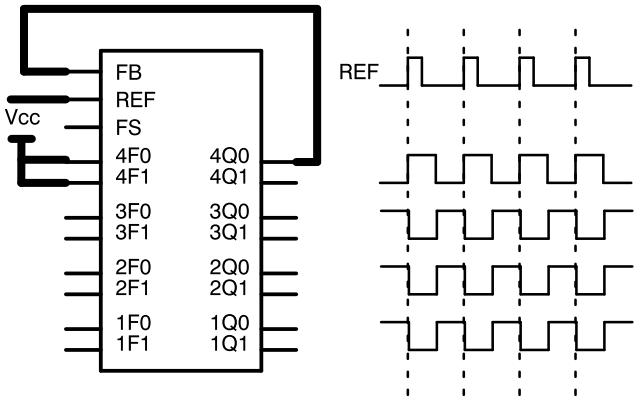

Figure 37. Inverted Output Clock Driver

outputs to operate in inverted mode. If one of these outputs is used as the FB input, then the PLL will align the rising edge of 4Q0 with REF and all of the other outputs operate 180˚ phase shifted from the FB input. This type of configuration is useful for system designs that require a greater number of clocks with 180º phase shift (inverted). These inverted clocks are useful for clocking logic at twice the frequency without distributing a higher frequency clock. In this configuration, RoboClock offers 6 inverted outputs and 2 non-inverted outputs. This configuration also has the advantage that all of the inverted outputs can be phase shifted and the 3Qn outputs can even be configured to divide the REF frequency by two or four while still maintaining phase inversion.

If only two inverted clocks are needed, then any output except the 4Qn outputs can be connected to the FB input. This will allow the 4Qn outputs to be selected for output inversion without affecting the other outputs. If the REF clock is not being used in other parts of the system, both of these two configuration options yield the same net effect.

Frequency Divider

RoboClock provides frequency division while still maintaining very low skew between the various output edges (more on this in the AC Specifications section). *Figure 38* shows RoboClock configured as a frequency divider. Since the PLL is operating at 20 MHz, the FS pin in this configuration is tied to ground indicating the selection of the 15− to 30-MHz operating range. By selecting 4Fn = LL, the 4Qn outputs will divide the FB frequency by two, and by selecting 3Fn = HH, the 3Qn outputs will divide the FB frequency by four.

Any of the 1Qn or 2Qn outputs could have been selected as the FB input with equivalent results. Note again that the divide-by-two and divide-by-four outputs have no coincidental rising edges. This features allows the system designer to use both outputs for multiphase clocking without concern for skew requirements between the rising edges of these two outputs.

Frequency Multiplier

RoboClock provides frequency multiplication by selecting an output configured to divide by two or divide by four as the FB input. *Figure 39* shows RoboClock multiplying up the REF input frequency. The 3Fn function select inputs are both tied to V_{CC}, configuring the 3Qn outputs to divide by four. But because 3Q0 is used as the FB input, the 3Qn outputs operate at the same frequency as the REF input. The RoboClock PLL, therefore, now operates at four times the REF frequency. This is the reason that the FS pin is tied to V_{CC} indicating the selection of the fastest operating frequency range. The selection of FS is based not on the operating frequency of the REF input, but rather on the operating frequency of the VCO. The operating frequency of the VCO is the same frequency as the 1Qn and 2Qn outputs at all times and also the 3Qn and 4Qn outputs when frequency division is not selected.

The 4Fn function select inputs are both tied to ground, which configures the 4Qn output for divide by two mode. Note that this figure looks much the same as *Figure 38* except for the selection of the FS

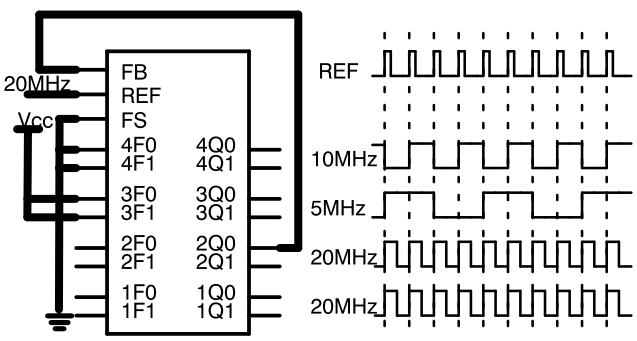

Figure 38. Frequency Divider

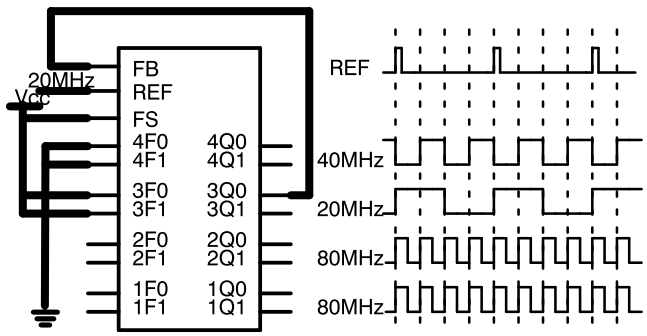

Figure 39. Frequency Multiplier

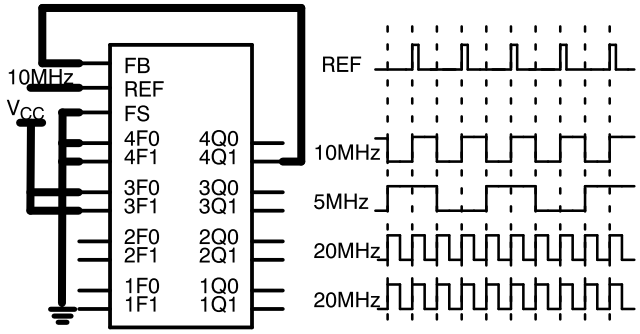

Figure 40. Frequency Divider and Multiplier

input and the selection of the output used as the FB input.

Frequency Divider and Multiplier

Figure 40 illustrates how RoboClock can be used to both multiply and divide the REF frequency. Here the VCO is running at 20MHz. The 4Qn output is used to divide the PLL frequency by two and the 3Qn outputs are used to divide the PLL frequency by four. 4Q1 is used as the FB input doubling the PLL rate.

Multi-Function Clock Driver

RoboClock is truly a multi-function clock driver. It has the ability to multiply up the REF frequency by two or four, divide down the REF frequency by two or four, perform phase inversion, create phase adjustments up to ±12 time units, while always providing very low output skew.

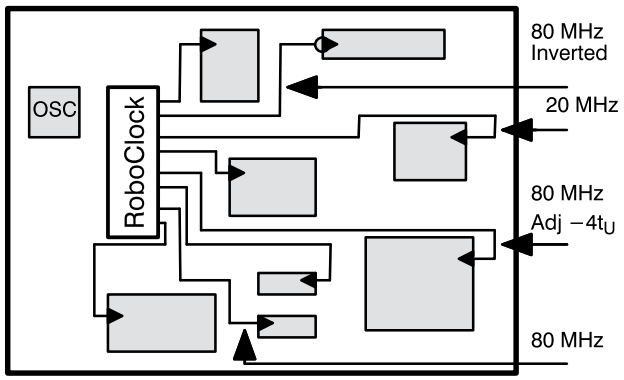

Figure 42. Multi-Function Clock Buffer Application

Figure 41 shows RoboClock configured as a multi-function clock driver. This figure shows how Roboclock can simultaneously multiply the REF frequency by four to a speed of 80 MHz and allow these high-speed outputs to be phase shifted and inverted. *Figure 42* shows how this configuration can be integrated to perform various system clocking functions.

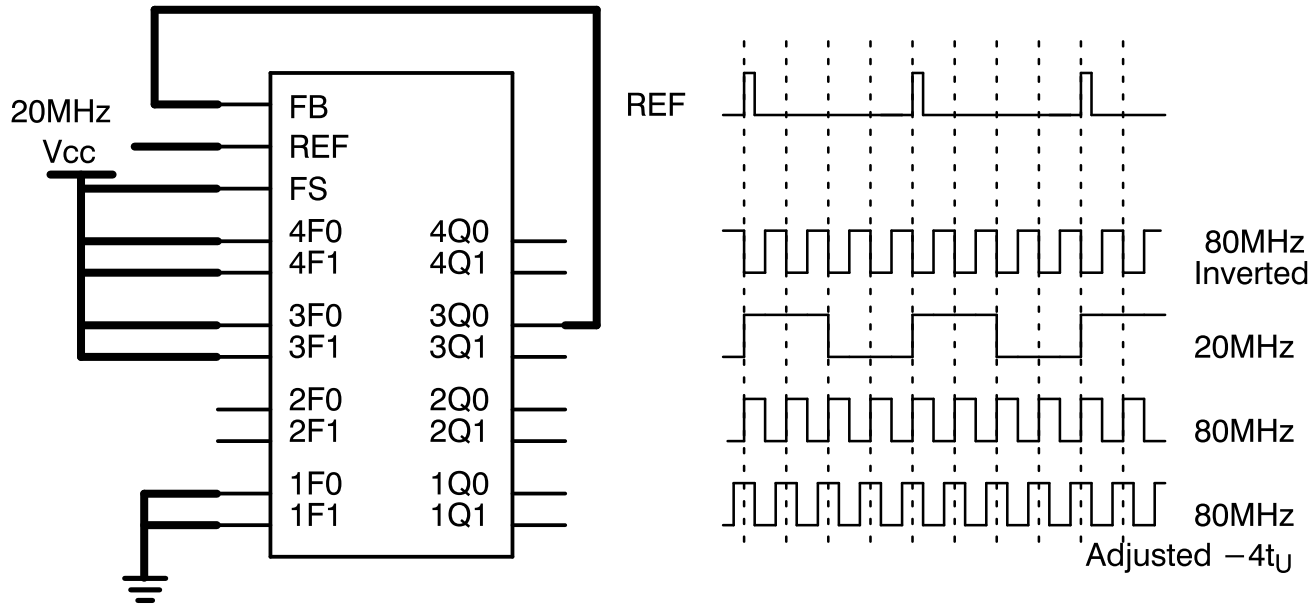

Figure 41. Multi-Function Clock Buffer

Many other examples exist of the tremendous capabilities of RoboClock. External circuitry, for example, can be placed between the RoboClock output and the FB input. This may be the case when RoboClock is used to drive external buffers, frequency dividers, or multipliers. Virtually any delay element can be placed between a RoboClock output and the FB input. A few things, however, must be remembered when doing this:

- The FB input must always be function of one of the RoboClock outputs.
- The other outputs will be referenced to the input of the external device and the delay may not be well defined due to the timing characteristics of the external devices.
- The output edge placement will be dependent on the function and skew characteristics of the external device.
- An external divider of no greater than 16 may be used in the FB path (jitter specifications may be compromised).

AC Specifications

Many AC Specifications exist for RoboClock. The following discussion will explain what these specifications mean to the designer. There are four different parts in the RoboClock family. The CY7B991 is a TTL-output (0 to 3V swing) device and the CY7B992 is a CMOS output (0 to V_{CC} swing) device. The CY7B99x−5 is the lowest skew device that Cypress offers. Its output skew has a typical value of just 250 ps with a maximum skew of 500 ps while the CY7B99x−7 has a maximum output skew of only 750 ps. The following sections will begin with the relevant datasheet specification. Only the CY7B99x−5 specifications will be explained, but all specifications apply directly to the CY7B99x−7 devices except for parameter value. Also, only the CY7B991−5 device will be explained unless the CY7B992−5 device has a different specification.

f_{NOM}: Operating Clock Frequency in MHz

Parameter	Description	CY7B99x			Unit
		Min.	Typ.	Max.	
f_{NOM}	FS = LOW	15		30	ns
	FS = MID	25		50	ns
	FS = HIGH	40		80*	ns

* The maximum operating frequency of the 7B992−7 devices is 50 MHz.

This parameter indicates the frequency range relative to given selections of the FS pin. The three-level FS input can either be tied to ground (LOW), left unconnected (MID), or tied to V_{CC} (HIGH).

The operating frequency these ranges refer to is based on the operating frequency of the VCO. If a divide-by-two output is used as the FB input, then the operating frequency of the VCO is twice that of the REF input. If a divide-by-four output is used as the FB input, then the operating frequency of the VCO is four times that of the REF input. If a non-divided output is used as the FB input then the selection of the FS pin can be made based upon the operating frequency of the REF input.

For example if a divide-by-four output is used as the FB input then the total possible REF input frequency range is 3.75 to 20 MHz (¼*15 to ¼*80 MHz). And the frequency range of the REF input when the FS pin is tied to ground, in particular, is 3.75 to 7.50 MHz.

t_{RPWH}, t_{RPWL} REF Pulse Width High and Low

Parameter	Min.	Typ.	Max.	Unit
t_{RPWH}	5.0			ns
t_{RPWL}	5.0			ns

The frequency and phase detector uses only the rising edge of the REF and FB inputs for alignment purposes. RoboClock, therefore, does not require a 50/50 duty cycle clock. The t_{RPWx} parameter is measured at the 1.5V level.

t_{PD} : Propagation Delay, REF Rise to FB Rise

Parameter	CY7B99x−5			
	Min.	Typ.	Max.	Unit
t_{PD}	− 0.5	0.0	+0.5	ns
Parameter	**CY7B99x−7**			
	Min.	**Typ.**	**Max.**	**Unit**
t_{PD}	− 0.7	0.0	+0.7	ns

Because of the PLL architecture of RoboClock there is no true propagation delay through the device as there is in a device such as a 74F244 buffer. The outputs of RoboClock are independent of the wave shape or duty cycle of the REF input. The PLL uses the REF and FB pins to generate the outputs by aligning these two inputs in both phase and frequency.

This static misalignment (t_{PD} in the datasheet) may be either positive or negative and is a function of the REF frequency. The ±500 ps specification is to accommodate the normal variation in process, voltage, temperature, and frequency. Two parts operating at the same frequency and similar voltage and temperature (approximately ±100 mV and ±10°C) will never have a t_{PD} variation more than 200 ps while the total magnitude of either might be 500 ps). This part-to-part variation appears as t_{SKEW5} in the datasheet and is discussed below. While the PLL aligns the REF and FB pins, some time difference may exist between the REF and FB pin (See *Figure 43*).

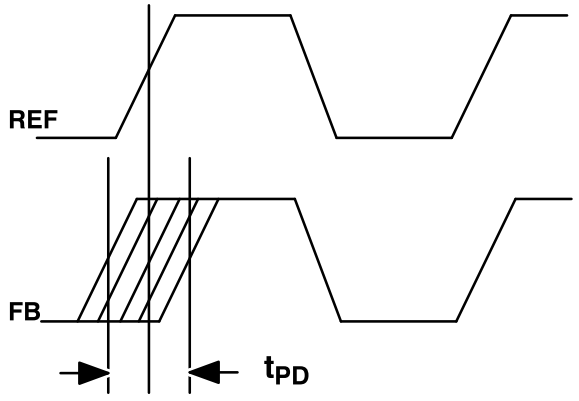

Figure 43. Propagation Delay

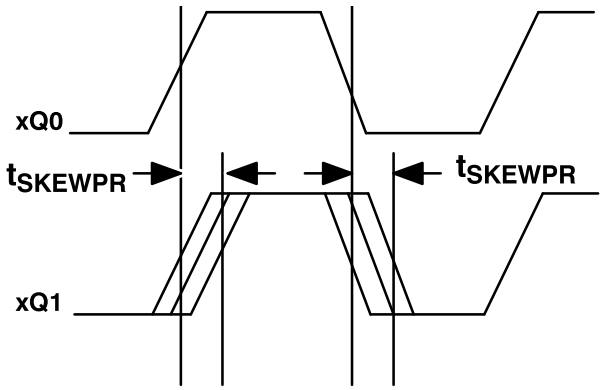

Figure 44. Zero-Output Matched Pair Skew

t_{SKEW} : Output Skew

There are six different parameters specifying output skew. Each of these parameters relates to different output configurations and to different output edges. Each of the following sections will describe the particular skew parameter with a diagram and include an example showing when this parameter would be used to calculate output skew.

t_{SKEWPR} : Zero Output Matched-Pair Skew

Parameter	Min.	Typ.	Max.	Unit
t_{SKEWPR}		0.1	0.25	ns

This parameter specifies the maximum amount of skew between two outputs of the same pair (e.g., 1Q1 and 1Q0) when all output are configured for 0 t_U. This specification has a maximum value of 250 ps. Bench characterization, however, indicates that t_{SKEWPR} is rarely greater than 100 ps. The additional margin is included for tester guard band. The reason that both outputs of the same pair can be so tightly coupled is that each pair has a dedicated power and ground pin, that they lie adjacent to each other allowing them to reinforce each other with crosstalk effects, and that they are separated from adjacent outputs by at least two non-switching pins.

Figure 44 shows that skew is measured from the first output to the last output and that t_{SKEWPR} as well as all other skew parameters pertains to both edges of the output waveform. *Figure 45* shows the 4Qn output pair loaded with the datasheet load. Although it may look like one output waveform, both outputs of the 4Qn pair are displayed. *Figure 46* shows the

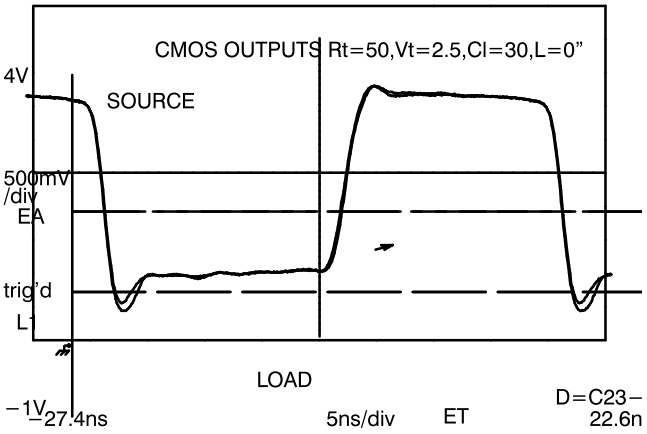

Figure 45. Lumped Load with Datasheet Load

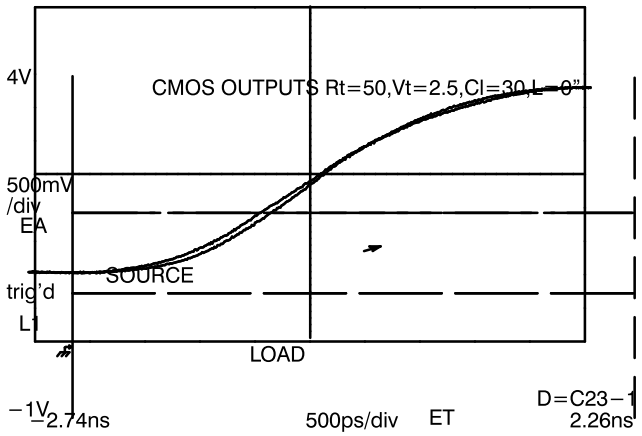

Figure 46. t_{SKEWPR} Measurement

measurement of t_{SKEWPR} with an expanded voltage and time scale as being only 27 ps.

t_{SKEW0} : Zero Output Skew

Parameter	CY7B99x−5 Min.	Typ.	Max.	Unit
t_{SKEW0}		0.25	0.5	ns

Parameter	CY7B99x−7 Min.	Typ.	Max.	Unit
t_{SKEW0}		0.3	0.7	ns

t_{SKEW0} is the maximum skew between the first output edge and the last output edge of all outputs when all outputs are configured for 0 t_U. This specification also applies to outputs that are not adjusted when another output is divided-by-two or divided-by-four. Bench data indicates that these skew values are usually no greater than 350 ps.

For example the skew between any of the outputs in *Figure 33* is no greater than 500 ps. The maximum skew between the 1Qn and 2Qn outputs in *Figure 38* is also 500 ps, even though both the 3Qn and 4Qn outputs are divided. This assumes that a CY7B99x−5 is used to generate these signals.

t_{SKEW1} : Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)

Parameter	CY7B99x−5 Min.	Typ.	Max.	Unit
t_{SKEW1}		0.25	0.5	ns

Parameter	CY7B99x−7 Min.	Typ.	Max.	Unit
t_{SKEW1}		0.3	0.7	ns

t_{SKEW1} is specified as the maximum amount of skew between outputs of the same output class selected for the same output adjustment without restrictions on the placement or function of other outputs. For the purposes of skew specification, there are three types of output classes:

- *Nominal*: Outputs that are selected for phase adjustment, but not inversion, division, or multiplication are of the Nominal output class. This also includes outputs that are not phase adjusted when other outputs have a non 0t_U configuration.
- *Divided*: This class of outputs includes the 3Qn and 4Qn outputs that are configured for divide-by-two or -four mode (3Fn=HH, or LL, and 4Fn = LL). Even when these outputs are configured this way and selected as the FB input, the are still considered to be part of the Divided output class.
- *Inverted*: This class of outputs includes the 4Qn outputs configured in the inverted mode of operation (4Fn = HH). The Inverted output class also applies to a 4Qn output configured for phase inversion and used as the FB input.

This parameter, as in the case of $t_{SKEWPR, 0, and 3}$ applies not only to rising edge to rising edge output skew, but also to falling edge to falling edge skew.

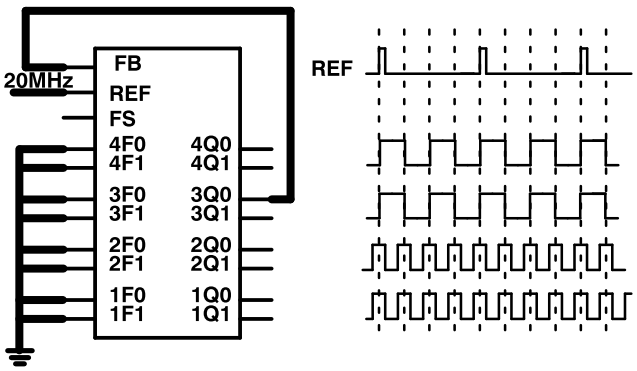

Figure 47. Multi-Function Clock Buffer

Figure 47 illustrates a an example of when to use t_{SKEW1} to calculate output skew. The maximum skew between the 1Qn and 2Qn outputs, when they are selected in this case for −4 time unit adjustment, is no greater than 700 ps. The maximum skew between the 4Qn and 3Qn when both are selected for divide−by−two is also 700 ps.

Figure 48 shows a diagram of an output (Adjusted Q) that has been programmed to occur N time units (t_U) later than another output (Q). The maximum amount of time between these two outputs will be

$$t_{DIFF} = N \times t_U + t_{SKEW1} \quad \text{Eq. 27}$$

and the minimum amount of difference between these two outputs is

$$t_{DIFF} = N \times t_U - t_{SKEW1} \quad \text{Eq. 28}$$

Where N is difference in the calculated tap delays between these two outputs. There is no need to add

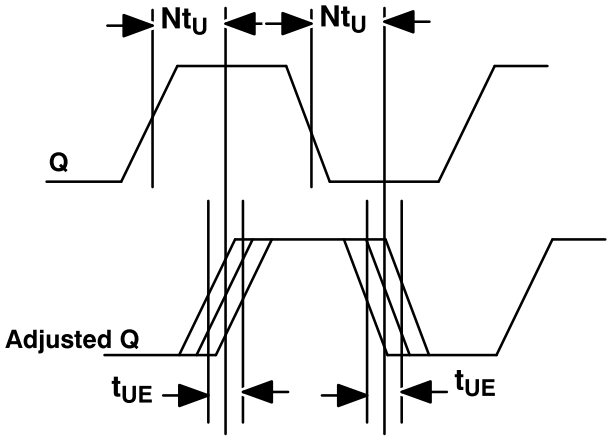

Figure 48. Programmable Adjustment Error

twice the t_{SKEW1} time in order to calculate the minimum and maximum time difference.

For example, the minimum and maximum time between the 1Qn and 2Qn outputs in a system configured as in *Figure 35* using a CY7B991−5 operating at 50 MHz would be

$$t_{DIFF(min)} = 2 * \left(\frac{1}{50 * 10^6 \times 26}\right) - .5 = 1.04\ ns \quad \text{Eq. 29}$$

$$t_{DIFF(max)} = 2 * \left(\frac{1}{50 * 10^6 \times 26}\right) + .5 = 2.04\ ns \quad \text{Eq. 30}$$

The time difference between the 3Qn and 4Qn outputs (which were not phase adjusted) and the 1Qn and 2Qn (which were phase adjusted in opposite directions) would be

$$t_{DIFF(min)} = \left(\frac{1}{50 * 10^6 \times 26}\right) - .5 = .269\ ns \quad \text{Eq. 31}$$

$$t_{DIFF(max)} = \left(\frac{1}{50 * 10^6 \times 26}\right) + .5 = 1.269\ ns \quad \text{Eq. 32}$$

These equations give the worst-case time value between outputs skewed by 1 time unit when operating at 50 MHz. No additional output skew parameters need to be added. The ordering, including skew, between two outputs that are phase adjusted, can always be determined from the functional input selections. This is shown in the above example where the minimum time between two output adjusted by one time unit was determined to be 269 ps.

t_{SKEW2}: Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)

Parameter	CY7B99x−5 Min.	Typ.	Max.	Unit
t_{SKEW2}		0.6	1.2	ns
Parameter	**CY7B99x−7 Min.**	**Typ.**	**Max.**	**Unit**
t_{SKEW2}		1.0	1.5	ns

This skew parameter specifies the amount of output skew between the rising or falling edge of a Nominal output and the opposite edge of an Inverted output as generalized in *Figure 49*. This parameter also applies to opposite edge transitions between Divided outputs.

For example, in *Figure 39,* the output skew between the opposite edge transitions of the the 3Qn and 4Qn outputs selected for divided mode is no greater than 1.2 ns. The magnitude of this number compensates for the different in the rising and falling edge rates.

t_{SKEW3} : Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)

Parameter	CY7B99x-5 Min.	Typ.	Max.	Unit
t_{SKEW3}		0.6	1.0	ns
Parameter	**CY7B99x−7 Min.**	**Typ.**	**Max.**	**Unit**
t_{SKEW3}		0.7	1.2	ns

This output skew parameter specifies the maximum same edge transition difference between different class outputs. In *Figure 39*, the difference between the rising edge of the 4Qn or 3Qn outputs that are configured for divided mode and the rising edge of the 1Qn and 2Qn outputs will be no greater than 1 ns.

t_{SKEW4} : Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)

Parameter	CY7B99x−5 Min.	Typ.	Max.	Unit
t_{SKEW4}		0.6	1.3	ns
Parameter	**CY7B99x−7 Min.**	**Typ.**	**Max.**	**Unit**
t_{SKEW4}		1.2	1.7	ns

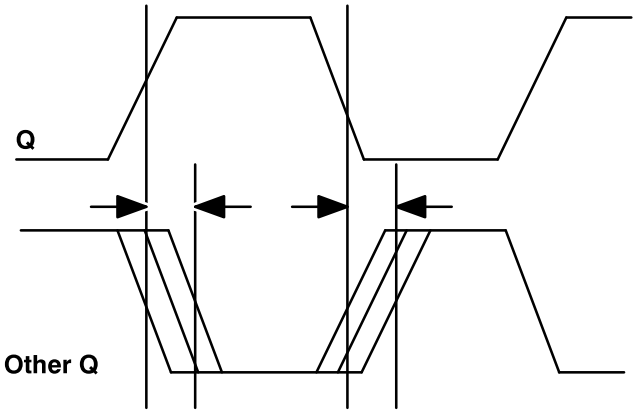

Figure 49. t_{SKEW2} and t_{SKEW4} Measurement

This output skew parameter specifies the maximum opposite edge transition difference between different class outputs as generalized in *Figure 49*. In *Figure 39,* the maximum difference between the opposite edge transition of the 4Qn or 3Qn outputs and the 1Qn and 2Qn outputs would be no greater than 1.3 ns

t_{SKEW5} : Device-to-Device Output Skew

Parameter	CY7B99x Min.	Typ.	Max.	Unit
t_{SKEW5}			0.2	ns

Taken by itself, this parameter has very little meaning in a system design. It must be used in conjunction with the other output skew parameters discussed above. This parameter states that the maximum variation in t_{PD} between two devices operating at the same frequency, temperature, and voltage will be no greater than 200 ps. This means that the device to device skew between two outputs used as the FB input will be no greater than 200 ps under these circumstances.

Figure 50 (an adapted version of *Figure 39*) shows two RoboClock devices configured as in *Figure 39* connected in parallel. To calculate the device to device skew for outputs configured for 0 t_U use the t_{SKEW0} parameter of each device plus t_{SKEW5} as in the following equation:

$$t_{SKEW} = t_{SKEW0(1)} + t_{SKEW0(2)} + t_{SKEW5}$$
$$t_{SKEW} = 0.5 + 0.5 + 0.2 = 1.2\ ns \qquad \text{Eq. 33}$$

This will give the output skew between the 2Qn and 1Qn output skew between devices 1 and 2. To calculate the output skew between the rising edges of the divided outputs and the 0-phase-adjusted outputs, use the following equation:

$$t_{SKEW} = t_{SKEW3(1)} + t_{SKEW3(2)} + t_{SKEW5}$$
$$t_{SKEW} = 1.0 + 1.0 + 0.2 = 2.2ns \qquad \text{Eq. 34}$$

In general, to calculate the skews between two devices, add the relevant skew component from each device and add 200 ps.

Figure 51 gives a slightly more complicated example to illustrate how to calculate device-to-device skew.

Device 3 has been added to the previous example. The outputs of this device are driving the REF inputs of devices 1 and 2. The only additional component to add to the output to output skew for devices 1 and 2 is the output-to-output skew of device 3. The part-to-part skew between devices 1 and 2 for outputs that are left unconfigured (1Qn and 2Qn) is now

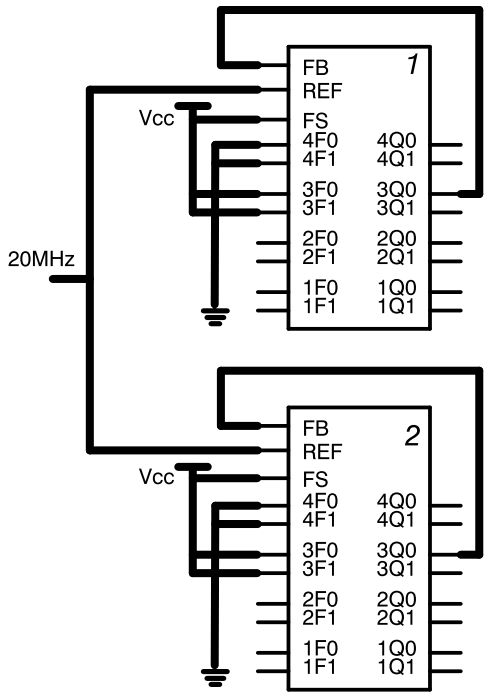

Figure 50. Part-to-Part Skew Example

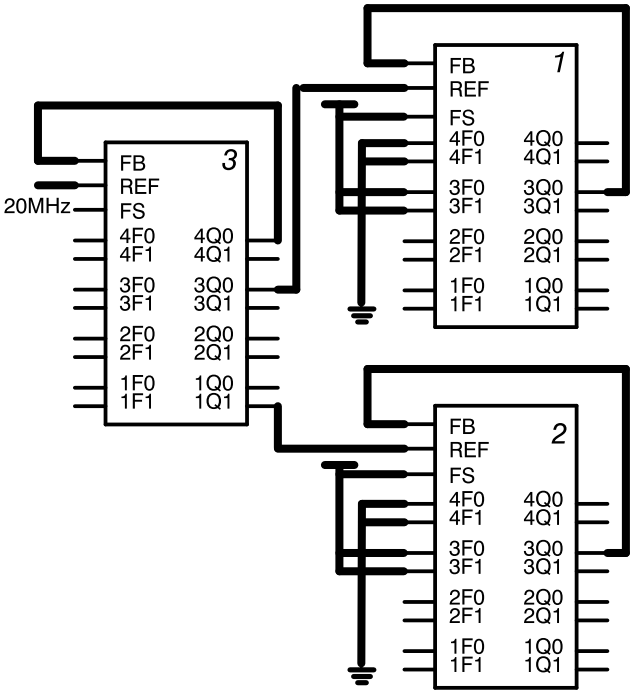

Figure 51. Devices in Parallel and Serial

$$t_{SKEW} = t_{SKEW0(3)} + t_{SKEW1(1)} + t_{SKEW1(2)} + t_{SKEW5}$$
$$t_{SKEW} = 0.5 + 0.5 + 0.5 + 0.2 = 1.7ns \quad \text{Eq. 35}$$

t_{ODCV} : Output Duty Cycle Variation

Parameter	CY7B99x−5 Min.	Typ.	Max.	Unit
t_{ODCV}	− 1.0	0.0	+1.0	ns

Parameter	CY7B99x−5 Min.	Typ.	Max.	Unit
t_{ODCV}	− 1.2	0.0	+1.2	ns

This parameter specifies the difference in the output duty cycle from 50%. It is measured at 1.5V. This parameter indicates, for example, that the outputs of the CY7B99x−5 have a worst-case duty cycle of 42/58, and at 15 MHz the duty cycle is 48.5/51.5 worst case. The AC Characterization section contains data on how the value of this parameter varies with loading, voltage, and temperature.

t_{ORISE}, t_{OFALL} : Output Rise and Fall Time

Parameter	CY7B991−5 Min.	Typ.	Max.	Unit
t_{ORISE}	0.15	1.0	1.5	ns
t_{OFALL}	0.15	1.0	1.5	ns

Parameter	CY7B992−5 Min.	Typ.	Max.	Unit
t_{ORISE}	0.5	2.0	2.5	ns
t_{OFALL}	0.5	2.0	2.5	ns

Parameter	CY7B991−7 Min.	Typ.	Max.	Unit
t_{ORISE}	0.15	1.5	2.5	ns
t_{OFALL}	0.15	1.5	2.5	ns

Parameter	CY7B992−7 Min.	Typ.	Max.	Unit
t_{ORISE}	0.5	3.0	5.0	ns
t_{OFALL}	0.5	3.0	5.0	ns

The output rise and fall time are measured with different loads for each of the four devices. The

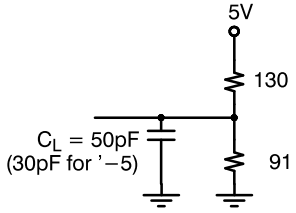

Figure 52. TTL AC Test Load

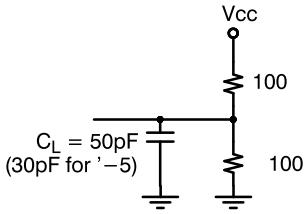

Figure 53. CMOS AC Test Load

CY7B991 devices (TTL) are tested with the load shown in *Figure 52*. The 130Ω over 91Ω load is the recommended parallel termination for 50Ω transmission lines. For the −7 devices a 50-pF load is used to test all AC parameters for the −5 devices a 30-pF load is used. *Figure 53* shows the CMOS device test load (CY7B992).

The TTL and CMOS devices are also measured between different voltage levels. *Figure 54* shows that the TTL rise and fall time parameters are measured between 0.8 and 2.0V, and *Figure 55* shows that the

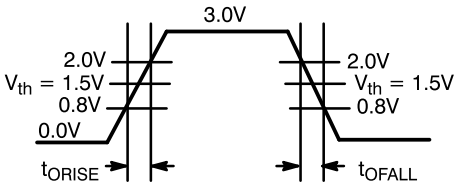

Figure 54. TTL Output Voltage Levels

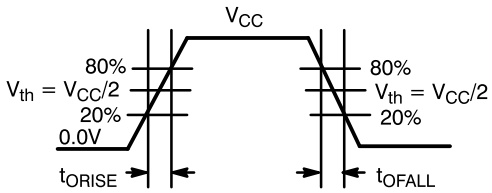

Figure 55. CMOS Output Voltage Levels

CMOS rise and fall times are measured between 20% and 80% of V_{CC}.

The outputs edge rates of these devices are controlled to about 1 V/ns to minimize the generation of system noise and transmission line effects. The AC Characterization section will give examples of how this parameter varies with loading, voltage, and temperature.

t_{PWH}, t_{PWL} : Output High and Low Time Deviation from 50%

Parameter	CY7B991−5 Min.	CY7B991−5 Typ.	CY7B991−5 Max.	Unit
t_{PWH}			2.5	ns
t_{PWL}			3	ns
Parameter	**CY7B992−5 Min.**	**CY7B992−5 Typ.**	**CY7B992−5 Max.**	**Unit**
t_{PWH}			3.5	ns
t_{PWL}			3.5	ns
Parameter	**CY7B991−7 Min.**	**CY7B991−7 Typ.**	**CY7B991−7 Max.**	**Unit**
t_{PWH}			3	ns
t_{PWL}			3.5	ns
Parameter	**CY7B992−7 Min.**	**CY7B992−7 Typ.**	**CY7B992−7 Max.**	**Unit**
t_{PWH}			5.5	ns
t_{PWL}			5.5	ns

The output pulse width high and low times are specified as deviations from an ideal 50/50 duty cycle. t_{PWH} is measured above the 2.0V (80% V_{CC}) for the TTL (CMOS) devices and t_{PWL} is measured below 0.8V (20% V_{CC}) for the TTL (CMOS) devices. The value of these parameters can be calculated from the combination of the t_{ODCV} parameter and the t_{ORISE} and t_{OFALL} parameters. The specifications can be calculated as follows

$$t_{PWH} = 2 * t_{OR/OF} * \left(\frac{V_{MAX} - V_{TH}}{V_{MAX} - V_{MIN}}\right) + t_{ODCV} \quad \text{Eq. 36}$$

$$t_{PWL} = 2 * t_{OR/OF} * \left(\frac{V_{TH} - V_{MIN}}{V_{MAX} - V_{MIN}}\right) + t_{ODCV} \quad \text{Eq. 37}$$

Where t_{OROF} represents either the rise time or fall time of the output since they are equal, V_{TH} represents the measurement threshold (TTL = 1.5V and CMOS = $V_{CC}/2$), V_{MAX} represents the maximum voltage point of rise and fall time measurements and V_{MIN} represents the minimum voltage point for rise and fall time measurements.

AC Characterization

Included with this application note are output rise time, output fall time, and output duty cycle variation versus temperature, voltage, capacitive loading, and termination voltage.

Output Rise Time

As explained previously, output rise time (t_{ORISE}) is the maximum amount of time it takes the output to rise from the 0.8V to the 2.0V level.

Figure 56 shows the variation in output rise time based on capacitive loading. This graph can be used to calculate the skew caused by the unequal loading of outputs.

Figure 57 shows the output rise time versus voltage over temperature. Within the normal operating limits of RoboClock (4.5 to 5.5V), the output rise time varies very little with respect to temperature. This means that, within a normal board environment, output rise time will not significantly vary due to minor variations in temperature or voltage.

Figure 58 shows the output rise time vs. termination voltage. In the section entitled Transmission Line Termination the parallel termination Thevenin voltage was specified as 2.06V for the CY7B991−x devices. This figure shows that because output rise time does not vary with termination voltage, convenient resistor value can be chosen that maintain $R_{TH} = Z_0$ within the limits of $1.5V < V_{TH} < 2.5V$.

Output Fall Time

Output fall time is the amount of time it takes for the output to swing from 2.0V to 0.8V.

Figure 59 shows the variation in output fall time with load capacitance. *Figure 60* shows the output fall time vs. chip voltage at various temperatures. Notice that there is almost no variation in output fall time due to changes in device temperature. *Figure 61* shows the output fall time vs. termination voltage.

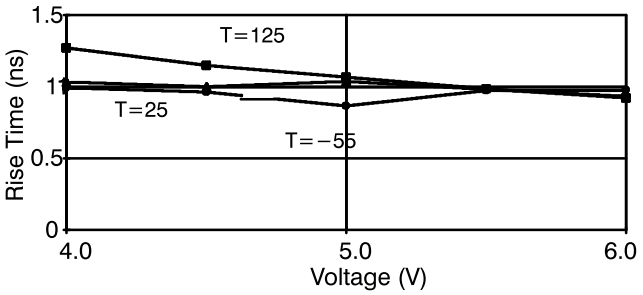

Figure 57. Rise Time vs. Voltage over Temperature

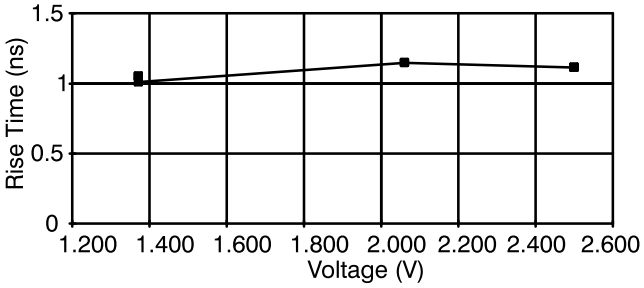

Figure 58. Rise Time vs. Termination Voltage

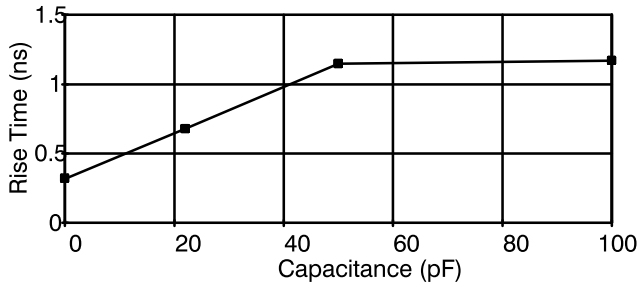

Figure 56. Rise Time vs. Capacitance

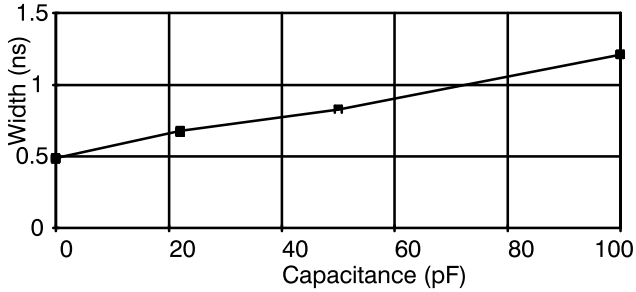

Figure 59. Fall Time vs. Capacitance

Output Duty Cycle Variation

Output duty cycle variation is the difference in the output pulse width from the ideal 50%. This parameter is measured at the 1.5V level. Characterization of this parameter was performed by measuring the output pulse width high. Measurements were taken at two different REF input cycle times (Tref): 50 ns and 12 ns.

Figure 62 and *Figure 63* show the variation in output duty cycle due to variations in output capacitance.

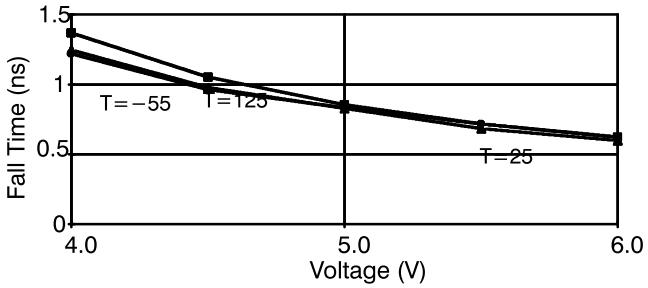

Figure 60. Fall Time vs. Voltage over Temperature

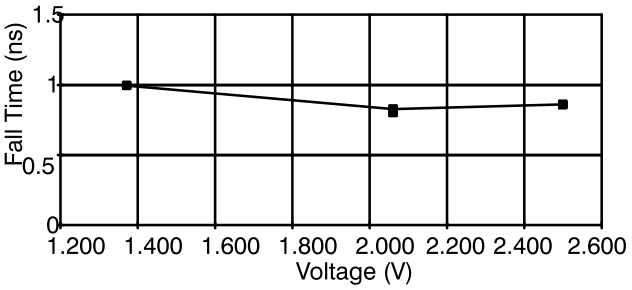

Figure 61. Fall Time vs. Termination Voltage

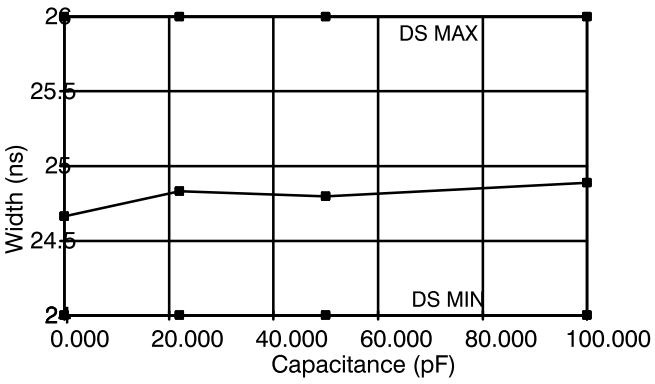

Figure 62. Pulse Width High vs. Capacitance t_{REF} = 50ns

These graphs indicate that if the outputs are loaded according to the datasheet specification, the output duty cycle will be very near 50%.

Figure 64 and *Figure 65* show the output pulse width high vs. device voltage over temperature. These graphs indicate that the propagation delay difference between the rising and falling edge of the outputs varies according to frequency. For operation within the ±10% V_{CC} and the commercial temperature range, the output duty cycle specification is ±500 ps.

Figure 66 and *Figure 67* show the output pulse width high vs. termination voltage. Both of these graphs indicate that with normal variance in termination

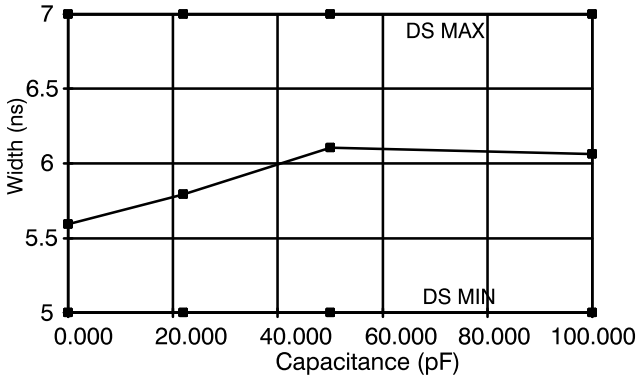

Figure 63. Pulse Width High vs. Capacitance t_{REF} = 12ns

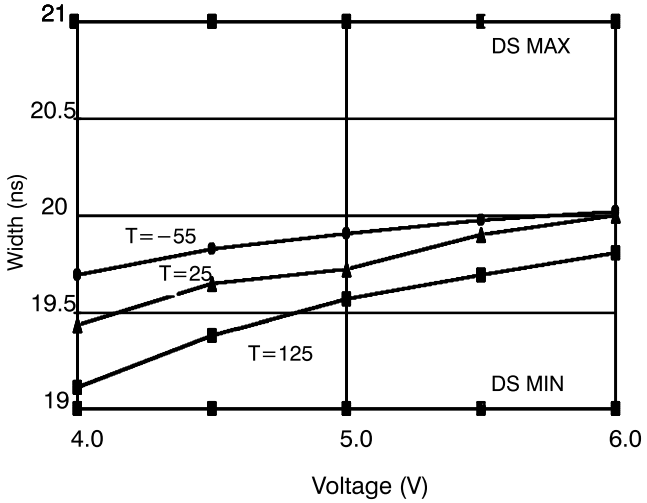

Figure 64. Pulse Width High vs. Voltage over Temperature

voltage the output duty cycle specification remains within the ±500 ps range.

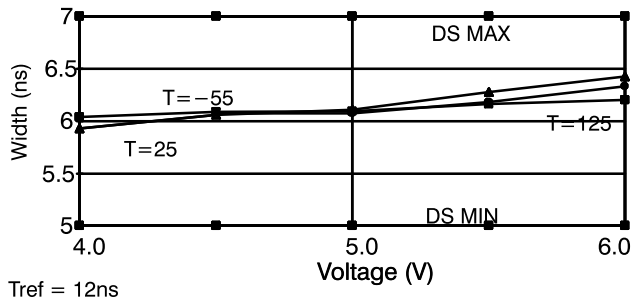

Figure 65. Pulse Width High vs. Voltage over Temperature

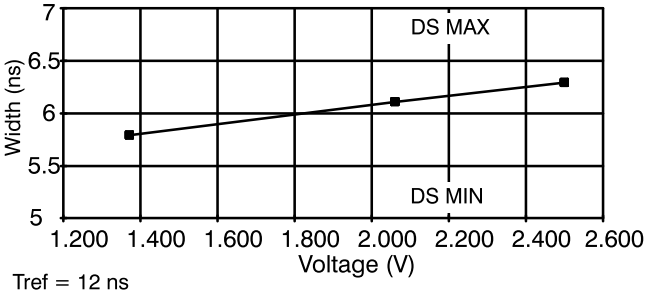

Figure 66. Pulse Width High vs. Termination Voltage

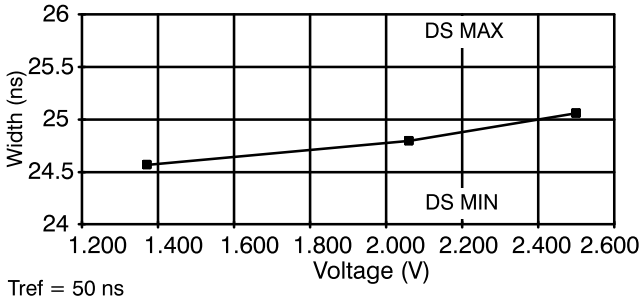

Figure 67. Pulse Width High vs. Termination Voltage

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Conclusion

RoboClock provides system designers with a multi-functional resource that solves most clock distribution problems. The third-generation PLL architecture based on a distributed phase clock oscillator allows phase shifting, division, multiplication and inversion of outputs with over 26,000 possible output configurations. These features combine to offer compensation for trace-length differences, elimination of set-up and hold time mismatches, multiplication of lower-frequency system clocks, division of system clocks for lower-performance system components, and phase inversion for multiphase clocking. All of these benefits are combined with extremely low skew outputs, low device propagation delay, and high-frequency operation to provide the most full-featured device available.

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