Understanding the CY2254

Introduction

The CY2254 is a two-PLL clock generator for the Intel Triton™ chipset-based motherboard and other Pentium™ motherboards. It features four high-drive outputs at the CPU clock frequency (50, 60, or 66.66 MHz, selected by two pins), six high-drive synchronous PCI clock outputs at half the frequency of the CPU clocks, two high-drive Reference outputs at 14.318 MHz, a 12-MHz Keyboard clock output, and a 24-MHz Floppy clock output. This application note discusses the internal architecture of the CY2254, and provides recommendations for using it in a system.

CY2254 Features

The logic block diagram of the CY2254 is shown in *Figure 1*. The device accepts input from a 14.318-MHz parallel-resonant crystal. This signal is then fed to the two internal PLLs, which generate the required frequencies on the outputs. All clock outputs are controlled by an active-HIGH Output Enable pin, which three-states the outputs when

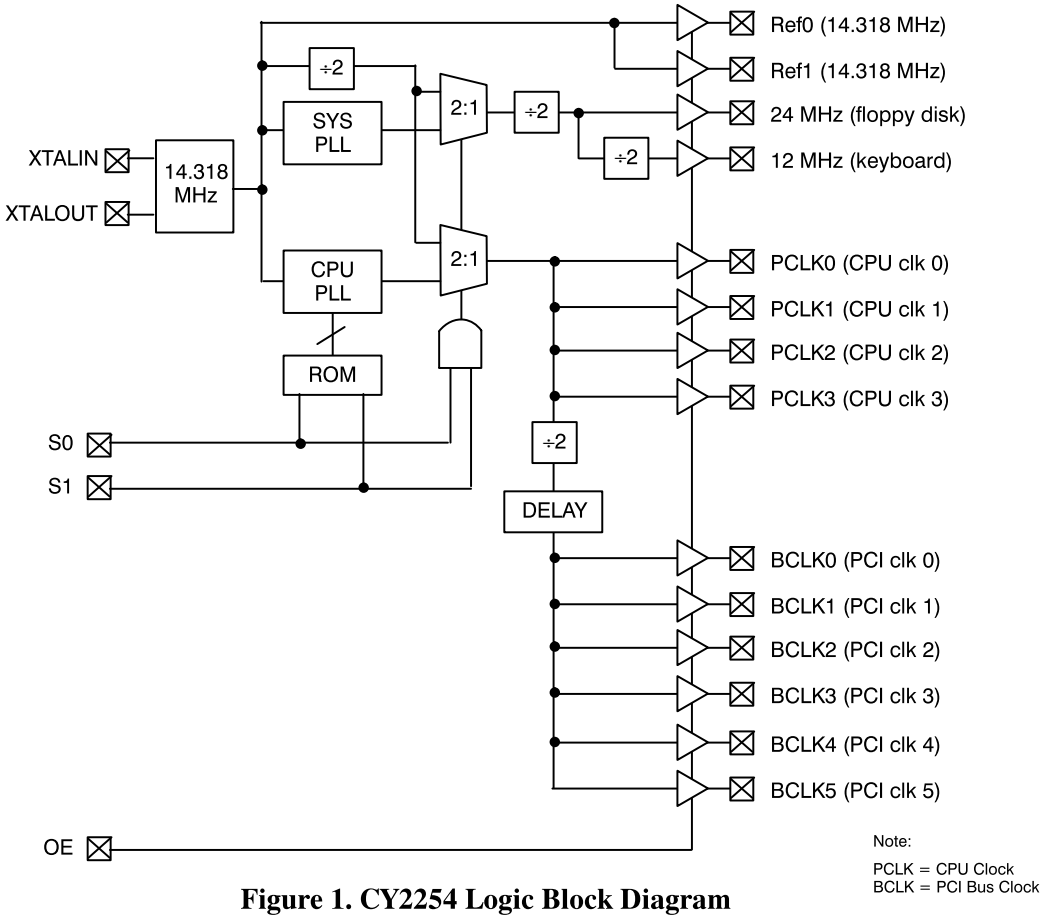

Figure 1. CY2254 Logic Block Diagram

deasserted. *Table 1* shows the CY2254 function table.

CPU Clock Outputs

The CY2254 CPU PLL generates four outputs at the CPU clock frequencies of 50, 60 or 66.66 MHz, by applying appropriate levels on the select inputs, S0 and S1. All CPU clock outputs meet the Pentium's maximum cycle-cycle jitter specification of 200 ps. Finally, all CPU clock outputs are skew-controlled, with a maximum skew of 250 ps between them.

PCI Clock Outputs

The CPU PLL output, after being internally divided by two, drives six outputs at one-half the CPU clock frequency. In addition, these PCI clock outputs lag the CPU clock outputs by 1 to 5 ns. Finally, all PCI clocks outputs are skew-controlled, with a maximum skew of 500 ps between them.

Both CPU and PCI clock outputs feature:

- Matched impedances on the rising and falling edges of output drivers resulting in equal rise and fall times
- Low output impedance: 25Ω (typical) and 40Ω (maximum), measured at 1.5V
- Max. Load on CPU clock = 20 pF
- Max. Load on PCI clock = 30 pF

Reference Clock Outputs

The CY2254 buffers two clock outputs at the reference frequency of 14.318 MHz. The REF0 output has a larger drive capability of 30 pF, as compared to the REF1 drive capability of 15 pF.

Keyboard and Floppy Clocks

The SYS PLL generates the Keyboard and Floppy clocks at 12 and 24 MHz respectively. Both these outputs are capable of driving 20-pF loads, with low jitter.

Test Mode Support

The CY2254 supports the Triton Test mode when both S1 and S0 are set to a logic HIGH. In this mode, reference frequency (TCLK), applied to the XTALIN input, is buffered onto the REF0 and REF1 outputs. The CY2254 also generates TCLK/2, TCLK/4, TCLK/4, TCLK/8 frequencies on the CPU, PCI, Floppy, and Keyboard clock outputs respectively.

Power Supply

The CY2254 requires a clean and accurate 3.3-Volt (±5%) power supply for proper operation.

Reference Frequency

Cypress recommends the use of a parallel-resonant 14.318-MHz crystal to generate the most accurate clock outputs. A series-resonant crystal will result in clock outputs of a slightly higher frequency (appx. 5%).

System Applications

The CY2254 was primarily designed to meet the clock requirements of the Intel Triton chipset. However, since it is a Pentium-compatible device, it can be used in any motherboard requiring high-drive CPU and PCI clock outputs.

Table 1. CY2254 Function Table

OE	S0	S1	XTALIN Input	PCLK	BCLK	Ref. Clock Output	24 MHz	12 MHz
0	X	X	14.318 MHz	High-Z	High-Z	High-Z	High-Z	High-Z
1	0	0	14.318 MHz	50 MHz	PCLK/2	14.318 MHz	24 MHz	12 MHz
1	0	1	14.318 MHz	60 MHz	PCLK/2	14.318 MHz	24 MHz	12 MHz
1	1	0	14.318 MHz	66 MHz	PCLK/2	14.318 MHz	24 MHz	12 MHz
1	1	1	TCLK	TCLK/2	TCLK/4	TCLK	TCLK/4	TCLK/8

The CY2254 will provide accurate, low-jitter clocks on its output. To ensure the quality of the clock outputs, a noise-free power supply is necessary. Additionally, the user should follow the high-speed design techniques summarized in the following sections to ensure reliable operation of the CY2254 and the board. For more details on these techniques, please refer to the Application Notes, "System Design Considerations" and "Protection, Decoupling, and Filtering of Cypress CMOS Circuits," both of which are available in the latest edition of the Cypress Applications Handbook. Please contact your local Cypress representative for a copy.

Supply Bypass and Filtering

To ensure low jitter on the outputs of the CY2254, the designer must provide a clean source of power. A large tantalum capacitor (10−1000 µF) *attached to the board power supply*, will prevent a fall in voltage caused by current surges, as well as reduce power supply ripple. Attach this capacitor as close as possible to where the V_{dd} and GND signals enter the PCB.

This large capacitor will, however, be ineffective at very high frequencies. Hence, a small capacitor, 0.1 µF, will be required to filter high-frequency noise. Cypress recommends attaching a 0.1-µF ceramic capacitor *on every V_{dd} pin* of the CY2254. These capacitors must be attached as close to the pins as is physically possible. Surface mount capacitors are preferred because they have lower lead inductance.

Figure 2 shows the external capacitor connections.

Series Terminations

If the output of the CY2254 drives multiple loads or long traces, use a terminating resistor in series with the output, attached as close to the output pin as is possible. *Figure 2* shows a 22Ω resistor in series with the output. The value of this resistor, summed with the output impedance of the CY2254, should equal the characteristic impedance of the trace (transmission line). Typical values of the series resistor range from 10Ω to 75Ω.

A resistor in series with the output dampens the voltage reflections which occur with output impedance mismatches. It has the ultimate effect of reducing jitter on the output of the CY2254. Once again, surface mount resistors are preferred because of their lower lead inductance.

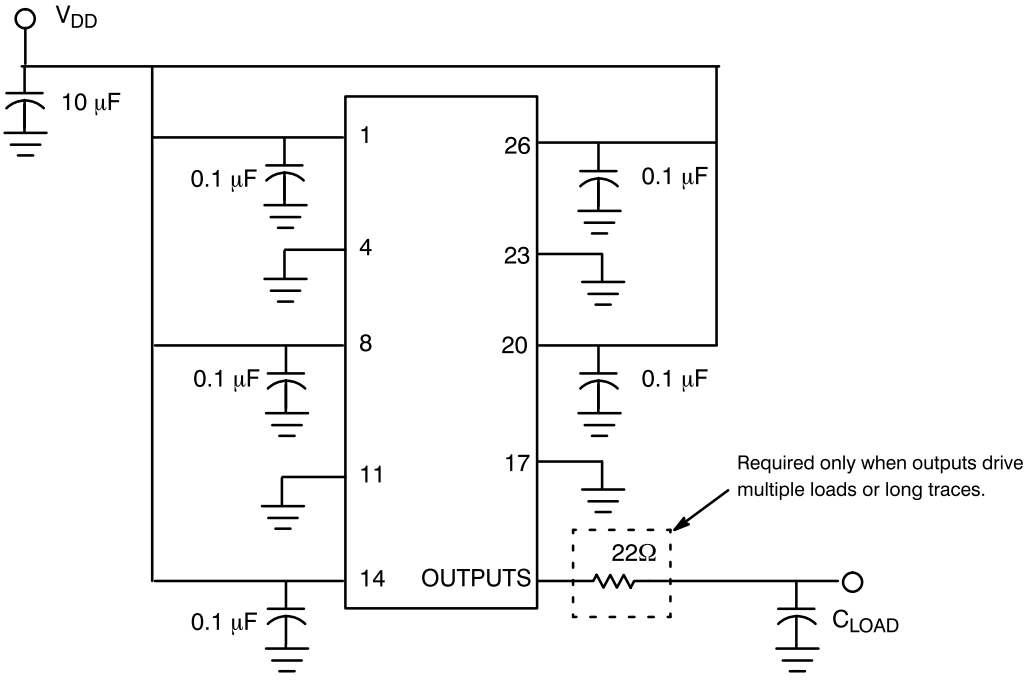

Figure 2. External Connections of the CY2254

Layout Guidelines

The following guidelines apply for laying out the CY2254 on a board:

- Provide a large ground plane under the CY2254. This will have the effect of reducing ground bounce in the system, thus reducing jitter.
- Connect each V_{SS} pin of the CY2254 to the ground plane individually. Connecting them together, and then to the plane will defeat the purpose of providing multiple ground pins.
- Avoid routing any high-frequency or clock signals below the CY2254, and place it in a relatively quiet area of the board. This will eliminate the coupling of any noise into the PLL, and will ensure lower jitter on the outputs.

All the above recommendations, along with a stable power supply source, will result in significantly reduced jitter on the clock outputs of the CY2254.

Conclusion

This application note introduced the reader to the CY2254 and presented some guidelines on using the device in systems. A summary of power supply filtering, termination, and layout guidelines was presented. With this information, the reader should be better able to design with the CY2254.