



CYPRESS

PRELIMINARY

CY7C375i

UltraLogic™ 128-Macrocell Flash CPLD

Features

- 128 macrocells in eight logic blocks
- 128 I/O pins
- 5 dedicated inputs including 4 clock pins
- In-System Reprogrammable (ISR™) Flash technology
 - JTAG interface
- Bus Hold capabilities on all I/Os and dedicated inputs
- No hidden delays
- High speed
 - $f_{MAX} = 100$ MHz
 - $t_{PD} = 12$ ns
 - $t_S = 6$ ns
 - $t_{CO} = 7$ ns
- Fully PCI compliant
- Available in 160-pin TQFP, CQFP, and PGA packages

Functional Description

The CY7C375i is an In-System Reprogrammable Complex Programmable Logic

Device (CPLD) and is part of the FLASH370i™ family of high-density, high-speed CPLDs. Like all members of the FLASH370i family, the CY7C375i is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

Like all of the UltraLogic FLASH370i devices, the CY7C375i is electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows thereby reducing costs. The Cypress ISR function is implemented through a 4-pin serial interface. Data is shifted in and out through the SDI and SDO pins. The ISR interface is enabled using the programming voltage pin (V_{PP}). Additionally, because of the superior routability of the FLASH370i devices, ISR often allows users to change existing logic designs while simultaneously fixing pinout assignments.

The 128 macrocells in the CY7C375i are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x

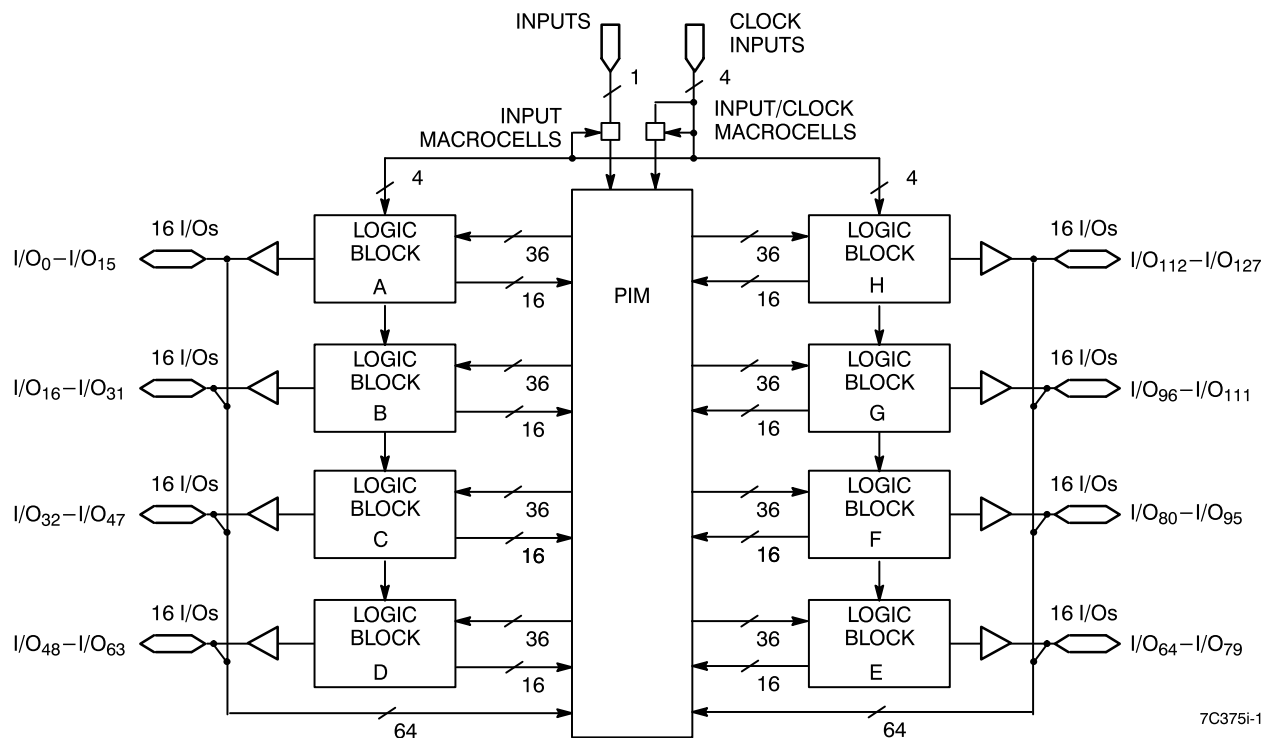
86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370i architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370i family, the CY7C375i is rich in I/O resources. Every macrocell in the device features an associated I/O pin, resulting in 128 I/O pins on the CY7C375i. In addition, there is one dedicated input and four input/clock pins.

Finally, the CY7C375i features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C375i remain the same.

Logic Block Diagram

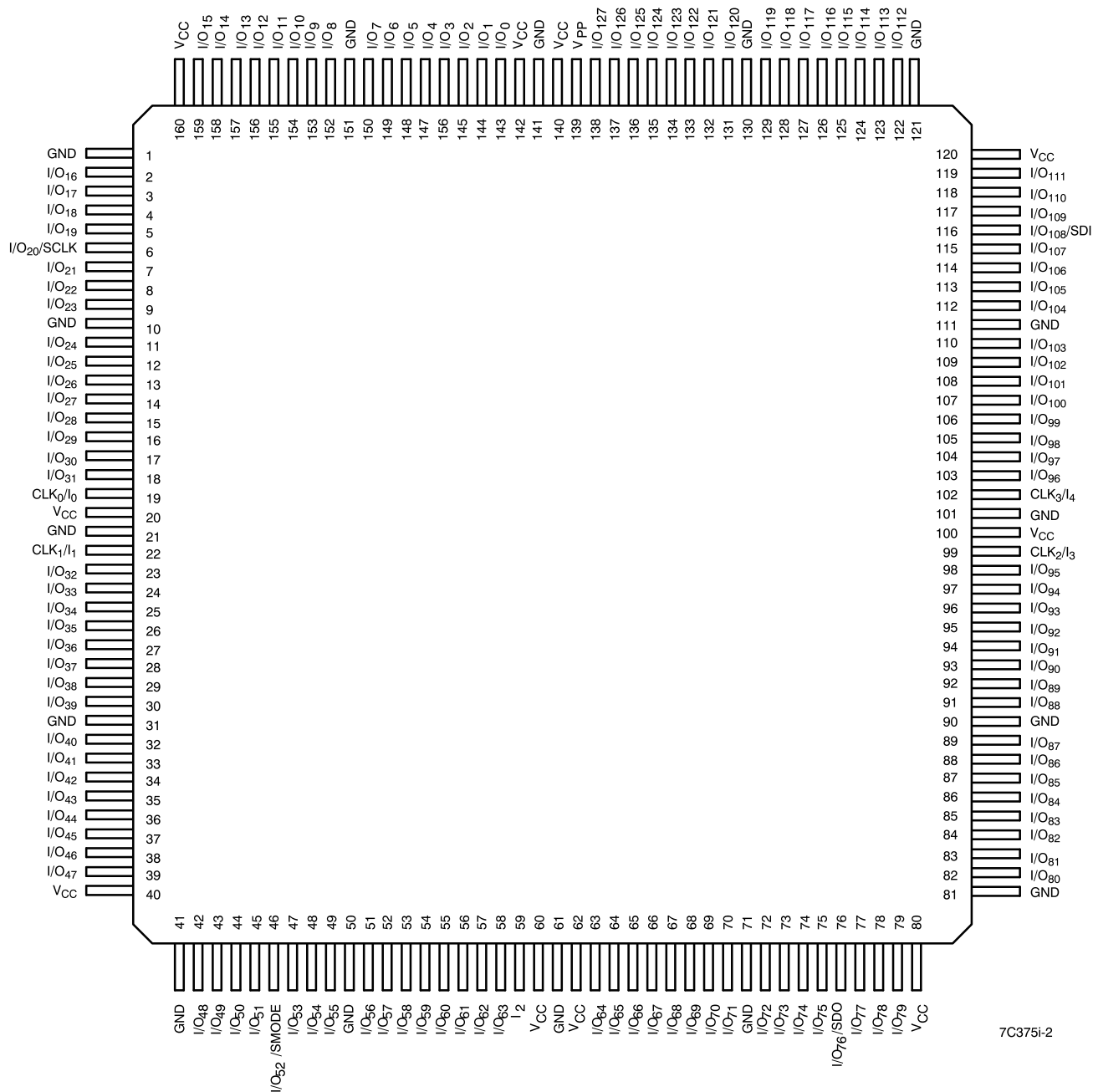


Selection Guide

		7C375i-100	7C375i-83	7C375i-66	7C375iL-66
Maximum Propagation Delay, t_{PD} (ns)		12	15	20	20
Minimum Set-Up, t_S (ns)		6	8	10	10
Maximum Clock to Output, t_{CO} (ns)		7	8	10	10
Maximum Supply Current, I_{CC} (mA)	Commercial	330	300	300	150
	Military/Industrial		370	370	

Pin Configurations

**Top View
TQFP/CQFP**



7C375i-2

Pin Configurations (continued)
**PGA
Bottom View**

R	I/O ₁₀₉	I/O ₁₁₂	I/O ₁₁₅	I/O ₁₁₈	I/O ₁₂₁	I/O ₁₂₃	I/O ₁₂₆	I/O ₁₂₇	I/O ₀	I/O ₃	I/O ₅	I/O ₇	I/O ₁₀	I/O ₁₁	I/O ₁₄
P	I/O ₁₀₆	I/O ₁₁₀	I/O ₁₁₃	I/O ₁₁₆	I/O ₁₁₉	I/O ₁₂₂	I/O ₁₂₅	GND	I/O ₁	I/O ₄	I/O ₆	I/O ₉	I/O ₁₃	I/O ₁₅	I/O ₁₆
N	I/O ₁₀₅	I/O ₁₀₈ /SDI	I/O ₁₁₁	I/O ₁₁₄	I/O ₁₁₇	I/O ₁₂₀	I/O ₁₂₄	V _{PP}	I/O ₂	GND	I/O ₈	I/O ₁₂	GND	I/O ₁₇	I/O ₁₉
M	I/O ₁₀₂	I/O ₁₀₄	I/O ₁₀₇	V _{CC}			V _{CC}	GND	V _{CC}			GND	I/O ₁₈	I/O ₂₀ /SCLK	I/O ₂₂
L	I/O ₁₀₀	I/O ₁₀₁	I/O ₁₀₃										I/O ₂₁	I/O ₂₃	I/O ₂₅
K	I/O ₉₈	I/O ₉₉	GND										I/O ₂₄	I/O ₂₆	I/O ₂₇
J	I/O ₉₆	I/O ₉₇	CLK3 /I ₄	V _{CC}								V _{CC}	I/O ₂₈	I/O ₂₉	I/O ₃₀
H	I/O ₉₅	GND	CLK2 /I ₃	GND								GND	CLK0 /I ₀	GND	I/O ₃₁
G	I/O ₉₄	I/O ₉₃	I/O ₉₂	V _{CC}								V _{CC}	CLK1 /I ₁	I/O ₃₃	I/O ₃₂
F	I/O ₉₁	I/O ₉₀	I/O ₈₈										GND	I/O ₃₅	I/O ₃₄
E	I/O ₈₉	I/O ₈₇	I/O ₈₅										I/O ₃₉	I/O ₃₇	I/O ₃₆
D	I/O ₈₆	I/O ₈₄	I/O ₈₂	GND			V _{CC}	GND	V _{CC}			V _{CC}	I/O ₄₃	I/O ₄₀	I/O ₃₈
C	I/O ₈₃	I/O ₈₁	GND	I/O ₇₈ /SDO	I/O ₇₂	GND	I/O ₆₆	I ₂	I/O ₆₀	I/O ₅₆	I/O ₅₃	I/O ₅₀	I/O ₄₇	I/O ₄₄	I/O ₄₁
B	I/O ₈₀	I/O ₇₉	I/O ₇₇	I/O ₇₃	I/O ₇₀	I/O ₆₈	I/O ₆₅	GND	I/O ₆₁	I/O ₅₈	I/O ₅₅	I/O ₅₂ /SMODE	I/O ₄₉	I/O ₄₆	I/O ₄₂
A	I/O ₇₈	I/O ₇₅	I/O ₇₄	I/O ₇₁	I/O ₆₉	I/O ₆₇	I/O ₆₄	I/O ₆₃	I/O ₆₂	I/O ₅₉	I/O ₅₇	I/O ₅₄	I/O ₅₁	I/O ₄₈	I/O ₄₅
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Functional Description (continued)

Logic Block

The number of logic blocks distinguishes the members of the FLASH370i family. The CY7C375i includes eight logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370i logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370i PLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Each of the macrocells on the CY7C375i has a separate I/O pin associated with it. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and four global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the eight logic blocks on the CY7C375i to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Programming

For an overview of ISR programming, refer to the FLASH370i Family data sheet and for ISR cable and software specifications, refer to ISR data sheets. For a detailed description of ISR capabilities, refer to the Cypress application note, "An Introduction to In System Reprogramming with FLASH370i."

PCI Compliance

The FLASH370i family of CMOS CPLDs are fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The simple and predictable timing model of

FLASH370i ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without simple and predictable timing, PCI compliance is dependent upon routing and product term distribution.

Bus Hold Capabilities on all I/Os and Dedicated Inputs

In addition to ISR capability, a new feature called bus-hold has been added to all FLASH370i I/Os and dedicated input pins. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold recalls the last state of a pin when it is three-stated, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND.

Design Tools

Development software for the CY7C375i is available from Cypress's *Warp2*™, *Warp2Sim*™, and *Warp3*™ software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABEL™, CUPL™, and LOG/IC™. Please refer to third-party tool support data sheets for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Program Voltage	12.5V
Output Current into Outputs	16 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	–40°C to +85°C	5V ± 10%
Military ^[1]	–55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range^[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	I _{OH} = -3.2 mA (Com'l/Ind) ^[3]	2.4		V
			I _{OH} = -2.0 mA (Mil)			V
V _{OL}	Output LOW Voltage	V _{CC} = Min.	I _{OL} = 16 mA (Com'l/Ind) ^[3]		0.5	V
			I _{OL} = 12 mA (Mil)			V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs ^[4]		2.0	7.0	V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs ^[4]		-0.5	0.8	V
I _{IX}	Input Load Current	V _I = Internal GND, V _I = V _{CC}		-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		-50	+50	μA
I _{OS}	Output Short Circuit Current ^[5, 6]	V _{CC} = Max., V _{OUT} = 0.5V		-30	-160	mA
I _{CC}	Power Supply Current ^[7]	V _{CC} = Max., I _{OUT} = 0 mA, f = 1 MHz, V _{IN} = GND, V _{CC}	Com'l		330	mA
			Com'l "L" -66		150	mA
			Mil/Ind		370	mA
I _{BHL}	Input Bus Hold LOW Sustaining Current	V _{CC} = Min., V _{IL} = 0.8V		+75		μA
I _{BHH}	Input Bus Hold HIGH Sustaining Current	V _{CC} = Min., V _{IH} = 2.0V		-75		μA
I _{BHLO}	Input Bus Hold LOW Overdrive Current	V _{CC} = Max.		+500		μA
I _{BHHO}	Input Bus Hold HIGH Overdrive Current	V _{CC} = Max.		-500		μA

Capacitance^[6]

Parameter	Description	Test Conditions	Min.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 5.0V at f = 1 MHz		8	pF
C _{OUT}	Output Capacitance	V _{OUT} = 5.0V at f = 1 MHz		12	pF
C _{CLK}	Clock Signal Capacitance	V _{IN} = 5.0V at f = 1 MHz	5	12	pF

Inductance^[6]

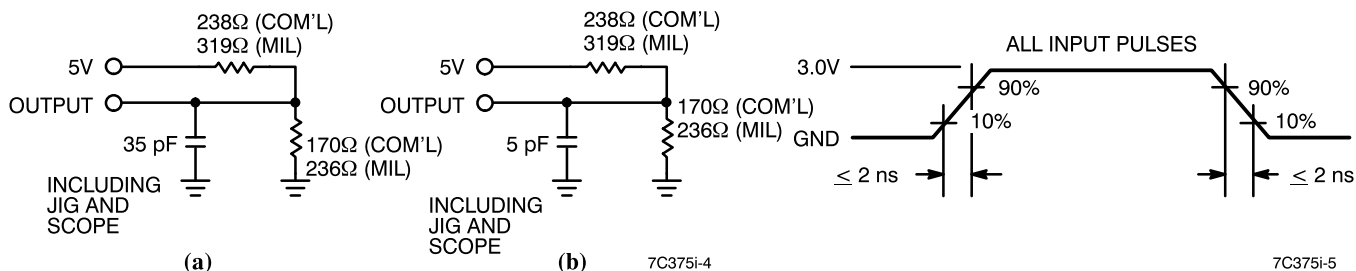
Parameter	Description	Test Conditions	160-Lead TQFP	160-Pin CQFP	160-Pin PGA	Unit
L	Maximum Pin Inductance	V _{IN} = 5.0V at f = 1 MHz	9	6	10	nH

Endurance Characteristics^[6]

Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

Notes:

- See the last page of this specification for Group A subgroup testing information.
- I_{OH} = -2 mA, I_{OL} = 2 mA for SDO. Note: SDI, SMODE, SCLK, have same V_{IH} and V_{IL}.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.
- Measured with 16-bit counter programmed into each logic block.

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT

99Ω (COM'L)
136Ω (MIL) 2.08V (COM'L)
2.13V (MIL)

Parameter ^[8]	V _X	Output Waveform—Measurement Level
t _{ER} (-)	1.5V	V _{OH} 0.5V V _X 7C375i-6
t _{ER} (+)	2.6V	V _{OL} 0.5V V _X 7C375i-7
t _{EA} (+)	1.5V	V _X 0.5V V _{OH} 7C375i-8
t _{EA} (-)	V _{thc}	V _X 0.5V V _{OL} 7C375i-9

(a) Test Waveforms

Switching Characteristics Over the Operating Range^[9]

Parameter	Description	7C375i-100		7C375i-83		7C375iL-66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters								
t _{PD}	Input to Combinatorial Output		12		15		20	ns
t _{PDL}	Input to Output Through Transparent Input or Output Latch		15		18		22	ns
t _{PDLL}	Input to Output Through Transparent Input and Output Latches		16		19		24	ns
t _{EA}	Input to Output Enable		16		19		24	ns
t _{ER}	Input to Output Disable		16		19		24	ns
Input Registered/Latched Mode Parameters								
t _{WL}	Clock or Latch Enable Input LOW Time ^[6]	3		4		5		ns
t _{WH}	Clock or Latch Enable Input HIGH Time ^[6]	3		4		5		ns
t _{IS}	Input Register or Latch Set-Up Time	2		3		4		ns
t _{IH}	Input Register or Latch Hold Time	2		3		4		ns
t _{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		16		19		24	ns
t _{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		18		21		26	ns

Notes:

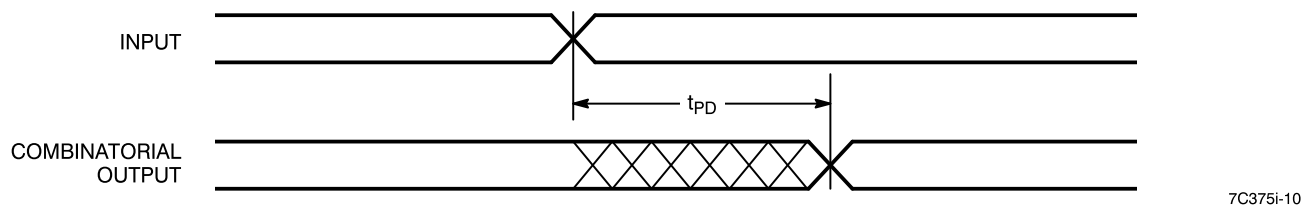
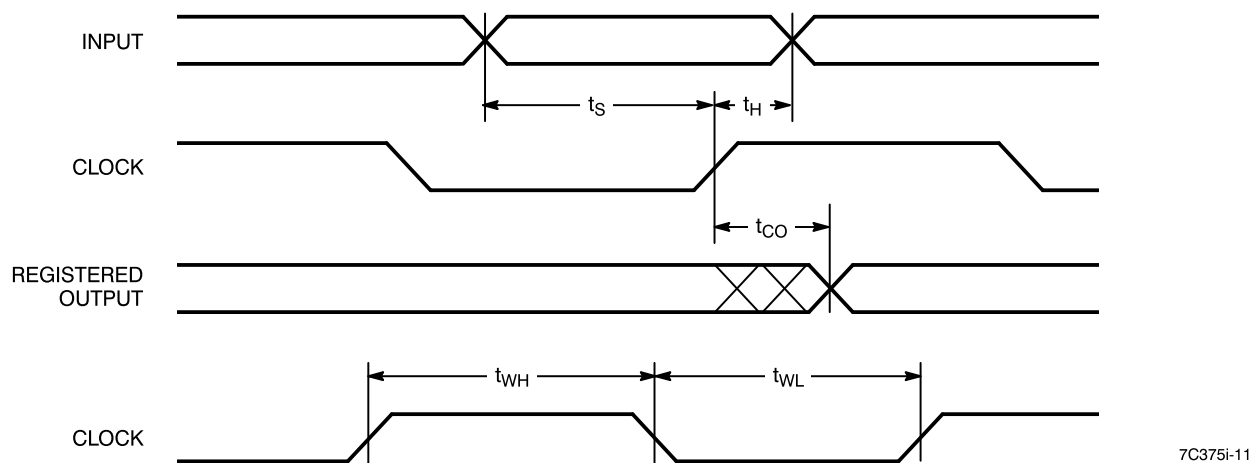
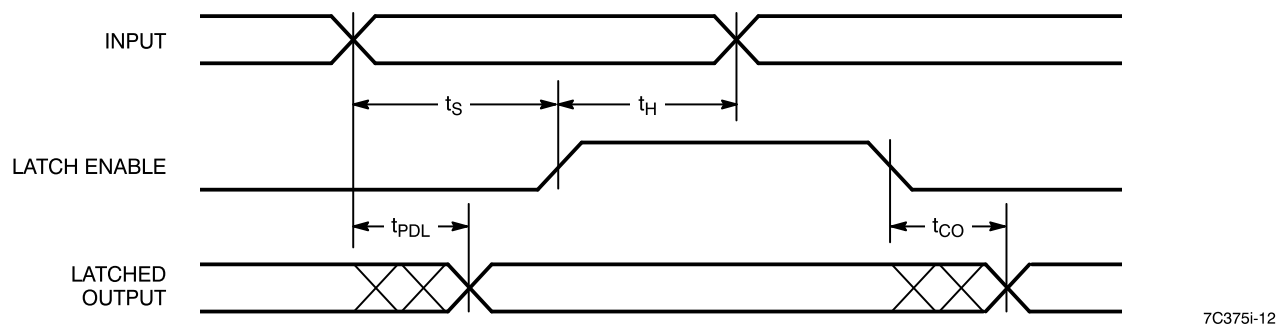
8. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.
9. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.

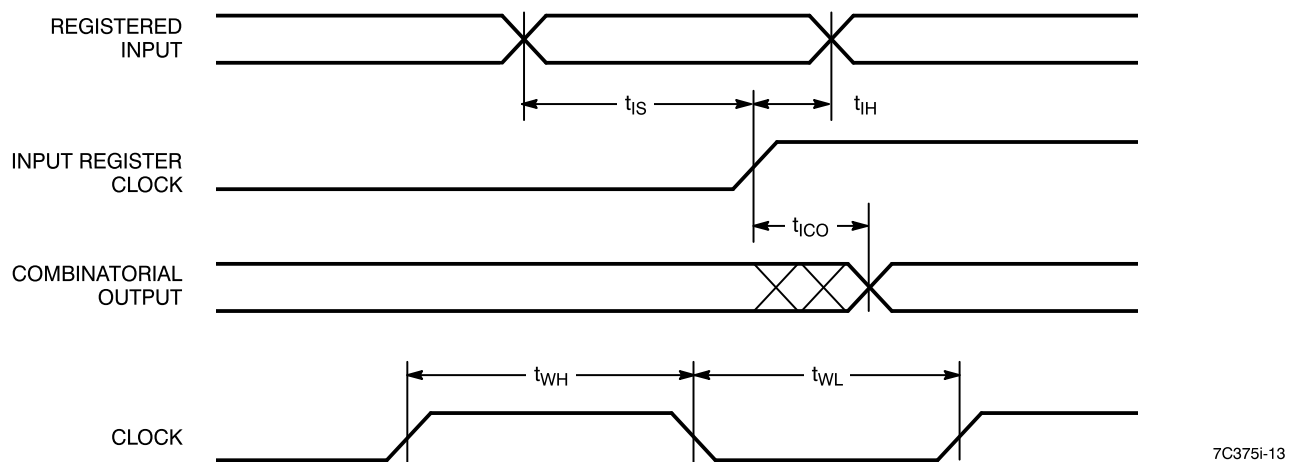
Switching Characteristics Over the Operating Range^[9] (continued)

Parameter	Description	7C375i–100		7C375i–83		7C375iL–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Output Registered/Latched Mode Parameters								
t _{CO}	Clock or Latch Enable to Output		7		8		10	ns
t _S	Set-Up Time from Input to Clock or Latch Enable	6		8		10		ns
t _H	Register or Latch Data Hold Time	0		0		0		ns
t _{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		16		19		24	ns
t _{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	10		12		15		ns
t _{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	12		15		20		ns
t _{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		ns
f _{MAX1}	Maximum Frequency with Internal Feedback (Least of 1/t _{SCS} , 1/(t _S + t _H), or 1/t _{CO}) ^[6]	100		83		66		MHz
f _{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of 1/(t _{WL} + t _{WH}), 1/(t _S + t _H), or 1/t _{CO})	143		125		100		MHz
f _{MAX3}	Maximum Frequency with External Feedback (Lesser of 1/(t _{CO} + t _S) and 1/(t _{WL} + t _{WH}))	76.9		62.5		50		MHz
t _{OH} –t _{IH} 37x	Output Data Stable from Output Clock Minus Input Register Hold Time for 7C37x ^[6, 10]	0		0		0		ns
Pipelined Mode Parameters								
t _{ICS}	Input Register Clock to Output Register Clock	10		12		15		ns
f _{MAX4}	Maximum Frequency in Pipelined Mode (Least of 1/(t _{CO} + t _{IS}), 1/t _{ICS} , 1/(t _{WL} + t _{WH}), 1/(t _{IS} + t _{IH}), or 1/t _{SCS})	100		83.3		66.6		MHz
Reset/Preset Parameters								
t _{RW}	Asynchronous Reset Width ^[6]	12		15		20		ns
t _{RR}	Asynchronous Reset Recovery Time ^[6]	14		17		22		ns
t _{RO}	Asynchronous Reset to Output		18		21		26	ns
t _{PW}	Asynchronous Preset Width ^[6]	12		15		20		ns
t _{PR}	Asynchronous Preset Recovery Time ^[6]	14		17		22		ns
t _{PO}	Asynchronous Preset to Output		18		21		26	ns
t _{POR}	Power-On Reset		1		1		1	μs
Tap Controller Parameter								
f _{TAP}	Tap Controller Frequency	500		500		500		kHz

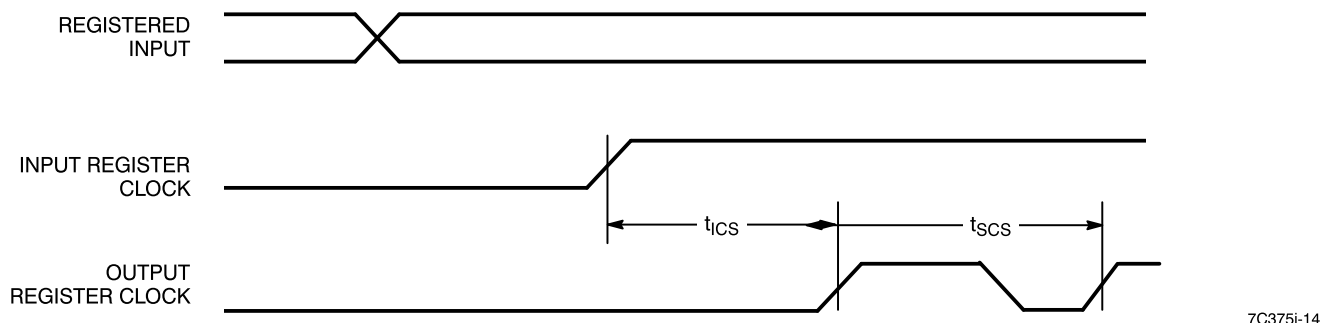
Note:

10. This specification is intended to guarantee interface compatibility of the other members of the CY7C370i family with the CY7C375i. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

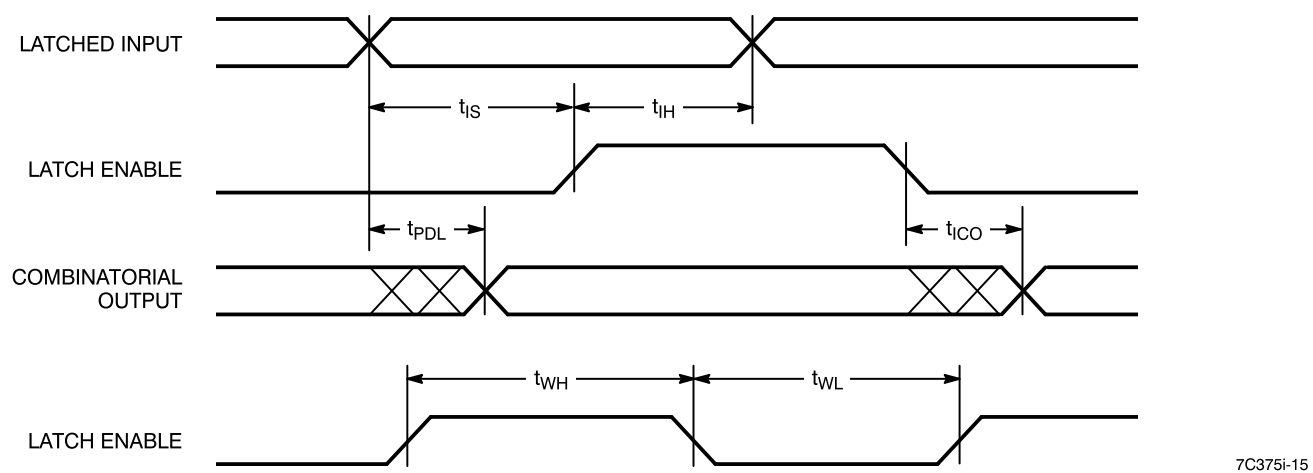
Switching Waveforms
Combinatorial Output

Registered Output

Latched Output


Switching Waveforms (continued)
Registered Input


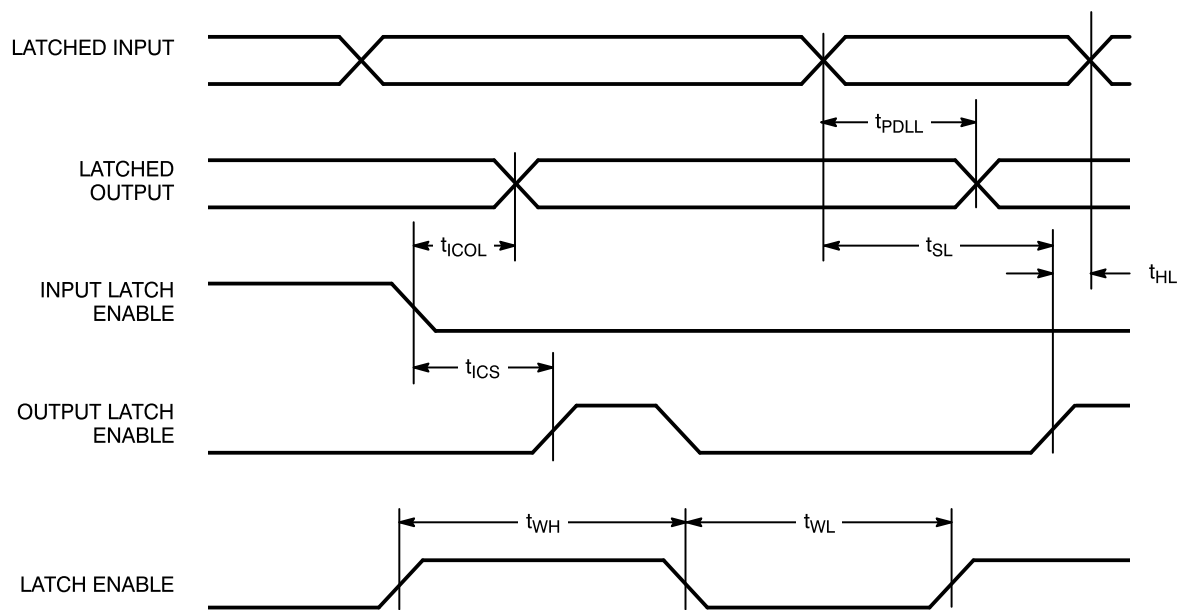
7C375i-13

Clock to Clock


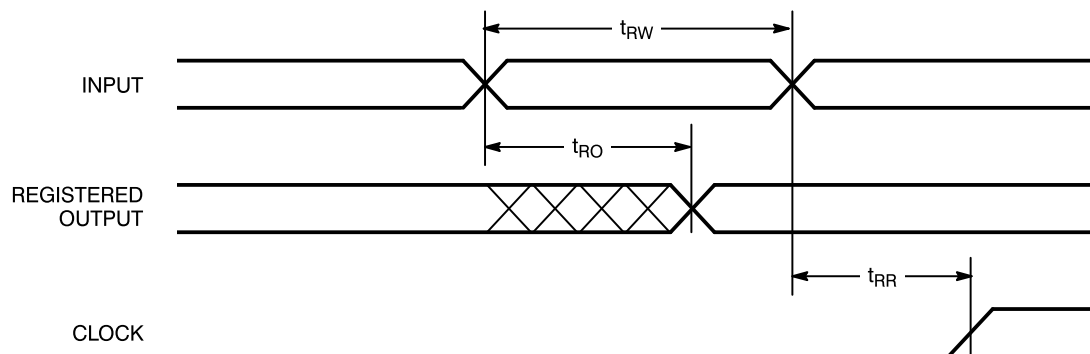
7C375i-14

Latched Input


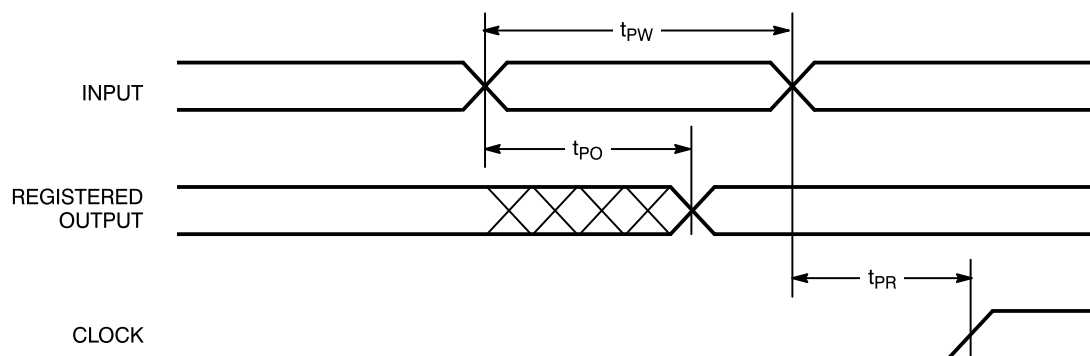
7C375i-15

Switching Waveforms (continued)
Latched Input and Output


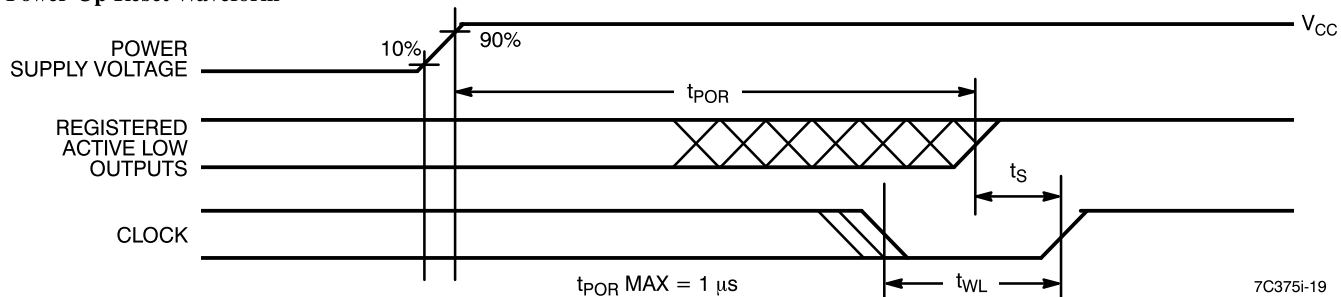
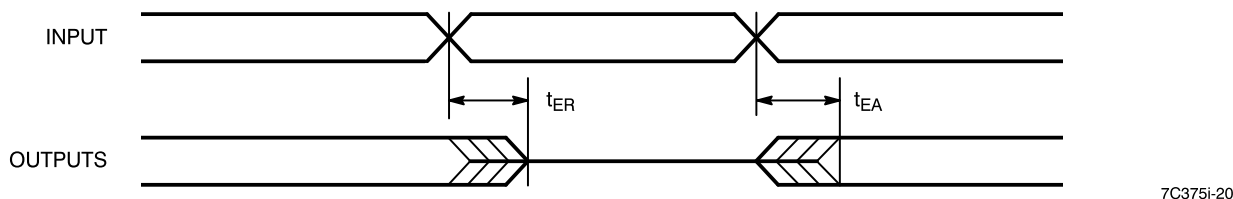
7C375i-16

Asynchronous Reset


7C375i-17

Asynchronous Preset


7C375i-18

Switching Waveforms (continued)
Power-Up Reset Waveform

Output Enable/Disable

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
100	CY7C375i-100AC	A160	160-Lead Thin Quad Flatpack	Commercial
83	CY7C375i-83AC	A160	160-Lead Thin Quad Flatpack	Commercial
	CY7C375i-83AI	A160	160-Lead Thin Quad Flatpack	Industrial
	CY7C375i-83GMB	G160	160-Pin Grid Array	Military
	CY7C375i-83UMB	U162	160-Pin Ceramic Quad Flatpack ^[11]	
66	CY7C375i-66AC	A160	160-Lead Thin Quad Flatpack	Commercial
	CY7C375i-66AI	A160	160-Lead Thin Quad Flatpack	Industrial
	CY7C375i-66GMB	G160	160-Pin Grid Array	Military
	CY7C375i-66UMB	U162	160-Pin Ceramic Quad Flatpack ^[11]	
66	CY7C375iL-66AC	A160	160-Lead Thin Quad Flatpack	Commercial

Note:

11. Available as custom trim and form version. Contact local Cypress office for package information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{PD}	9, 10, 11
t _{CO}	9, 10, 11
t _{ICO}	9, 10, 11
t _S	9, 10, 11
t _H	9, 10, 11
t _{IS}	9, 10, 11
t _{IH}	9, 10, 11
t _{ICS}	9, 10, 11

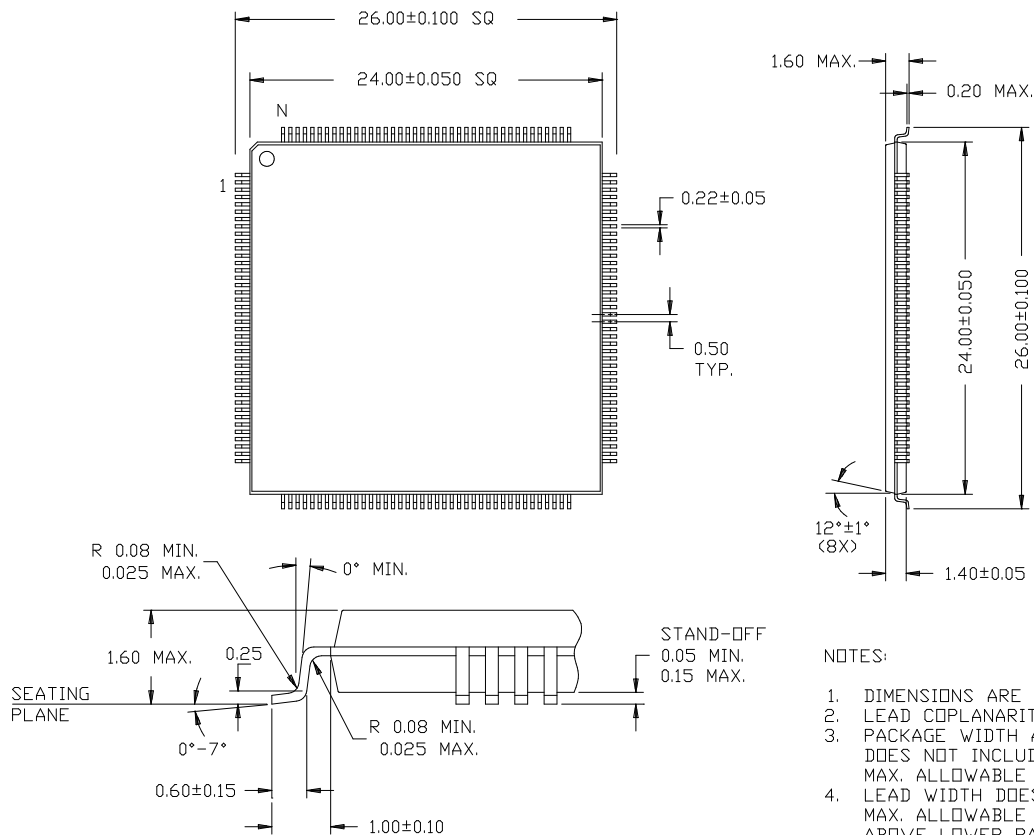
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LOG/iC is a trademark of Isdata Corporation.

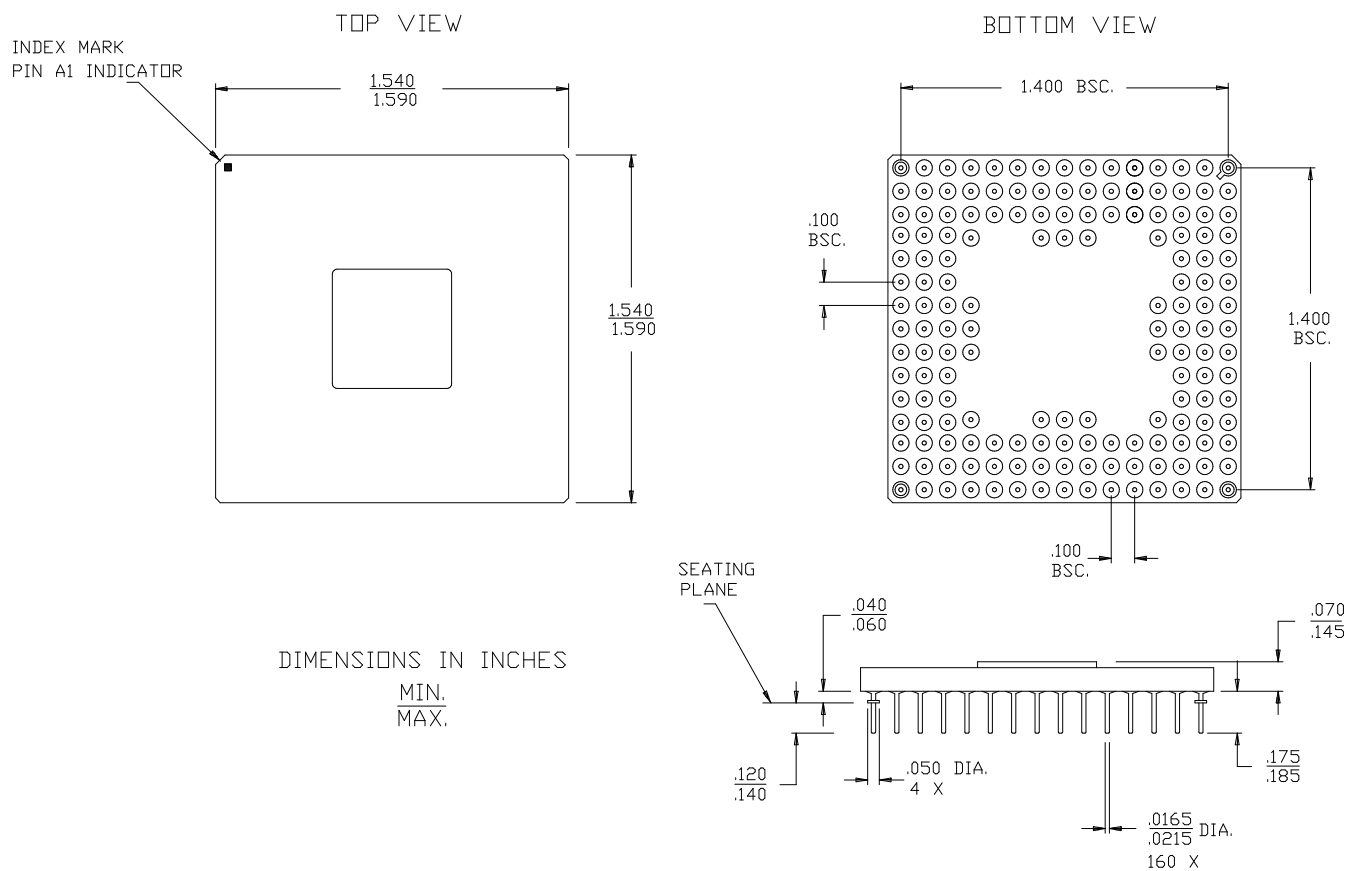
CUPL is a trademark of Logical Devices Incorporated.

Package Diagrams
160-Lead Thin Quad Flat Pack (TQFP) A160

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. LEAD COPLANARITY 0.100 MAX.
3. PACKAGE WIDTH AND LENGTH (24.00 ± 0.05) DOES NOT INCLUDE MOLD PROTRUSION. MAX. ALLOWABLE PROTRUSION IS 0.25 MM.
4. LEAD WIDTH DOES NOT INCLUDE DAMBAR PROTRUSION. MAX. ALLOWABLE DAMBAR PROTRUSION ABOVE LOWER RADIUS IS 0.08 MM.

Package Diagrams (continued)

160-Pin PGA G160



Package Diagrams (continued)
160-Lead Ceramic Quad Flatpack (Cavity Up) U162
