isrintro: February 15, 1996
Revision: February 19, 1996

An Introduction to In System Reprogramming with FLASH370i™

Introduction

This application note provides an introduction to the FLASH370i™ family of In System Reprogrammable (ISR™) CPLDs. The FLASH370i ISR CPLD family is a superset replacement for the popular FLASH370™ CPLD family. All of the features and advantages of the FLASH370 CPLD architecture are present in the FLASH370i CPLD architecture, with the FLASH370i family also providing additional capabilities. The most celebrated new feature is the capability for the FLASH370i devices to be reprogrammed in the user's system.

In System Reprogrammability is the capability of a programmable device to be reprogrammed after being soldered onto a printed circuit board. This allows the configuration and functionality of a device, and therefore the electronic system in which it is contained, to be modified after the system has completed the manufacturing cycle. Reprogramming can happen at any time, such as prior to the shipment of the system or product, in the form of a field upgrade to provide additional capabilities and features or to correct previous problems, or during actual system operation so that a different function or algorithm is implemented.

In many cases, ISR capability is used only to simplify the manufacturing cycle, by eliminating the handling of a traditional programmable logic device to facilitate programming. With an ISR device, one handling step can be removed if desired. Additionally, ISR devices can be reprogrammed again and again as required.

Several topics and issues are introduced in this application note. These are: the compatibility of the FLASH370i CPLD family with the FLASH370 family, the features of ISR, the FLASH370i pin descriptions and pinouts, the ISR programming options, the ISR programming interface, the FLASH370i ISR kit, and the other application notes that address other ISR design issues more specifically.

Compatibility of the FLASH370i and FLASH370 CPLD Families

Like the FLASH370 CPLD family, the FLASH370i family comprises five devices at three standard densities: 32, 64, and 128 macrocells. For each density, there is a device that has all macrocells associated with I/O pins, and for the 64-macrocell and 128-macrocell densities, there are devices that have half of the macrocells associated with I/O pins. Each of the five devices has six additional dedicated input pins with up to four of these available as high-speed clocks.

Each FLASH370i device is both functionally and pinout compatible with a FLASH370 device. As such, the CY7C371i 32-macrocell device has the same number of flexible macrocells, the same number and superior allocation of product terms, the same robust interconnect that provides the same excellent routability, the same output enable capability, and even the same, identical JEDEC map as the CY7C371 32-macrocell device that it replaces. This same statement applies equally to the other four devices of the FLASH370i CPLD family. The normal PAL mode functionality of a FLASH370i device is also exactly the same as the normal PAL mode functionality of its FLASH370 counterpart. The speed grades

of the two CPLD families match, while maintaining the same parallel programming algorithms.

As previously mentioned, the major difference between the FLASH370i and the FLASH370 CPLD families is that the FLASH370i CPLD family provides the capability for in system reprogramming. Other new features of the FLASH370i devices are outputs that are fully PCI (peripheral component interconnect) compliant and bus-hold structures on all pins. While the FLASH370 CPLDs were suitable for use in PCI bus applications, the FLASH370i CPLDs are fully compliant with the electrical requirements of the PCI specification over all operating temperatures and voltages. The bus-hold structures eliminate the need for connecting unused inputs and I/O pins to a supply by providing an improved version of an internal pull-up resistor. The bus-hold structure provides a weak internal pull-up or pull-down, depending upon the last driven state on the pin, and it is initialized at power-up to provide a weak pull-up.

Overview of the FLASH370i ISR Features

The FLASH370i ISR capability is provided through a four-pin JTAG interface comprising a clock (SCLK), a mode select (SMODE), a serial data in (SDI), and a serial data out (SDO). Additionally, there is a fifth pin, ISRVPP, that provides the high voltage required for programming and erasing the flash programmable portion of the CPLD.

The ISR interface is provided in one of two modes. These two modes are termed “single function” and “dual function.” The basic difference between these two modes is that the five ISR interface pins have either one function or two functions. *Table 1* shows the FLASH370i devices and the function mode for each.

For the CY7C373i and CY7C374i in 100-pin packages, the four basic ISR interface pins, SCLK, SMODE, SDI, and SDO, are assigned to pins that were previously no-connects on the CY7C374. The ISRVPP pin is also assigned to a CY7C374 no-connect pin. This is the simpler ISR interface, and since every pin only has a single function, these are the single-function FLASH370i devices.

Table 1. FLASH370i Device Function Modes

Device	# Macrocells	# Pins	Function Mode	
CY7C371i	32	44	—	dual
CY7C372i	64	44	—	dual
CY7C373i	64	84	—	dual
CY7C373i	64	100	single	—
CY7C374i	128	84	—	dual
CY7C374i	128	100	single	—
CY7C375i	128	160	—	dual

All other FLASH370i CPLDs are dual function mode devices. As shown in *Table 1*, this includes the CY7C371i, CY7C372i, and CY7C375i devices, and also the CY7C373i and CY7C374i devices in 84-pin packages.

The single-function solution also provides extra diagnostic capability as compared to the dual-function devices. For all FLASH370i ISR devices, when the ISRVPP pin is at high voltage, the full capability to program, erase, read, or verify the device is provided. For single-function FLASH370i devices, reading and verifying the device is provided even when the ISRVPP pin is not at a high voltage. This allows diagnostic software to have normal, operational voltage access to the silicon ID, user ID, bypass mode, and complete programmed pattern when using single function devices.

Cascading and program security are also features of the FLASH370i ISR family of CPLDs. The FLASH370i ISR interface provides unlimited cascading capability, as FLASH370i CPLDs can be cascaded homogeneously or with other devices that support the IEEE 1149.1 JTAG interface. FLASH370i devices are cascaded by connecting the SDO pin of one device to the SDI pin of the next device, while also connecting the SCLK, SMODE, and ISRVPP pins of all devices in parallel, just as provided in the IEEE 1149.1 specification. Also, a security bit is included and can be programmed if desired to disallow the reading or verifying of a FLASH370i device, thus protecting the programmable device’s contents from being discovered.

FLASH370i Pin Descriptions

Tables 2 and *3* describe the functionality of all of the pins for the FLASH370i devices. *Table 2* is for the dual-function FLASH370i devices, and *Table 3* is for the single-function devices. Each table has two parts, part A and part B. Part A of each table describes the pin functionality when the ISRVPP pin is at high voltage, i.e., 12V. Part B gives the pin functionality for the ISRVPP pin being in the normal operating range of 0V to 5V.

Table 2A. Dual-Function Pin Descriptions (ISRVPP = 12V; ISR Interface Enabled)

Pin	Mode	Description
ISRVPP (I)	Input	Provides the high voltage to the programming circuitry and is used to differentiate the function of the other pins; the bus-hold structure is connected
SCLK (I/O)	Input	I/O three-stated with the bus-hold structure connected; functions as SCLK input for the ISR interface
SMODE (I/O)	Input	I/O three-stated with the bus-hold structure connected; functions as SMODE input for the ISR interface
SDI (I/O)	Input	I/O three-stated with the bus-hold structure connected; functions as SDI input for the ISR interface
SDO (I/O)	Output	Functions as SDO output for the ISR interface; the output is enabled when the JTAG state machine is in the Shift-IR or Shift-DR states and is three-stated in the other states as defined in the 1149.1 spec; the bus-hold structure is connected
Other I/Os	High-Z	Output three-stated with the bus-hold structure connected
Other Inputs	High-Z	Unused with the bus-hold structure connected
Other I/CLKs	High-Z	Unused with the bus-hold structure connected

Table 2B. Dual-Function Pin Descriptions (ISRVPP not 12V; ISR Interface Disabled)

Pin	Mode	Description
Input (ISRVPP)	Input	Normal input function; the bus-hold structure is connected
I/O (SCLK) I/O (SMODE) I/O (SDI) I/O (SDO)	I/O I/O I/O I/O	Normal I/O function; each of these pins functions according to how the device is programmed; the bus-hold structure is connected; the JTAG state machine returns to the “Test-Logic-Reset” state when ISRVPP is in the normal operating range and does not interfere with the normal operation of the device
Other I/Os	I/O	Normal I/O function; each of these pins functions according to how the device is programmed; the bus-hold structure is connected
Other Inputs	Input	Normal input function; the bus-hold structure is connected
Other I/CLKs	I/CLK	Normal input/clock function; the bus-hold structure is connected

Table 3A. Single-Function Pin Descriptions (ISRVPP = 12V; ISR Enabled)

Pin	Mode	Description
ISRVPP	Input	Provides the high voltage to the programming circuitry to enable all ISR operations; the JTAG state machine is completely operational independent of the state of the ISRVPP pin
SCLK	Input	Functions as SCLK input for the ISR interface; the bus-hold structure is connected
SMODE	Input	Functions as SMODE input for the ISR interface; the bus-hold structure is connected
SDI	Input	Functions as SDI input for the ISR interface; the bus-hold structure is connected
SDO	Output	Functions as SDO output for the ISR interface; the output is enabled when the JTAG state machine is in the Shift-IR or Shift-DR states as defined in the 1149.1 spec; the bus-hold structure is not connected
All I/Os	High-Z	Output three-stated with the bus-hold structure connected
All Inputs	High-Z	Unused with the bus-hold structure connected
All I/CLKs	High-Z	Unused with the bus-hold structure connected

Table 3B. Single-Function Pin Descriptions (ISRVPP not 12V; ISR Programming Disabled)

Pin	Mode	Description
ISRVPP	Input	All ISR operations except for the programming and erasing functions are enabled
SCLK	Input	Functions as SCLK input for the ISR interface; the bus-hold structure is connected
SMODE	Input	Functions as SMODE input for the ISR interface; the bus-hold structure is connected
SDI	Input	Functions as SDI input for the ISR interface; the bus-hold structure is connected
SDO	Output	Functions as SDO output for the ISR interface; the output is enabled when the JTAG state machine is in the Shift-IR or Shift-DR states as defined in the 1149.1 spec; the bus-hold structure is not connected
All I/Os	I/O	Normal I/O function; the bus-hold structure is connected
All Inputs	Input	Normal input function; the bus-hold structure is connected
All I/CLKs	I/CLK	Normal input/clock function; the bus-hold structure is connected

FLASH370i Pinouts

As previously described, there are single-function and dual-function FLASH370i ISR devices. The CY7C373i and CY7C374i in 100-pin packages are the single-function FLASH370i ISR solutions, and the ISR pin assignments for these are shown in *Table 4*.

Table 4. ISR Pins for the 100-Pin CY7C373i and CY7C374i

ISR Pin	Normal Mode	TQFP Pin #
ISRVPP	N/A	88
SCLK	SCLK	1
SMODE	SMODE	26
SDI	SDI	75
SDO	SDO	50

All other FLASH370i ISR devices besides the 100-pin CY7C373i and CY7C374i are dual-function ISR solutions. The pin assignments for all of these devices are shown in *Tables 5*, *6*, and *7*. *Table 5* shows the ISR pin assignments for the CY7C373i and CY7C374i in 84-pin packages. *Table 6* shows the ISR pin assignments for the CY7C375i, which has 160 total pins. *Table 7* shows the ISR pin assignments for the CY7C371i and CY7C372i in 44-pin packages.

Table 5. ISR Pins for the 84-Pin CY7C373i and CY7C374i

ISR Pin	Normal Mode	PLCC Pin #	CLCC Pin #	PGA Pin #
ISRVPP	I5	83	83	C7
SCLK	I/O 10	14	14	C1
SMODE	I/O 26	35	35	L3
SDI	I/O 54	72	72	C10
SDO	I/O 38	51	51	K9

Note: The CY7C373i is not available in the CLCC or PGA packages.

Table 6. ISR Pins for the 160-Pin CY7C375i

ISR Pin	Normal Mode	TQFP Pin #	CQFP Pin #	PGA Pin #
ISRVPP	I5	139	139	N8
SCLK	I/O 20	6	6	M14
SMODE	I/O 52	46	46	B12
SDI	I/O 108	116	116	N2
SDO	I/O 76	76	76	C4

Table 7. ISR Pins for the 44-Pin CY7C371i and CY7C372i

ISR Pin	Normal Mode	PLCC Pin #	TQFP Pin #
ISRVPP	I1	11	5
SCLK	I/O 5	7	1
SMODE	I/O 13	19	13
SDI	I/O 27	39	22
SDO	I/O 19	27	21

Note: The CY7C372i is not available in the TQFP package.

Overview of ISR Programming Options

There are four programming options available for FLASH370i devices. The first is to use a PC with the FLASH370i ISR programming cable and software. With this method, the ISR pins of the FLASH370i devices are routed to a connector at the edge of the printed circuit board. The ISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the FLASH370i devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions that are supported.

The second method for programming FLASH370i devices is on an ATE (automatic test equipment). If this method is selected, the FLASH370i ISR software generates programming test vectors for the target tester.

The third programming option for FLASH370i devices is to utilize the embedded controller or proces-

sor that already exists in the electronic system. The FLASH370i ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of FLASH370i devices to complete the desired reconfiguring or diagnostic operations.

The fourth method for programming FLASH370i devices is to use the same parallel programmer that is currently being used to program FLASH370 devices. Since the programming algorithms are the same, normal third party programming support for the FLASH370i family is readily available.

FLASH370i ISR Programming Interface

Although detailed knowledge of the ISR internal architecture is not required for users to design with or program FLASH370i devices, the basics are provided here for those interested. The IEEE 1149.1 specification, or JTAG (Joint Test Access Group), requires that the finite state machine shown in *Figure 1* be implemented for controlling the sequence of operations. Transitions are made on the rising edge of SCLK, and the SMODE input determines the next state.

Figure 2 shows the ISR internal registers that are linked between the serial data input (SDI) and the serial data output (SDO). There are five registers: the Byte Register (BR), the Address Register (AR), the Fast Verify Register (FVR), the Bypass Register (BPR), and the Instruction Register (IR).

The 4-bit instruction register holds the instruction to be executed. The supported instructions and their codes are shown in *Table 8*. The execution of each instruction is beyond the scope of this application note, but the instructions are presented to indicate that the codes are consistent with the IEEE

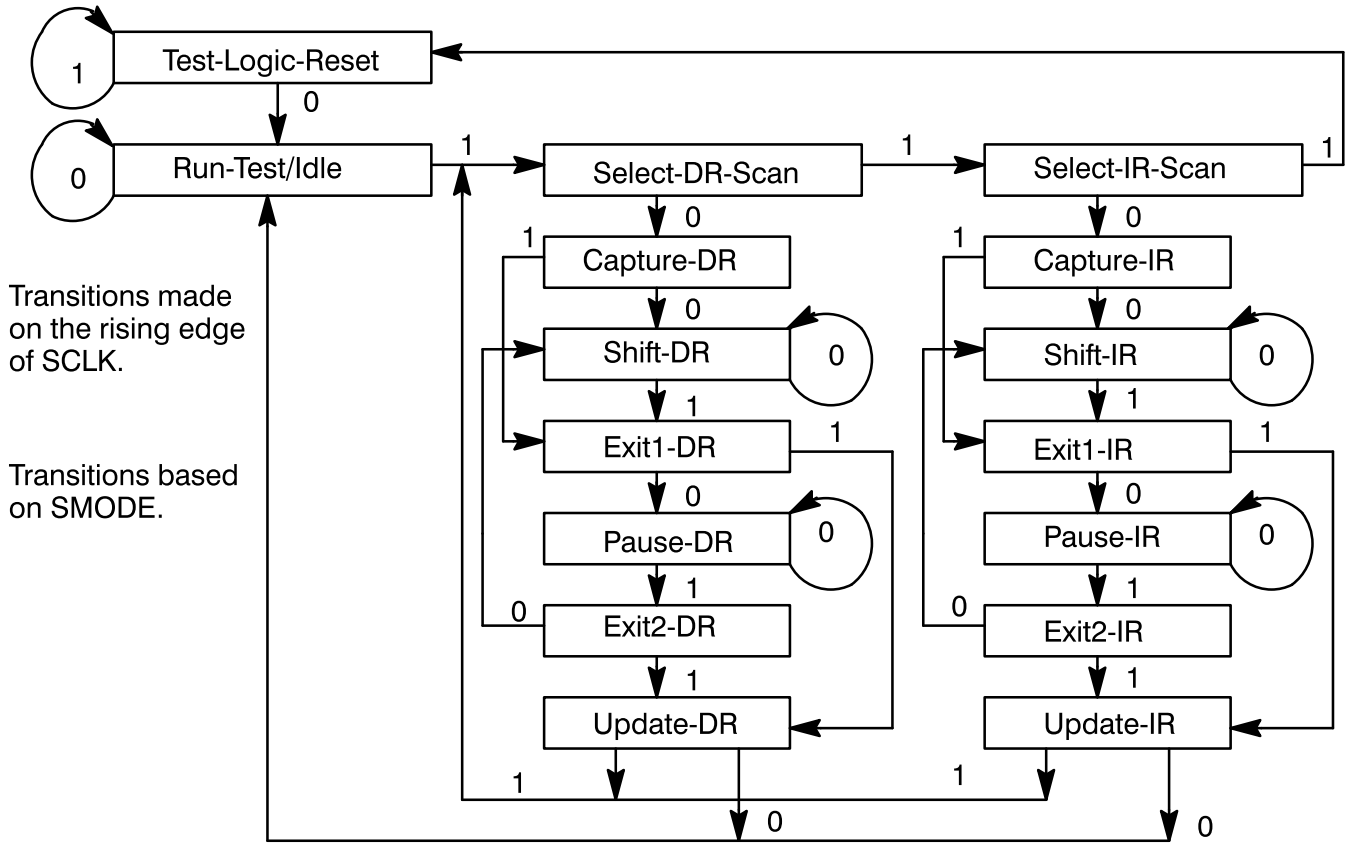

Figure 1. JTAG State Diagram

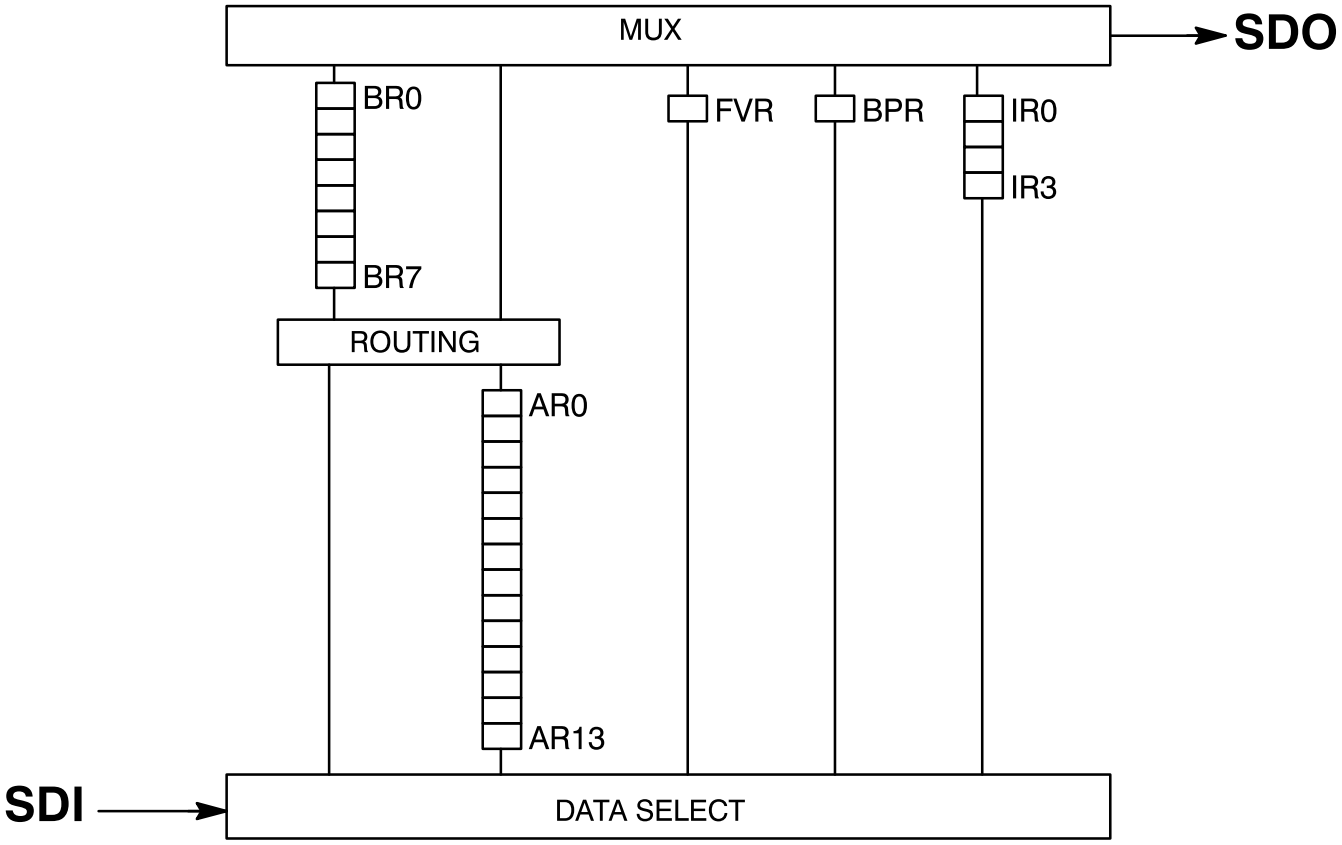

Figure 2. FLASH370i ISR Interface Registers

1149.1 specification, which requires that the EXTEST and BYPASS be assigned the codes with all 0s and 1s, respectively.

Table 8. FLASH370i ISR Instruction Set

Code	Instruction
0000	(Reserved for EXTEST)
0100	Read Location (Shift AR&BR)
0101	Program / Shift AR&BR
0111	Program / Shift AR
1000	Initiate Power-On-Reset
1001	Read Silicon ID (Shift FVR)
1010	Program / Fast Verify (Shift FVR)
1100	Erase Device
1101	Program / Shift BR
1111	BYPASS

The address register holds the address of the memory location to be programmed, read, or verified. As indicated in *Figure 1*, there is an additional routing block that allows the address register and the byte register to be concatenated during shifting. This reduces the time required to complete some of the programming operations, but is transparent to the user.

The byte register is used for multiple purposes. The first is to shift in and hold the data that is used for programming a memory location. The second use is for holding and shifting the memory location data during a read operation. The third use of the byte register is to hold and shift the data when executing the read silicon ID instruction. The fourth use is to hold and shift the data when executing the read user ID instruction.

The fast verify register and function enhances the programming and verification process. During portions of the programming flow, a fast verify opera-

tion compares the addressed memory byte with the contents of the byte register, and a single bit is loaded into FVR to indicate the outcome of the comparison. This single bit is then shifted out of the FLASH370i device.

The single-bit bypass register is used for implementing the bypass mode. This is a requirement of the IEEE 1149.1 specification, and helps the entire system perform operations more quickly than otherwise would be possible.

FLASH370i ISR Kit

The FLASH370i ISR kit comes complete with the following items: the ISR User's Guide, the ISR PC programming cable, the ISR software, and all ISR application notes.

The ISR User's Guide contains the documentation of how to use the ISR software for the chosen programming method. Also included in the ISR User's Guide is a list of error messages that the ISR software generates if problems are encountered.

The ISR programming cable provided in the FLASH370i ISR kit is used to facilitate programming from a PC. The ISR programming cable is connected between the parallel port of the PC and the connector at the edge of the printed circuit board which contains the FLASH370i devices.

The ISR software is used for programming FLASH370i devices in all serial programming methods: PC, ATE, and embedded controller.

Other FLASH370i ISR Application Notes

Additionally, the FLASH370i ISR kit contains this application note and all other ISR application notes to assist designers in utilizing the FLASH370i CPLDs properly. A brief introduction to each of these application notes is provided here to help direct designers to where additional design information can be found.

"Designing with FLASH370i for PC Cable Programming." This application note provides detailed design information on utilizing single-function mode and dual-function mode FLASH370i devices. Utilizing a dual-function mode device in the single-function mode, guidelines for routing the ISRVPP signal on the printed circuit board, and other board design issues are only part of the PC cable programming application note.

"Cascading FLASH370i Devices." FLASH370i devices can be cascaded not only with each other, but with other devices that support the IEEE 1149.1 JTAG interface. This is independent of whether or not the other devices are programmable. This application note provides insight into how simple and complex cascading is accomplished.

"Designing with FLASH370i for Board Tester Programming." This application note is similar to the PC cable programming application note. This board tester application note discusses the additional design issues related to programming a FLASH370i ISR device using an ATE.

"Designing with FLASH370i for Embedded Controller Programming." This application note is also similar to the PC cable programming application note. This embedded controller programming application note discusses the specific design issues for using one popular microcontroller to reconfigure FLASH370i devices, and how this information applies to other microcontrollers and microprocessors is also presented.

"The Impact of Routability on Using FLASH370i ISR Devices for Debugging and Making Field Upgrades." The intentions for utilizing a reprogrammable device that is permanently connected within an electronic system are sometimes quite large. Being successful when utilizing a reprogrammable device begins with a firm understanding of the features and capabilities of the device's architecture. With this understanding, being able to complete operations like field upgrades without encountering unexpected problems is more likely. This application note provides additional insight into the FLASH370i CPLD architecture to assist designers in gaining the necessary expertise to use ISR effectively.

"FLASH370i ISR Demonstration and Evaluation Boards." Every demonstration or evaluation board that is built for FLASH370i devices is documented in the form of an application note. The schematics for the board, the VHDL code used to describe the de-

signs contained within the devices, and the design issues and solutions are provided in these application notes.

Conclusion

This application note provides the introductory information to begin designing with the FLASH370i family of In System Reprogrammable (ISR) CPLDs. The FLASH370i ISR CPLD family is a superset replacement for the popular FLASH370 CPLD family that maintains all of the features and advantages of the FLASH370 CPLD architecture. The FLASH370i family additionally provides the ability for the device to be reprogrammed in the system. More detailed information for designing with the FLASH370i CPLD family is available with the FLASH370i ISR kit, and the appropriate information should be reviewed prior to designing with a FLASH370i device.

FLASH370, FLASH370i, and ISR are trademarks of Cypress Semiconductor Corporation.