



100BASE-T4/10BASE-T Fast Ethernet Transceiver (CAT 3)

Features

- Complies with IEEE 802.3u draft standard
- Three operating modes:
 - 100BASE-T4
 - 10BASE-T Full Duplex
 - 10BASE-T
- Media Independent Interface (MII)
 - Three-state receive port
 - Serial management port
- Auto-Negotiation
- On-chip transmit wave shaper
- Receive filter and adaptive equalization
- PMA Interface for repeater applications
- Jam function for hub applications
- LED status indicators: TX, RX, Link

- Loopback mode for PHY integrity testing
- Auto-polarity correction
- Low-power CMOS
- 80-pin PQFP

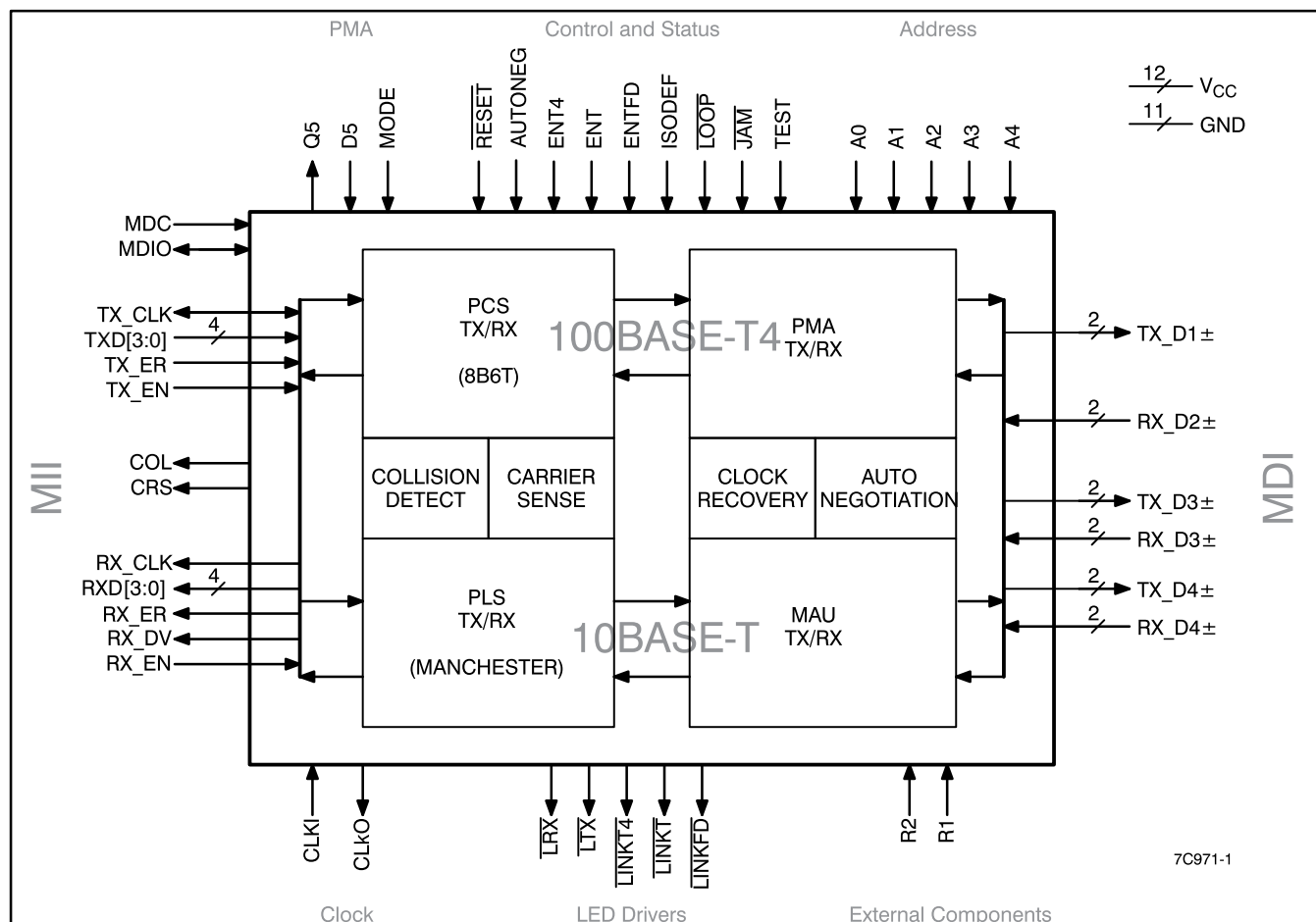
Functional Description

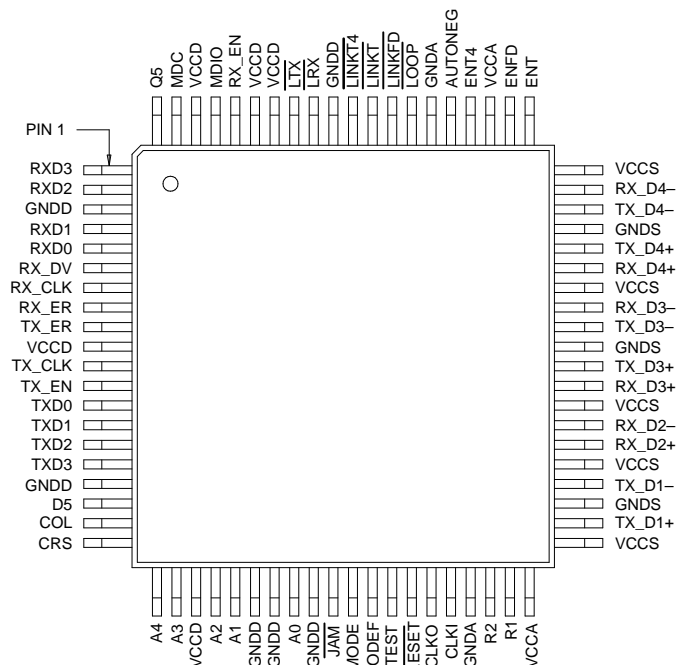
The CY7C971 is a full featured physical layer transceiver (PHY) device supporting both 100BASE-T4 (Fast Ethernet) and 10BASE-T Local Area Network (LAN) standards. The CY7C971 complies with IEEE 802.3 100BASE-T4, 10BASE-T, MII, and Auto-Negotiation standards for twisted pair interfaces.

The CY7C971 interfaces to category 3, 4, or 5 unshielded twisted-pair cable through its Media Dependent Interface (MDI). The Media Independent Interface (MII) attaches directly to Media Access Control (MAC) layer devices.

The CY7C971 performs the Physical Coding Sublayer (PCS), Physical Layer Signaling (PLS), Physical Media Attachment (PMA), and Media Attachment Unit (MAU) functions defined in the 802.3 standard. Ethernet frames are transferred from the MAC to the CY7C971 over the MII interface. The data is encoded in the PCS or PLS encoder (8B6T for 100BASE-T4 or Manchester for 10BASE-T) and then passed to the PMA or MAU where the encoded data is shifted bitwise on to the twisted-pair media. Collision and Carrier Sense signals are generated by the CY7C971 and passed to the MAC over the MII.

The CY7C971 PHY uses 802.3 standard Auto Negotiation to configure the link. The PHY includes a direct interface to the PMA layer for repeater applications.



Pin Configuration
**80-Lead Plastic Quad Flatpack
(Top View)**


7C971-2

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with
Power Applied -55°C to $+125^{\circ}\text{C}$

Supply Voltage to Ground Potential -0.5V to $+7.0\text{V}$

DC Voltage Applied to Outputs
in High Z State -0.5V to $+7.0\text{V}$

DC Input Voltage -3.0V to $+7.0\text{V}$

Static Discharge Voltage $>2001\text{V}$
(per MIL-STD-883, Method 3015)

Latch-Up Current $>200\text{ mA}$
Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Pin Descriptions
Media Independent Interface (MII)

Name	I/O	Description
TXD[3:0] (D[3:0])	Input (TTL)	Transmit Data. TXD[3:0] are the data signals that carry the Ethernet transmit frame data from the MAC to the PHY on a nibble basis. TXD[3:0] are sampled on the rising edge of TX_CLK when TX_EN is asserted HIGH. In PMA mode, these pins become the D[3:0] pins used for passing binary encoded 8B6T symbols to the PMA sublayer.
TX_EN	Input (TTL)	Transmit Enable. When asserted HIGH, TX_EN indicates that the MAC is presenting data to the TXD[3:0] inputs of the PHY. TX_EN should be asserted HIGH with the first nibble of the preamble and remain HIGH for the duration of the frame. TX_EN should be deasserted on the first cycle following the final nibble of the frame. In PMA mode, TX_EN is asserted HIGH in order to latch D[5:0] into the transmitter.
TX_CLK	Output (TTL, Three State)	Transmit Clock. In MII Mode (MODE = HIGH), TX_CLK is a continuous clock that provides a timing reference for the transfer of TXD[3:0], TX_EN, and TX_ER from the MAC. The nominal frequency of TX_CLK is 25 MHz in 100-Mb/s mode and 2.5 MHz in 10-Mb/s mode.
TX_ER (D4)	Input (TTL)	Transmit Coding Error. When asserted HIGH while TX_EN is HIGH, the PHY will transmit an error code word. TX_ER is sampled on the rising edge of TX_CLK. In PMA mode, this pin becomes the D4 pin used for passing binary encoded 8B6T symbols to the PMA sublayer.
RXD[3:0] (Q[3:0])	Output (TTL, Three State)	Receive Data. RXD[3:0] are the data signals that carry the received Ethernet frame data from the PHY to the MAC on a nibble basis. RXD[3:0] are driven synchronous to RX_CLK. In PMA mode, these pins become the Q[3:0] pins used for transferring binary encoded 8B6T symbols from the PMA sublayer.
RX_DV	Output (TTL, Three State)	Receive Data Valid. When asserted HIGH, RX_DV indicates that the PHY is presenting recovered and decoded nibbles on the RXD[3:0] lines and that RX_CLK has been synchronized to the recovered data. RX_DV is first driven HIGH when RXD[3:0] contains the SFD and is held HIGH for the duration of the frame. RX_DV makes transitions synchronous to RX_CLK. In PMA Mode, RX_DV is driven high when Q2–3 contains the first data symbol.
RX_CLK	Output (TTL, Three State)	Receive Clock. RX_CLK is a continuous clock that provides a timing reference for the transfer of RXD[3:0], RX_DV, and RX_ER signals from the PHY to the MAC. When RX_DV is HIGH, RX_CLK is recovered from the received data. When RX_DV is LOW, RX_CLK is sourced from the PHY's nominal frequency. Transition between nominal frequency and recovered frequency is made while RX_DV is LOW. In 100-Mb/s mode, the nominal clock frequency is 25 MHz, and in 10-Mb/s the nominal frequency is 2.5 MHz.
RX_EN ^[1]	Input (TTL)	Receiver Output Enable. RX_EN enables the RXD[3:0], COL, Q5, RX_ER, and RX_DV signal drivers. RX_EN allows the receive data signals to be bussed together for multiple PHY applications.
RX_ER	Output (TTL, Three State)	Receive Error. RX_ER is asserted HIGH to indicate to the MAC that a fault condition was detected during the frame presently being transferred from the PHY to the MAC. RX_ER is driven synchronously with RX_CLK.
COL (Q4)	Output (TTL, Three State)	Collision Detect. COL is asserted HIGH to indicate that a collision has occurred on the media. COL is asserted asynchronously and with minimum delay from the start of the collision. In PMA Mode, this pin becomes the Q4 pin used for transferring binary encoded 8B6T symbols from the PMA sublayer.
CRS	Output (TTL, Three State)	Carrier Sense. CRS is asserted HIGH by the PHY to indicate the detection of a non-idle condition on the media. CRS is asserted asynchronously and with minimum delay from the detection of the non-idle condition. CRS is asserted HIGH throughout the duration of a collision condition.
MDC	Input (TTL)	Management Data Clock. MDC is sourced from the station management entity (STA) to the PHY as a timing reference for the transfer of management information on the MDIO signal.
MDIO	Bidirectional (TTL, Three State)	Management Data Input/Output. MDIO is a bidirectional signal between the PHY and the station management entity (STA) used to transfer control and status information. Control information is driven from STA to the PHY synchronously with MDC and sampled on the rising edge of MDC. The PHY drives status information to the STA synchronously with MDC. The STA samples the data on the rising edge of MDC.

Note:

1. RX_EN is not specified in the 802.3 MII standard.

Pin Descriptions (continued)
Media Dependent Interface

Name	I/O	Description
TX_D1+ TX_D1–	Differential Output	Transmit Data. TX_D1± are differential line drivers for data transmission. In 10BASE-T mode TX_D1± transmit Manchester encoded data with a nominal period of 100 ns. In 100BASE-T4 mode TX_D1± transmit 8B6T ternary symbols with a nominal period of 40 ns. TX_D1± also participate in the Link Integrity function.
RX_D2+ RX_D2–	Differential Input	Receive Data. RX_D2± are differential line receivers for data reception. In 100-Mb/s mode, RX_D2± receives 8B6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, RX_D2± receives Manchester encoded bits with a nominal period of 100ns. RX_D2± also participates in the Link Integrity function.
TX_D3+ TX_D3–	Differential Output	Transmit Data. TX_D3± are differential line drivers for data transmission. In 100-Mb/s mode, TX_D3± transmits 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, TX_D3± are not used.
RX_D3+ RX_D3–	Differential Input	Receive Data. RX_D3± are differential line receivers used for data reception. In 100-Mb/s mode, RX_D3± receives 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, RX_D3± are not used.
TX_D4+ TX_D4–	Differential Output	Transmit Data. TX_D4± are differential line drivers used for data transmission. In 100-Mb/s mode, TX_D4± transmits 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, TX_D4± are not used.
RX_D4+ RX_D4–	Differential Input	Receive Data. RX_D4± are differential line receivers used for data reception. In 100-Mb/s mode, RX_D4± receives 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, RX_D4± are not used.

Physical Media Attachment Interface

Name	I/O	Description
MODE	Input (TTL)	Mode. When MODE is tied HIGH, the transceiver is in normal mode. Received and transmitted data will move through the PMA and the PCS sublayers. Asserting MODE LOW exposes the 100BASE-T4 PMA service interface and disables 10BASE-T. The PCS is bypassed and the binary coded 6T serial data is presented at the MII and PMA interface pins.
D5	Input (TTL)	PMA Input Data. D5 is an input signal to the PMA transmit sublayer when MODE is asserted LOW.
Q5	Output (TTL, Three State)	PMA Output Data. Q5 is an output signal from the PMA receive sublayer when MODE is asserted LOW. Q5 is high-impedance when RX_EN is HIGH.

Control and Status

Name	I/O	Description
RESET	Input (TTL)	Reset. When RESET is asserted LOW, the PHY is placed in the reset state and the transmit and receive functions are disabled. The MII registers are placed in their default states.
AUTONEG	Input (TTL)	Auto-Negotiation Enable. When asserted HIGH, Auto-Negotiation capability is enabled by setting the Status Register bit 1.3. Auto-Negotiation is controlled through the MII management registers. When asserted LOW, Auto-Negotiation capability is disabled. AUTONEG is sampled on the rising edge of RESET.
ENT4	Input (TTL)	Enable 100BASE-T4. ENT4 enables 100BASE-T4 operation by setting the Status Register bit 1.15. When ENT4 is HIGH, bit 1.15 is forced HIGH, enabling 100BASE-T4 operation. When ENT4 is LOW, bit 1.15 is forced LOW, disabling 100BASE-T4. ENT4 is latched on the rising edge of RESET.
ENT	Input (TTL)	Enable 10BASE-T. ENT enables 10BASE-T operation by setting the Status Register bit 1.11. When ENT is HIGH, bit 1.11 is forced HIGH, enabling 10BASE-T operation. When ENT4 is LOW, bit 1.11 is forced LOW, disabling 10BASE-T. ENT is latched on the rising edge of RESET.
ENTFD	Input (TTL)	Enable 10BASE-T Full Duplex. ENTFD enables 10BASE-T Full Duplex operation by setting the Status Register bit 1.12. When ENTFD is HIGH, bit 1.12 is forced HIGH, enabling 10BASE-T Full Duplex operation. When ENTFD is LOW, bit 1.12 is forced LOW, disabling 10BASE-T Full Duplex. ENTFD is latched on the rising edge of RESET.
ISODEF	Input (TTL)	Isolate Default. ISODEF determines the default state of Isolate Bit 0.10 in the Control Register. When ISODEF is HIGH, the default value for 0.10 is 1. When ISODEF is LOW, the default value for 0.10 is 0. ISODEF is latched on the rising edge of RESET.
LOOP	Input (TTL)	Loopback Enable. When asserted LOW, the transmitter bit stream is looped back to the receiver for diagnostic testing. When LOOP is HIGH, the Loopback function is controlled by the Loopback bit in the control register.

Pin Descriptions (continued)
Control and Status (continued)

Name	I/O	Description
JAM	Input (TTL)	100BASE-T4 Jam Generation. When JAM is LOW in 100BASE-T4 mode and a carrier is present, the PHY will enter the collision state and generate the Jam pattern. The jam condition will persist for a minimum of 512 bit times.
TEST	Input (TTL)	Test. This pin is used for factory testing and should be tied LOW for normal operation.

Address

Name	I/O	Description
A[4:0]	Input (TTL)	PHY Address. These pins assign the management address to the PHY. A0 is least significant bit and A4 is the most significant bit. A4 is the first address bit received by the PHY in the management frame. The address is latched on the rising edge of RESET.

LED Drivers

Name	I/O	Description
LRX	Output (Open Drain, Weak Pull-Up)	Receive LED Indicator. LRX is driven LOW when the transceiver is receiving. An internal 20KΩ resistor will pull LRX HIGH when the transceiver is not receiving.
LTX	Output (Open Drain, Weak Pull-Up)	Transmit LED Indicator. LTX is driven LOW when the transceiver is transmitting. An internal 20KΩ resistor will pull LTX HIGH when the transceiver is not transmitting.
LINKT4	Output (Open Drain, Weak Pull-Up)	100BASE-T4 Link Pass LED Indicator. LINKT4 is driven LOW when the 100BASE-T4 transceiver is in the Link Pass State. An internal 20KΩ resistor will pull LINKT4 HIGH when the transceiver is not in the 100BASE-T4 Link Pass State.
LINKT	Output (Open Drain, Weak Pull-Up)	10BASE-T Link Pass LED Indicator. LINKT is driven LOW when the 10BASE-T transceiver is in the Link Pass State. An internal 20KΩ resistor will pull LINKT HIGH when the transceiver is not in the 100BASE-T Link Pass State.
LINKFD	Output (Open Drain, Weak Pull-Up)	10BASE-T Full Duplex Link Pass LED Indicator. LINKFD is driven LOW when 10BASE-T Full Duplex has been negotiated or chosen as the operating mode and the 10BASE-T transceiver is in the Link Pass State. An internal 20KΩ resistor will pull LINKFD HIGH when the transceiver is not in the 100BASE-T Link Pass State.

Clock

Name	I/O	Description
CLKI	Input	Reference Clock Input. In MII Mode (MODE=HIGH), the 25-MHz signal is used as a timing reference for TX_CLK and analog circuits. This pin should be connected to either to a 25-MHz crystal or a crystal-controlled TTL-level clock source. In PMA mode (MODE = LOW), CLKI is an input and is used as a timing reference for the PMA interface and analog circuits.
CLKO	Output	Reference Clock Output. This pin connects to a 25 MHz crystal or is left open if a TTL clock is used with CLKI. In PMA mode, CLKO should be left open.

External Components

Name	I/O	Description
R1	Passive	10K ±1% External resistor.
R2	Passive	10K ±1% External resistor.

Power and Ground

Name	I/O	Description
V _{CCD}	Digital Power	Positive Voltage Supply. V _{CC} requires a 5V±10% supply.
V _{CCA}	Analog Power	Positive Voltage Supply. V _{CC} requires a 5V±10% supply.
V _{CCS}	Serial MDI Power	Positive Voltage Supply. V _{CC} requires a 5V±10% supply.
GNDD	Digital Ground	Ground.
GNDA	Analog Ground	Ground.
GNDS	Serial MDI Ground	Ground.

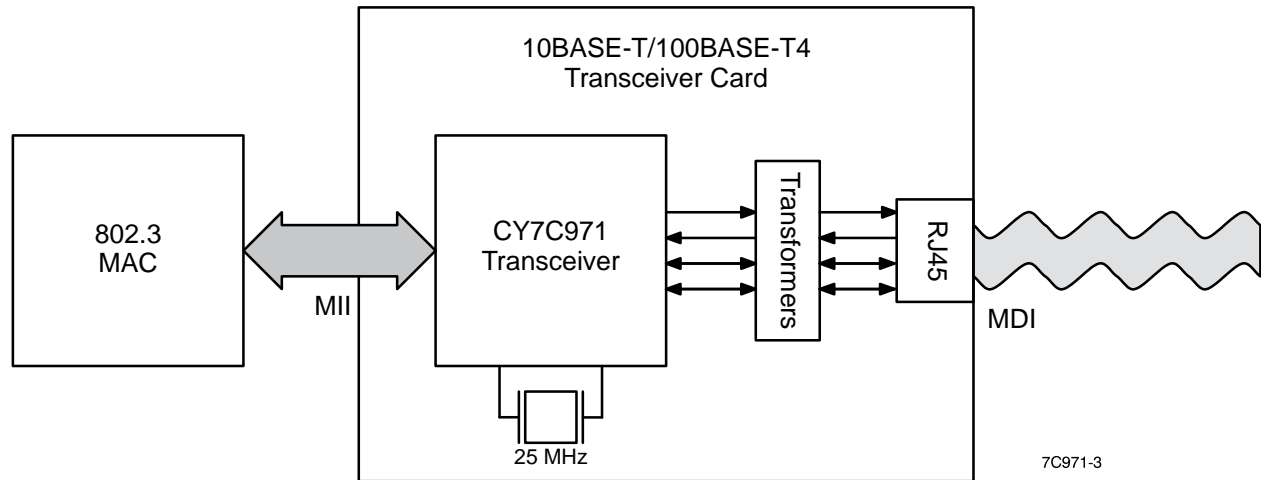


Figure 1. Transceiver Card Block Diagram

CY7C971 Description

100BASE-T4

The CY7C971 provides a physical layer interface (PHY) for dual speed IEEE 802.3 100BASE-T4 and 10BASE-T CSMA/CD local area networks. 100BASE-T4 offers increased performance over existing 10BASE-T networks while maintaining compatibility with the existing Ethernet Media Access Control (MAC) specification. The 100BASE-T4 PHY interfaces to 4 pairs of category 3, 4, or 5 cable. The 100BASE-T4 PHY is comprised of the Physical Coding Sublayer (PCS), Physical Media Attachment (PMA), Media Independent Interface (MII), and Media Dependent Interface (MDI). A typical 100BASE-T4 transceiver card application is shown in Figure 1.

Transmitter

The transmitter is comprised of the Physical Coding Sublayer (PCS) and the Physical Media Attachment (PMA). Figure 2 shows a block diagram of the T4 transmitter.

Transmit Physical Coding Sublayer (PCS)

The PCS takes nibble-wide data from the MII and accumulates them into 8-bit octets in the TXD1 and TXD2 registers. The octets are then encoded using the 8B6T ternary code according to the 802.3 standard. The encoded 8B6T code groups are then loaded in binary form to the shift registers.

Three shift registers convert the parallel 8B6T code groups to serial form. When the transmitter is active, a shift register is loaded on every other TX_CLK cycle. The first 8B6T code group of the frame is loaded into TX_shift1. The second group is loaded into TX_shift2 and the third into TX_shift3. The 4th group will be loaded into TX_shift1. This sequence continues until all of the 8B6T code groups comprising the frame have been transmitted.

At the start of the transmit frame, TX_shift2 and TX_shift3 will be loaded with a pad sequence aligned with first 8B6T code group in TX_shift1. The pad sequence aides the receiver with clock recovery and pair alignment. The preamble is generated automatically and follows the pad sequence.

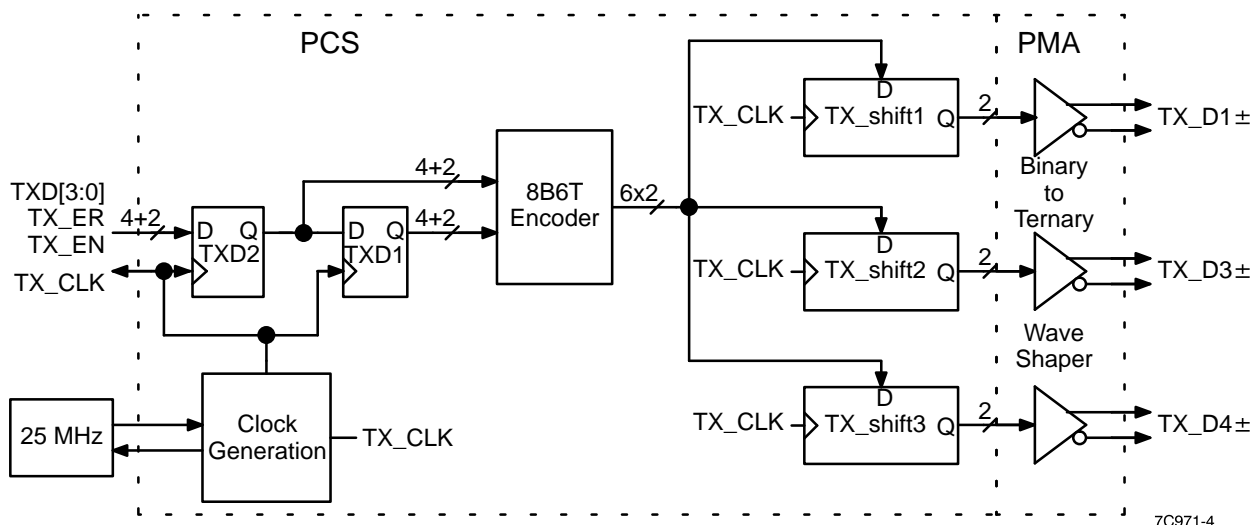


Figure 2. T4 Transmitter Block Diagram

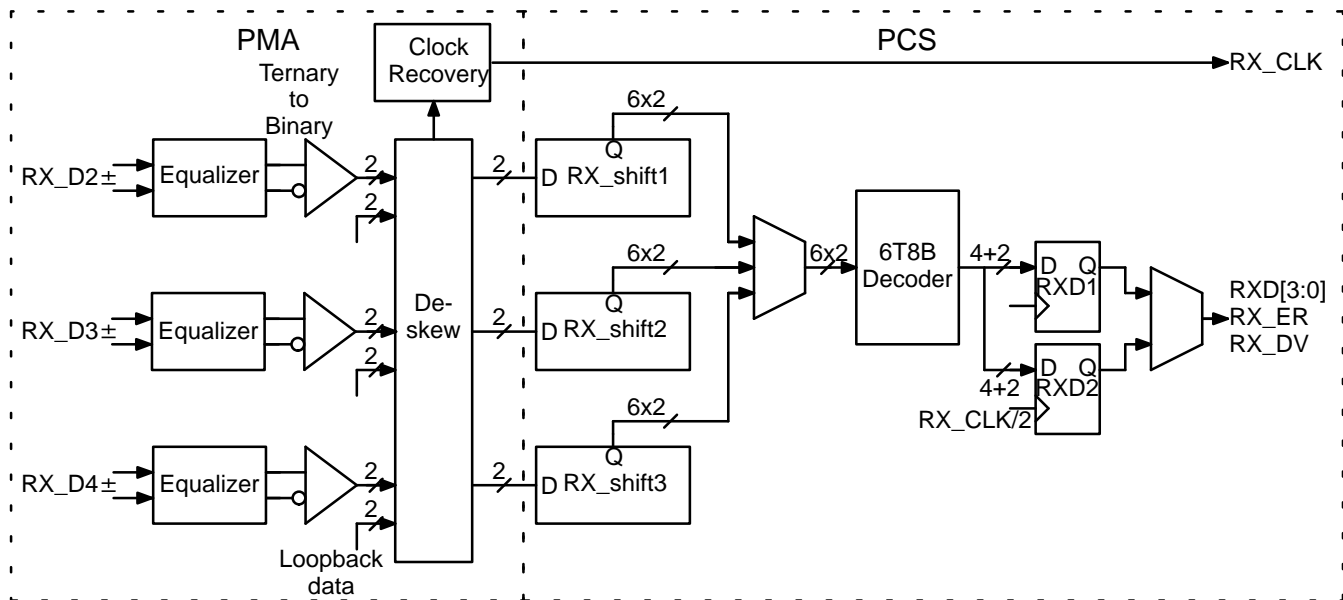


Figure 3. T4 Receiver Block Diagram

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Transmit Physical Media Attachment (PMA)

The Transmit PMA converts the serial encoded 6T bits from the transmit PCS to their corresponding ternary waveforms. The wave-shaper Digital to Analog Converter (DAC) generates high precision raised cosine waveforms on each transmission pair. The waveforms conform to the 100BASE-T4 output template specification. No external filters are required. The PMA output drives interface to the media through external termination resistors and isolation transformers.

Receiver

The T4 receiver is comprised of the PCS and the PMA. Figure 3 shows a block diagram of the receiver

Receive Physical Media Attachment (PMA)

The PMA receives serial 8B6T symbols from the twisted-pair interface and presents them to the PCS. The T4 receiver media interface features three adaptive equalizers. The equalizers compensate for the attenuation of high-frequency signals by up to 100 meters of category 3, 4, or 5 twisted-pair cable. The equalized waveforms are converted to binary form and passed to the clock recovery and data alignment blocks. The clock recovery circuit aligns the frequency and phase of RX_CLK with that of the received serial data. The data alignment block deskews the three receive channels.

Receive Physical Coding Sublayer (PCS)

The PCS accepts serial 8B6T symbols from the PMA, deserializes them, and then decodes the 8B6T code groups. Three shift registers convert the serial data back to parallel form. The first 8B6T code group is shifted into RX_shift1. The second 6T symbol group is shifted into RX_shift2 and the third into RX_shift3. The fourth code group is then shifted into RX_shift1. This process continues until the entire frame has been deserialized. The parallel 8B6T data are converted to 8-bit octets and latched into registers RXD1 and RXD2 on every other RX_CLK. The data is then presented at the MII interface in nibble form. RX_DV indicates that received data is present on the RXD[3:0] pins. RX_ER indicates that a receiver fault has occurred.

Carrier Sense

The carrier sense function detects activity on the media using a smart squelch function similar to 10BASE-T. The CRS signal is asserted HIGH when a valid carrier is detected on the pair RX_D2 according to the 10BASE-T4 draft standard. After detecting a valid carrier, an eop1 code group or seven consecutive zeros on RX_D2 must be detected before CRS is deasserted.

Collision Detection

A collision is detected when the transmitter is active simultaneously with the detection of a valid carrier by the carrier sense function. The MII COL signal will be asserted HIGH to signal the presence of a collision. When a collision is detected the TX_D2 and TX_D3 pair drivers turn off.

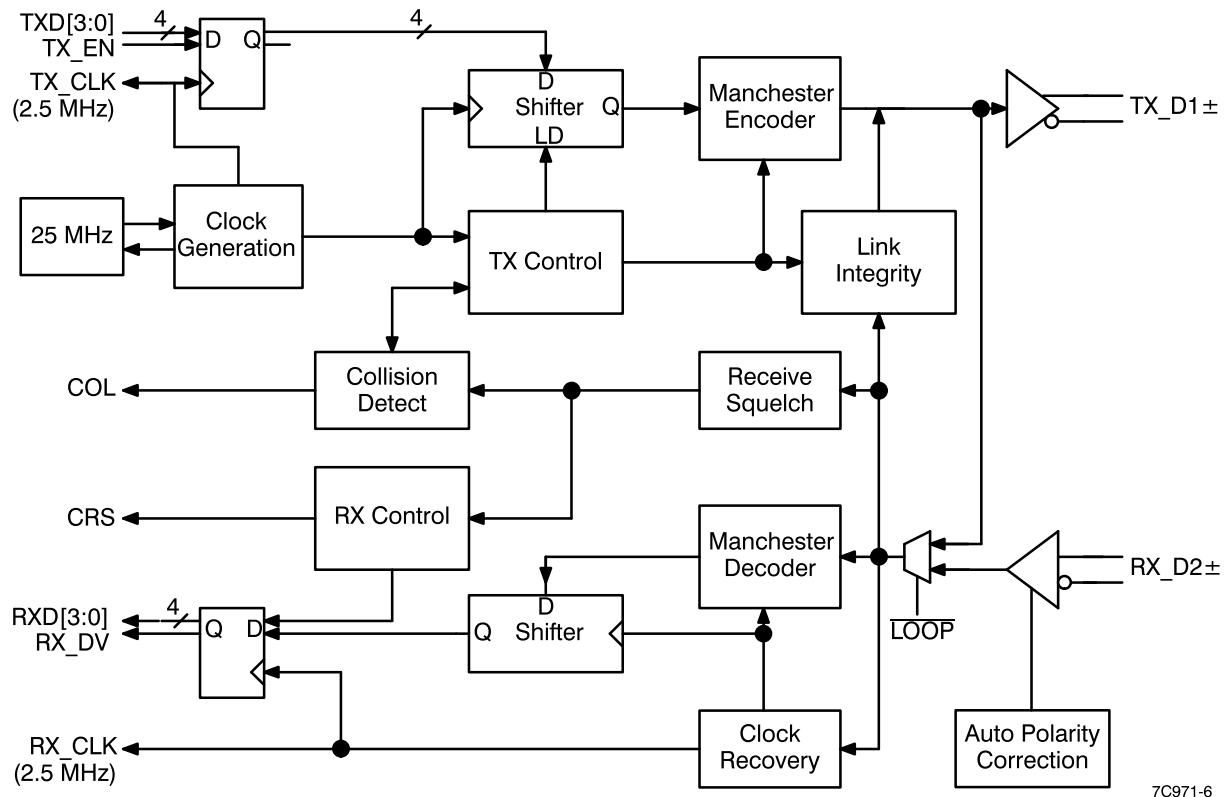
Auto-Polarity Correction

The Auto-Polarity Correction function monitors the received signal polarity on RX_D2± and inverts the received signal internally if its polarity is inverted. Auto-Polarity Correction is active during Auto-Negotiation and normal operation.

10BASE-T

The CY7C971 provides a 10BASE-T physical layer interface for compatibility with existing 10-Mb/s Ethernet networks. 10BASE-T operation is automatically selected if Auto-Negotiation established 10BASE-T as the highest common operating mode. The 10BASE-T transceiver can also be enabled manually by disabling Auto-Negotiation and clearing the Speed Selection (0.13) bit in the MII Control Register. The LINKT pin indicates when 10BASE-T is the selected mode of operation and the 10BASE-T transceiver is in the link pass state. Figure 4 shows a block diagram of the 10BASE-T transceiver.

During 10BASE-T operation, transmit and receive data are transferred over the MII interface in nibble wide groups. The TX_CLK and RX_CLK clocks are sourced from the PHY with a 2.5-MHz nominal clock rate. TX_EN qualifies incoming transmit data, and RX_DV qualifies receive data. In this mode, the MII complies with the IEEE MII specification for a 10-Mb/s interface.



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Figure 4. 10BASE-T Transmitter & Receiver Block Diagram

Full Duplex

The CY7C971 supports Full Duplex operation in 10BASE-T mode. 10BASE-T Full Duplex operation is automatically selected if Auto-Negotiation established 10BASE-T Full Duplex as the highest common operating mode. The 10BASE-T Full Duplex operation can also be selected manually by disabling Auto-Negotiation and clearing the Speed Selection (0.13) bit and setting the Duplex Mode Bit (0.8) in the MII Control Register. 10BASE-T Full Duplex mode cannot be enabled through Auto-Negotiation or manually unless the ENTDFD pin is HIGH. The LINKFD pin indicates when 10BASE-T Full Duplex is the selected mode of operation and the 10BASE-T transceiver is in the Link Pass State. During full duplex operation, the collision pin (COL) is LOW.

Auto-Polarity Correction

The Auto-Polarity Correction function monitors the received signal polarity on RX_D2± and inverts the received signal internally if its polarity is inverted. Auto-Polarity Correction is active during Auto-Negotiation and normal operation.

Media Independent Interface (MII)

The MII provides a connection between the PHY and the MAC and between the PHY and the station management (STA) entity. The MII is capable of supporting 100- and 10-Mb/s operation.

Data transfer is accomplished over nibble-wide dedicated transmit and receive channels. When TX_EN is asserted HIGH, data on TXD[3:0] channel is latched into the PHY on the rising edge of TX_CLK and passed to the PCS. If TX_ER is asserted HIGH, an 8B6T code violation word will be sent in place of the transmit data.

TX_CLK provides a continuous clock that is sourced from the PHY.

When recovered data is available from the PCS, the RX_DV signal is asserted HIGH simultaneously with the first Start of Frame Delimiter (SFD) nibble on RXD[3:0]. The RX_DV signal remains HIGH continuously through the final recovered nibble of the frame. If an error is detected in the frame by the PHY, the RX_ER signal is driven HIGH synchronously with RX_CLK.

RX_CLK is a continuous clock that provides a timing reference for the transfer of RXD[3:0], RX_DV, and RX_ER from the PHY to the MAC. RX_CLK is sourced from the PHY. While RX_DV is deasserted, RX_CLK will run at the PHY's nominal frequency. When RX_DV is asserted, the frequency and phase of RX_CLK is recovered from the received data. During the transition from nominal to recovered frequency, the period of RX_CLK may extend by up to one cycle. RX_CLK stretching prevents logic failures from occurring in downstream logic while the clock makes it transition.

When a carrier is detected, the CRS signal is asserted HIGH. A collision is signaled by asserting COL HIGH. CRS is asserted throughout a collision condition.

Access to the management facilities are provided through the MII with the MDC and MDIO pins. These pins provide a serial interface to the management control and status registers. The MDC signal is driven to the PHY from the management station (STA) as a timing reference for transfer of information on the MDIO signal. The MDIO signal is a bidirectional signal between the PHY and the STA. Control information is driven by the STA to the PHY. Status information is driven from the PHY to the STA.

Media Dependent Interface

The Media Interface is comprised of four communications channels. A dedicated transmit channel, TX_D1±, transmits 100BASE-T4 and 10BASE-T signals. RX_D2± is a dedicated receive channel for both 100BASE-T4 and 10BASE-T signals. The two bidirectional channels for 100BASE-T4 are formed from TX_D3±, RX_D3± and TX_D4±, RX_D4±.

The MDI pins interface to the medium through external resistors and isolation transformers. No external filters are required. The transmit drivers use class AB differential drivers to help reduce power consumption while providing ample drive capability. The drivers have a common mode control circuit to help reduce common mode emissions.

Management

The management facilities are used to control and indicate the status of the PHY resources. The management facilities and MII management interface is compliant with the IEEE 802.3 MII draft specification.

II Management Interface

The management facilities are accessed through the MII management pins MDC and MDIO. The management facilities respond to register accesses that match the PHY address. The PHY address is assigned with the A[4:0] pins. The value of these pins are latched into the internal PHY address register on the rising edge of RE-SET.

Register accesses are performed by transferring an opcode, address, and register number to the PHY management facility. If the address transferred matches the PHY address at the A0–A4 pins, the PHY responds to the access. During a read access, 16 bits of data from the selected register are transferred from the PHY to the STA on the MDIO pin. During a write, 16 bits of data are transferred from the STA to the PHY and written into the selected register.

Control and Status Registers

Control and status information are stored in two 16-bit registers. The Control register is assigned address 0 and the Status register is assigned address 1. *Table 1* shows a map of the Control register and *Table 2* shows the Status register.

Table 1. MII Control Register Definition^[2]

Control Register (Register 0)					
Bit(s)	Name	Setting	R/W	Default	Description
0.15	Reset	1 = PHY Reset 0 = Normal Operation	R/W S/C	0	Resets the status and control registers to their default states. Reset is self clearing.
0.14	Loopback	1 = Loopback Mode 0 = Normal Operation	R/W	0	Loopback connects the transmit data path to the receive data path.
0.13	Speed Selection	1 = 100 Mb/s 0 = 10 Mb/s	R/W	1	When Auto-Negotiation is disabled, Speed Select determines the speed of the PHY.
0.12	Auto Negotiation Enable	1 = Enable Auto-Negotiation 0 = Disable Auto-Negotiation	R/W	1	This bit enables the Auto-Negotiation function.
0.11	Power Down	1 = Power Down 0 = Normal operation	R/W	0	Power down shuts off the internal PLLs and core logic.
0.10	Isolate ^[3]	1 = Isolate PHY from MII 0 = Normal Operation	R/W	0, 1	Isolate places the receiver MII channel in high impedance, and the MII transmitter channel does not respond to MII activity.
0.9	RestartAuto-Negotiation	1 = Restart Auto-Negotiation 0 = Normal Operation	R/W S/C	0	Restart Auto-Negotiation breaks the link and restarts the Auto Negotiation process.
0.8	Duplex Mode	1 = Full Duplex 0 = Half Duplex	R/W	0	Duplex Mode selects between full and half duplex operation for 10BASE-T.
0.7	Collision Test	1 = Test COL Signal 0 = Normal Operation	R/W	0	Collision test causes the COL signal to be asserted when TX_EN is asserted.
0.6:0	Reserved			0	

Notes:

- R/W = Read/Write
SC = Self Cleaning
RO = Read Only
LH = Latched HIGH
- Isolate default is set by the ISODEF pin.

Table 2. MII Status Register Definition

Status Register (Register 1)					
Bit(s)	Name	Setting	R/W	Default	Description
1.15 ^[4]	100BASE-T4	1 = 100BASE-T4 Able 0 = 100BASE-T4 Able	RO	1,0	When set, this bit indicates that the PHY is 100BASE-T4 capable.
1.14	100BASE-TX Full Duplex	0 = 100BASE-TX Full Duplex Not Supported	RO	0	This bit is always set to zero.
1.13	100BASE-TX Half Duplex	0 = 100BASE-TX Half Duplex Not Supported	RO	0	This bit is always set to zero.
1.12 ^[5]	10BASE-T Full Duplex	1 = 10BASE-T Full Duplex Able 0 = 10BASE-T Full Duplex Able	RO	1,0	When set, this bit indicates that the PHY is 10BASE-T full duplex capable.
1.11 ^[6]	10BASE-T Half Duplex	1 = 10BASE-T Half Duplex Able 0 = 10BASE-T Half Duplex Able	RO	1,0	When set, this bit indicates that the PHY is 10BASE-T half duplex capable.
1.10:6	Reserved	0 = Default	RO	0	
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation Complete 0 = Auto-Negotiation Incomplete	RO	0	This bit is set when NWAY has completed the auto negotiation process.
1.4	Remote Fault	1 = Remote Fault Condition 0 = No Remote Fault Condition	RO	0	This bit is set when Auto Negotiation detects a remote fault.
1.3 ^[7]	Auto Negotiation Ability	1 = PHY is Able to Perform Auto Negotiation	RO	1,0	PHY supports Auto-Negotiation.
1.2	Link Status	1 = Link Is Up 0 = Link Is Down	RO	0	Link Status indicates that the PHY is in the Link Pass State.
1.1	Jabber Detect	1 = Jabber Condition Detected 0 = No Jabber Condition Detected	RO LH	0	Jabber Detect indicates that a jabber condition has been detected for 10BASE-T.
1.0	Extended Capabilities	1 = Extended Register Capable	RO	1	OUI and Auto-Negotiation Extended Registers 2–7 are present.

Vendor and Product ID Registers

Vendor and Product identification codes are stored in management ID registers 2 and 3. These registers contain the Cypress Semiconductor Corporation unique identifier and the CY7C971 product and revision number. *Table 3* explains the ID registers.

Auto-Negotiation Registers

The Auto-Negotiation process is managed through the Auto-Negotiation registers. Register 4 is the Auto-Negotiation Advertisement register. This register contains the 16-bit code word that is advertised to the remote link partner. Register 5 is the Auto-Negotiation Link Partner Ability register for base and next pages. This register holds the 16-bit code word that the Auto-Negotiation function receives from the remote link partner. Register 6 is the Auto-Negotiation Expansion register and is used to monitor the negotiation process. Register 7 is the Auto-Negotiation Next Page Transmit register. The function of the Auto-Negotiation register bits are defined in *Tables 4* through *7*.

Auto-Negotiation

The IEEE Auto-Negotiation function provides remote capability detection and automatic speed selection. Auto-Negotiation is fully compatible with existing 10BASE-T only devices.

Notes:

4. 100BASE-T4 Default is set by the ENT4 pin.
5. 10BASE-T FD Default is set by the ENT4 pin.

Auto-Negotiation advertises the capabilities of the PHY by transmitting a sequence of fast link pulses (FLPs) that form a standard 16-bit code word. The advertised code word is contained in the Auto-Negotiation Advertisement register (Register 4). Auto-Negotiation receives 16-bit code words and stores them in the Auto-Negotiation Partner Ability register (Register 5). Once the code words have been sent and acknowledged, Auto-Negotiation selects the highest common operating mode as the current mode of operation. The highest common mode of operation is determined by the Priority Resolution Table specified in the Auto-Negotiation standard. When a mode of operation is selected, Auto-Negotiation enables the transition to the selected mode's Link Pass state.

The Auto-Negotiation process is controlled and monitored through the MII management registers. Auto-Negotiation may be disabled in the MII control register or by asserting the AUTONEG pin HIGH.

The Auto-Negotiation is capable of transmitting and receiving code word pages in addition to the base pages. The next page process is controlled through the MII registers.

6. 10BASE-T HD Default is set by the ENT pin.
7. Auto-Negotiation Default is set by the AUTONEG pin.

Table 3. MII PHY ID Register Definition

PHY Identifier (Register 2 and 3)					
Bit(s)	Name	Setting	R/W	Default	Description
2.15:0	OUI PHY Identifier	16 Most Significant OUI Bits	RO	0028h	This field contains 16 bits of the Cypress Organizationally Unique Identifier (OUI).
3.15:10	OUI PHY Identifier	6 Least Significant OUI Bits	RO	02h	This field contains 6 bits of the Cypress Organizationally Unique Identifier (OUI).
3.9:4	Model Number	CY7C971 Model Number	RO	01h	This field contains a 6-bit model number.
3.3:0	Revision Number	CY7C971 Revision Number	RO	–	This field contains a 4-bit revision number.

Table 4. MII Auto-Negotiation Advertisement Register Definition

Auto-Negotiation Advertisement Register (Register 4)					
Bit(s)	Name	Setting	R/W	Default	Description
4.15	Next Page	1 = Next Page to be Transmitted 0 = No Next Page	R/W	0	When set, this bit will cause the PHY to advertise Next Page capability.
4.14	Reserved		RO	0	Reserved.
4.13	Remote Fault	1 = Fault Indication 0 = No Fault	R/W	0	When set, this bit will cause the PHY to advertise a Remote Fault has occurred.
4.12	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
4.11	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
4.10	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
4.9 ^[8]	Technology Ability Field 100BASE-T4	1 = Advertise 100BASE-T4 0 = Do Not Advertise	R/W	1,0	When set, this bit will cause the PHY to advertise 100BASE-T4 capability. This bit may only be set if 100BASE-T4 is enabled.
4.8	Technology Ability Field 100BASE-TX Full Duplex	0 = 100BASE-TX FD Not Supported	RO	0	This bit will always be zero. 100BASE-TX FD is not supported.
4.7	Technology Ability Field 100BASE-TX	0 = 100BASE-TX Not Supported	RO	0	This bit will always be zero. 100BASE-TX is not supported.
4.6 ^[9]	Technology Ability Field 10BASE-T Full Duplex	1 = Advertise 10BASE-T FD 0 = Do Not Advertise	R/W	1,0	When set, this bit will cause the PHY to advertise 10BASE-T FD capability. This bit may only be set if 10BASE-T FD is enabled.
4.5 ^[10]	Technology Ability Field 10BASE-T	1 = Advertise 10BASE-T 0 = Do Not Advertise	R/W	1,0	When set, this bit will cause the PHY to advertise 10BASE-T capability. This bit may only be set if 10BASE-T is enabled.
4.4:0	Selector Field	Indicates IEEE 802.3 LAN	RO	01h	This field is permanently set to 0001 to advertise IEEE 802.3 CSMA/CD LAN.

Notes:

8. 100BASE-T4 Advertised Ability default is set by the ENT4 pin.
9. 10BASE-T FD Advertised Ability default is set by the ENT4 pin.
10. 10BASE-T Advertised Ability default is set by the ENT pin.

Table 5. MII Auto-Negotiation Link Partner Ability Register Definition

Auto-Negotiation Link Partner Ability Register (Register 5)					
Bit(s)	Name	Setting	R/W	Default	Description
5.15	Remote Next Page	1 = Next Page to be Transmitted 0 = No Next Page	RO	0	When set, this bit indicates the remote PHY has a Next Page to send.
5.14	Remote Acknowledge	1 = Remote Acknowledge 0 = No Acknowledge	RO	0	When set, this bit indicates that the remote PHY has acknowledged receipt of a page.
5.13	Remote Fault	1 = Fault Indication 0 = No Fault	RO	0	When set, this bit indicates that a fault has occurred in the remote PHY.
5.12	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
5.11	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
5.10	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
5.9	Technology Ability Field 100BASE-T4	1 = 100BASE-T4 Able 0 = Not 100BASE-T4 Able	RO	0	When set, this bit indicates that the remote PHY has 100BASE-T4 capability.
5.8	Technology Ability Field 100BASE-TX Full Duplex	1 = 100BASE-TX FD Able 0 = Not 100BASE-TX FD Able	RO	0	When set, this bit indicates that the remote PHY has 100BASE-TX FD capability.
5.7	Technology Ability Field 100BASE-TX	1 = 100BASE-TX Able 0 = Not 00Base-TX Able	RO	0	When set, this bit indicates that the remote PHY has 100BASE-TX capability.
5.6	Technology Ability Field 10BASE-T Full Duplex	1 = 10BASE-T FD Able 0 = Not 10BASE-T Able	RO	0	When set, this bit indicates that the remote PHY has 10BASE-T FD capability.
5.5	Technology Ability Field 10BASE-T	1 = 10BASE-T Able 0 = Not 10BASE-T Able	RO	0	When set, this bit indicates that the remote PHY has 10BASE-T capability.
5.4:0	Selector Field	Indicates LAN Type	RO	00h	This field indicates the type of LANs being advertised by the remote PHY.

Table 6. MII Auto-Negotiation Expansion Register Definition

Auto Negotiation Expansion Register (Register 6)					
Bit(s)	Name	Setting	R/W	Default	Description
6.15:5	Reserved	Reserved	RO	0	Reserved.
6.4	Parallel Detection Fault	1 = Parallel Detection Fault 0 = No Parallel Detection Fault	RO LH	0	When set, this bit indicates that local Auto-Negotiation has detected more than one valid link.
6.3	Link Partner Next Page Able	1 = Link Partner is Next Page Able 0 = Link Partner is Not Next Page Able	RO	0	When set, this bit indicates that the remote PHY supports Next Page capability
6.2	Next Page Able	1 = Next Page Able	RO	1	This bit indicates that local Auto-Negotiation supports Next Page capability.
6.1	Page Received	1 = 3 Identical Code Words Received 0 = 3 Identical Code Words Have Not Been Received	RO LH	0	When set, this bit indicates that local Auto-Negotiation has received three consecutive and identical code words.
6.0	Link Partner Auto Negotiation Able	1 = Link Partner is Auto-Negotiation Able 0 = Link Partner is Not Auto-Negotiation Able	RO	0	When set, this bit indicates that the remote PHY has Auto-Negotiation capability.

Table 7. MII Auto-Negotiation Next Page Transmit Register Definition

Auto-Negotiation Next Page Transmit Register (Register 7)					
Bit(s)	Name	Setting	R/W	Default	Description
7.15	Next page	1 = More Pages Follow 0 = Last Page	R/W	0	When set, this bit indicates that more pages follow. When clear, it indicates that the last page is being sent.
7.14	Reserved		RO	0	
7.13	Message Page	1 = Message Page 0 = Unformatted Page	R/W	0	When set, this bit indicates that the next page being sent is formatted as a message page.
7.12	Acknowledge 2	1 = Will Comply 0 = Cannot Comply	RO	1	When set, this bit indicates that the device can comply with the received message.
7.11	Toggle	1 = Previous Toggle Was Zero 0 = Previous Toggle Was One	RO	0	This bit is used to ensure synchronization with the link partner during next page exchange.
7.10:0	Message/Unformatted Code Field	Eleven-Bit Field	R/W	000h	This field contains the message/unformatted bits for the next page.

Loopback

In Loopback Mode, the transmit PMA circuits are isolated from the media and are connected to the receive PMA circuits. Transmit data flows from the MII through the PCS and into the PMA. The serial data is then looped back through the Receiver PMA and PCS to the MII interface. Loopback Mode is useful for checking the integrity of the PHY and MAC operations.

Loopback Mode is enabled by either setting the Loopback bit in the Management Control register to one or by asserting the **LOOP** pin LOW.

PMA Mode

When the **MODE** pin is LOW, the CY7C971 is in 100BASE-T4 PMA mode. This mode of operation is intended for use in repeater applications. In PMA mode, the PCS is bypassed exposing the PMA sublayer. Binary encoded 6T symbols are transferred directly over the PMA interface pins. This reduces the transmitter latency for use in class 1 and class 2 repeaters. A block diagram of the PMA interface is shown in *Figure 5*. 10BASE-T is disabled in the Status register.

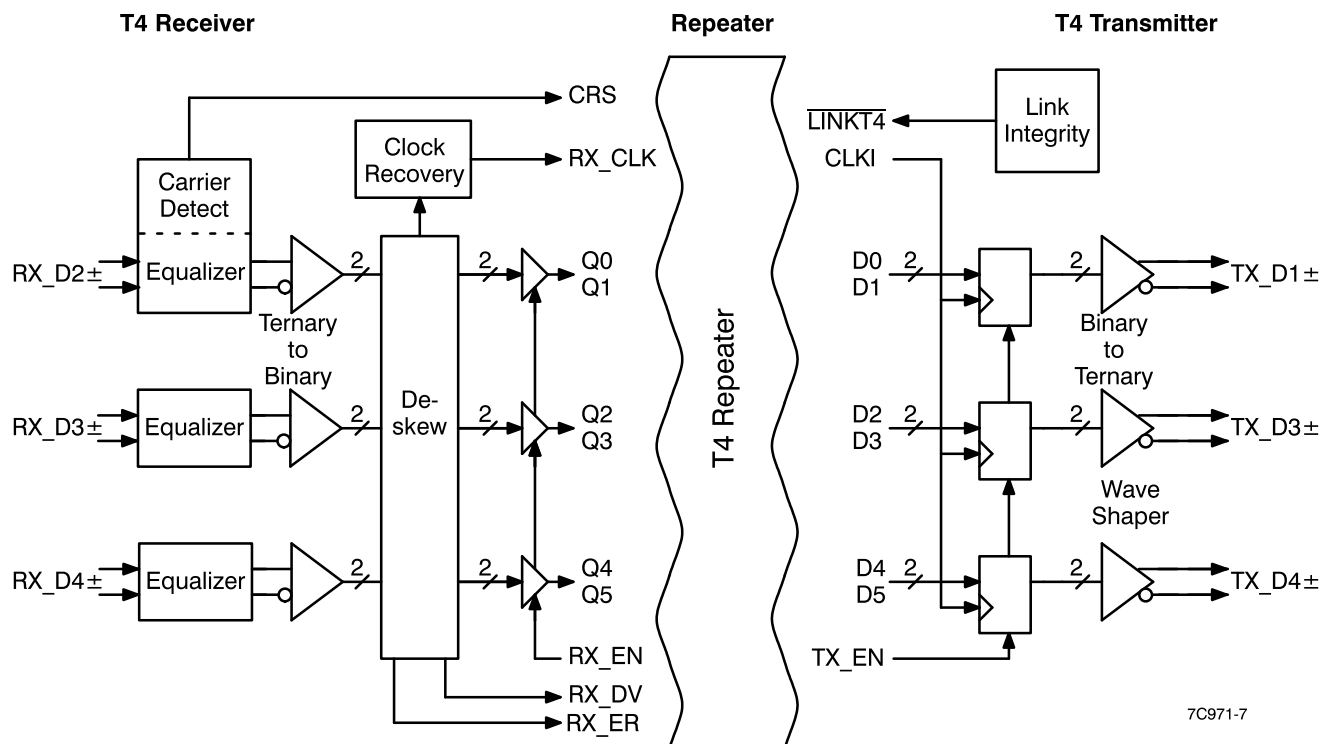


Figure 5. T4 Transmitter & Receiver PMA Interface and Block Diagram (MODE = LOW)

Serial 6T data from the three PMA circuits are transferred over the PMA interface pins in binary form. The Receiver aligns and converts the line signals to their 6T binary representation and drives them to the Q[5:0] pins. The transmitter latches the three 6T symbol streams on its D[5:0] input pins on the rising edge of TX_CLK. The 6T symbols are loaded into the waveshaper DAC and converted to their corresponding ternary waveforms. *Table 8* shows the mapping of binary PMA signals to ternary waveforms.

Table 8. PMA Binary to Ternary Map^[11]

PMA Q1-0, Q3-2, Q5-4 D1-0, D3-2, D5-4	Transmitter	Receiver
00	CS0	CS0
10	CS1	CS1
01	CS-1	CS-1
11	CS0	—

Notes:

11. CS0 is a waveform which conveys the ternary symbol 0.
 CS1 is a waveform which conveys the ternary symbol 1.
 CS-1 is a waveform which conveys the ternary symbol -1.

The RX_DV signal indicates when the first data symbol after sosb is present on the Q0-5 PMA interface pins. RX_DV will remain HIGH throughout the transfer of data symbols across the PMA interface. RX_DV is LOW when there is no carrier present. RX_ER HIGH indicates a pair alignment error. The RX_EN input pin enables the Q0-5, RX_DV, and RX_ER drivers. RX_EN LOW places the drivers in the high-impedance state.

The transmit PMA interface is synchronous to the CLKI input clock signal. The TX_EN HIGH causes data on the PMA D0-5 pins to be loaded into the transmit PMA waveshaper on the rising edge of CLKI. When TX_EN is LOW, the output drivers transmit the CS0 idle symbols.

Applications

The CY7C971 is a flexible physical-layer device that fits into any Ethernet application including network interface cards, transceiver cards, repeaters, hubs and switches. *Figure 6* shows a schematic of the CY7C971 configured for a transceiver card application with an exposed MII port.

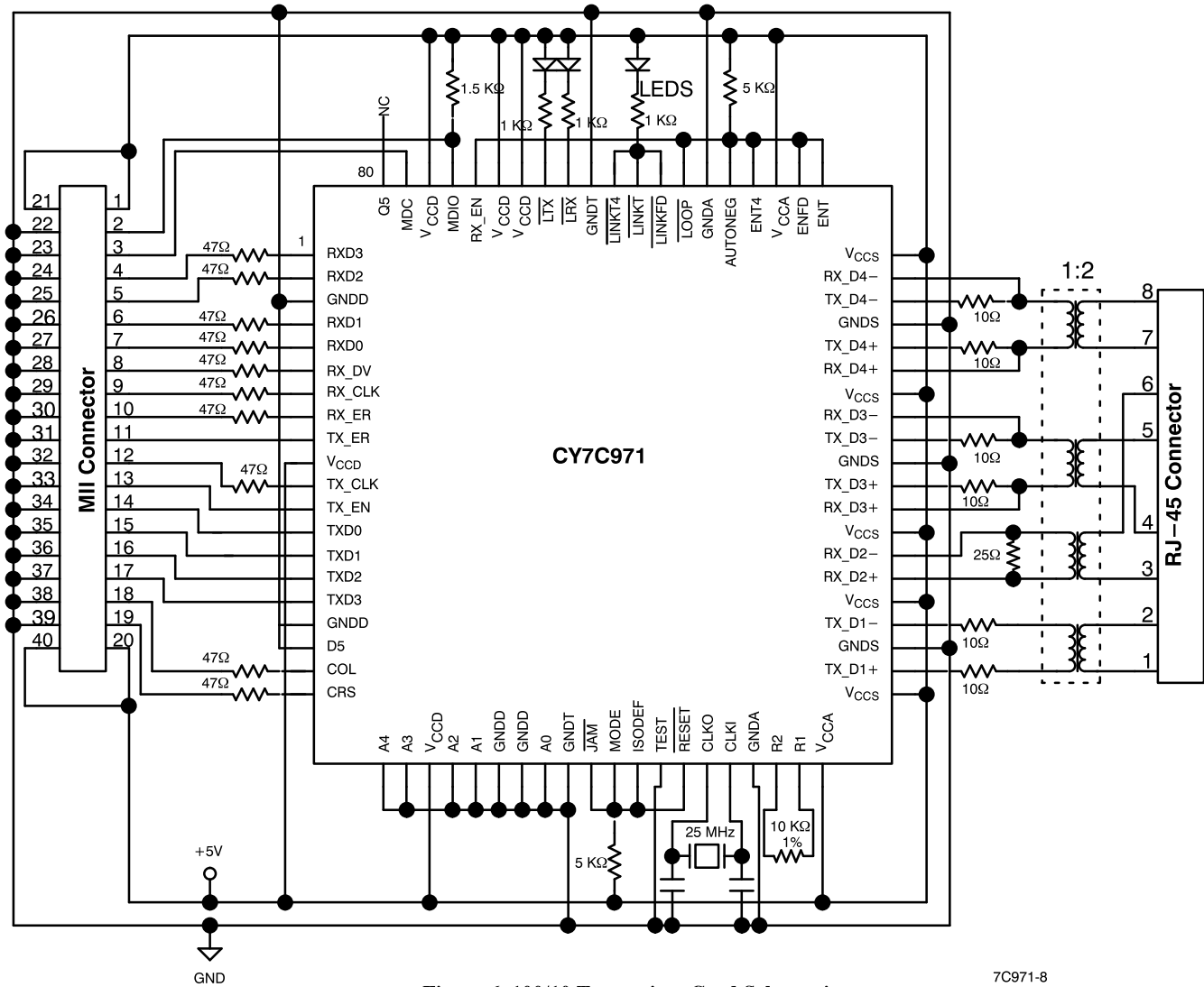


Figure 6. 100/10 Transceiver Card Schematic

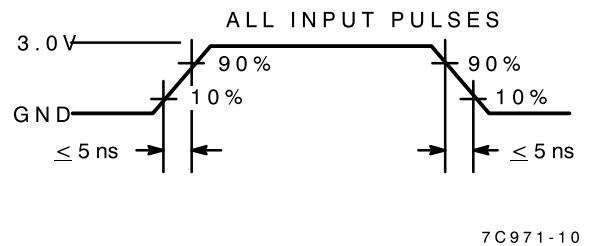
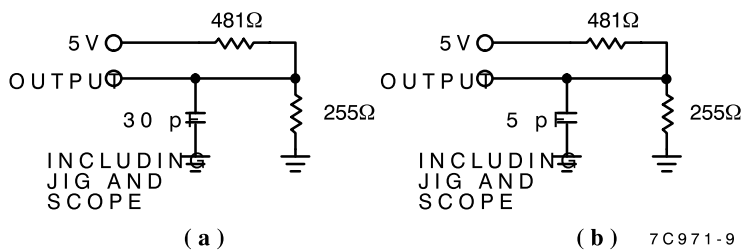
7C971-8

Electrical Characteristics Over the Operating Range

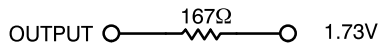
Parameter	Description	Test Conditions	Min.	Max.	Unit
TTL Pins					
V _{OHT}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		V
V _{OLT}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 4.0 mA		0.4	V
V _{IHT}	Input HIGH Voltage		2.0	6.0	V
V _{ILT}	Input LOW Voltage		-3.0	0.8	V
I _{IXT}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	μA
I _{OZT}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-50	+50	μA
I _{OST}	Output Short Circuit Current ^[12]	V _{CC} = Max., V _{OUT} = GND		-350	mA
Open Drain LED Pins					
V _{OLD}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12.0 mA		0.4	V
Miscellaneous					
I _{CC1}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, 100BASE-T4 transmitting		300	mA
I _{CC2}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, 100BASE-T4 not transmitting		100	mA
I _{SB}	Power-Down Current	Max. V _{CC}		TBD	mA

Capacitance^[13]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	5	pF
C _{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT


Notes:

12. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
13. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range^[14]

Parameter	Description	Min.	Max.	Unit
MII Timing				
t _{TCPWHT4}	TX_CLK Pulse Width HIGH (T4)	14	26	ns
t _{TCPWLT4}	TX_CLK Pulse Width LOW (T4)	14	26	ns
t _{TCPWHT}	TX_CLK Pulse Width HIGH (T)	194	206	ns
t _{TCPWLT}	TX_CLK Pulse Width LOW (T)	194	206	ns
t _{TDS}	TXD Set Up	10		ns
t _{TDH}	TXD Hold	0		ns
t _{TMIIT4}	Transmit Latency (T4)		110	ns
t _{TMIIT}	Transmit Latency (T)		500	ns
t _{TCSHT4}	Transmit Path CRS Assert (T4)		20	ns
t _{TCSHT}	Transmit Path CRS Assert (T)		20	ns
t _{TCSLT4}	Transmit Path CRS Deassert (T4)		320	ns
t _{TCSLT}	Transmit Path CRS Deassert (T)		100	ns
t _{RCPWHT4} ^[15]	RX_CLK Pulse Width HIGH	14	26	ns
t _{RCPWLT4} ^[15]	RX_CLK Pulse Width LOW	14	26	ns
t _{RCPWHT} ^[15]	RX_CLK Pulse Width HIGH	194	206	ns
t _{RCPWLT} ^[15]	RX_CLK Pulse Width LOW	194	206	ns
t _{RDV}	RXD Valid from Clock		18	ns
t _{RDH}	RXD Hold from Clock	10		ns
t _{RXDVT4}	RXD Valid Latency (T4)		870	ns
t _{RXDVT}	RXD Valid Latency (T)		500	ns
t _{RXDATAT4}	RXD Latency (T4)		950	ns
t _{RXDATAT}	RXD Latency (T)		8700	ns
t _{RHZD}	RX_EN HIGH to Valid Data		15	ns
t _{RDHZ}	RX_EN LOW to High Impedance		20	ns
100BASE-T4 CRS and COL				
t _{CRSH} ^[16]	CRS Assert Latency for Preamble	110	140	ns
t _{CRSLC} ^[17]	CRS Deassert Latency for EOC		370	ns
t _{CRSLE} ^[18]	CRS Deassert Latency for EOP		370	ns
t _{COLH1} ^[19]	COL Assert Latency from TX_EN HIGH		20	ns
t _{COLL1} ^[20]	COL Deassert Latency from TX_EN LOW		20	ns
t _{COLH2} ^[21]	COL Assert Latency from Preamble		190	ns
t _{COLL2} ^[22]	COL Deassert Latency from EOC or EOP		370	ns

Notes:

14. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
15. During clock transition, clock max time could be as long as an entire cycle.
16. t_{CRSH} is measured from the rising edge of the latest arriving signal of the three pair that meets the 100BASE-T4 squelch criterion to the rising edge of CRS. The rising and falling edges of CRS are guaranteed to meet the fairness timing specification defined in the 100BASE-T4 standard.
17. t_{CRSLC} is measured from the end of the last data symbol on RX_D2 to the falling edge on CRS. Seven consecutive zeros must be received on RX_D2 in order for the PMA to recognize loss of carrier.
18. t_{CRSLE} is measured from the beginning of the first symbol of EOP1 on any RX_Dx MDI pair accounting for skew to the falling edge on CRS. Detection of a properly framed EOP1 will cause the PCS to recognize loss of carrier.
19. t_{COLH1} is measured from the rising edge of TX_CLK while TX_EN is HIGH to the rising edge of COL.
20. t_{COLL1} is measured from the rising edge of TX_CLK while TX_EN is LOW to the falling edge of COL.
21. t_{COLH2} is measured from the rising edge of the signal on RX_D2 that meets the 100BASE-T4 unsquelch criterion to the rising edge of COL.
22. t_{COLL2} is measured from the first symbol of the EOP or EOC sequences to the falling edge of COL.

Switching Characteristics Over the Operating Range (continued)

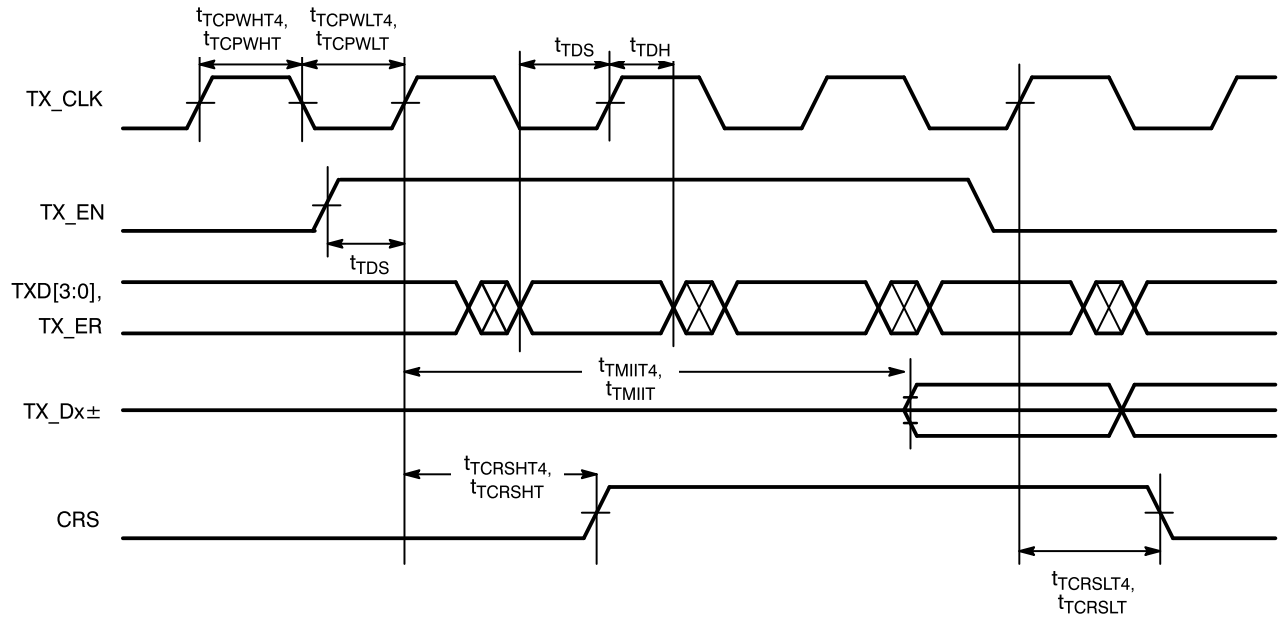
Parameter	Description	Min.	Max.	Unit
10BASE-T CRS and COL				
$t_{\text{CRSH3}}^{[23]}$	CRS Assert Latency		500	ns
$t_{\text{CRSL3}}^{[24]}$	CRS Deassert Latency		500	ns
Management Timing				
t_{MCPWH}	MDC Pulse Width HIGH	25		ns
t_{MCPWL}	MDC Pulse Width LOW	25		ns
f_{M}	MDC Frequency		12.5	MHz
t_{MDS}	MDIO Set-Up	10		ns
t_{MDH}	MDIO Hold	0		ns
t_{MDO}	MDIO Valid from Clock		40	ns
t_{MDOH}	MDIO Hold from Clock	0		ns
t_{MDHZ}	MDC to High Impedance		40	ns
t_{MDLZ}	MDC to Low Impedance	0	20	ns
Control and Status Timing				
t_{RL}	Reset Pulse Width LOW	5		μs
t_{RS}	Control Input Set-Up	100		ns
PMA Interface Timing				
t_{TPMA}	PMA Transmit Latency		40	ns
t_{TDS}	PMA Transmit Data Set Up	10		ns
t_{TDH}	PMA Transmit Data Hold	0		ns
t_{PMACRSH}	PMA CRS Assert Latency	110	140	ns
t_{PMACRSL}	PMA CRS Deassert Latency		650	ns
t_{PMADATA}	PMA Receiver Data Latency		800	ns
Clock Timing				
t_{CPWH}	Reference Clock Pulse Width HIGH	16	24	ns
t_{CPWL}	Reference Clock Pulse Width LOW	16	24	ns
f_{C}	Reference Clock Frequency	25 – 100 ppm	25 + 100 ppm	MHz

Notes:

23. t_{CRSH3} is measured from the rising edge of the signal on RX_D2 that meets the 10BASE-T carrier criterion to the rising edge of CRS.
24. t_{CRSL3} is measured from the end of the last data symbol on RX_D2 to the falling edge of CRS.

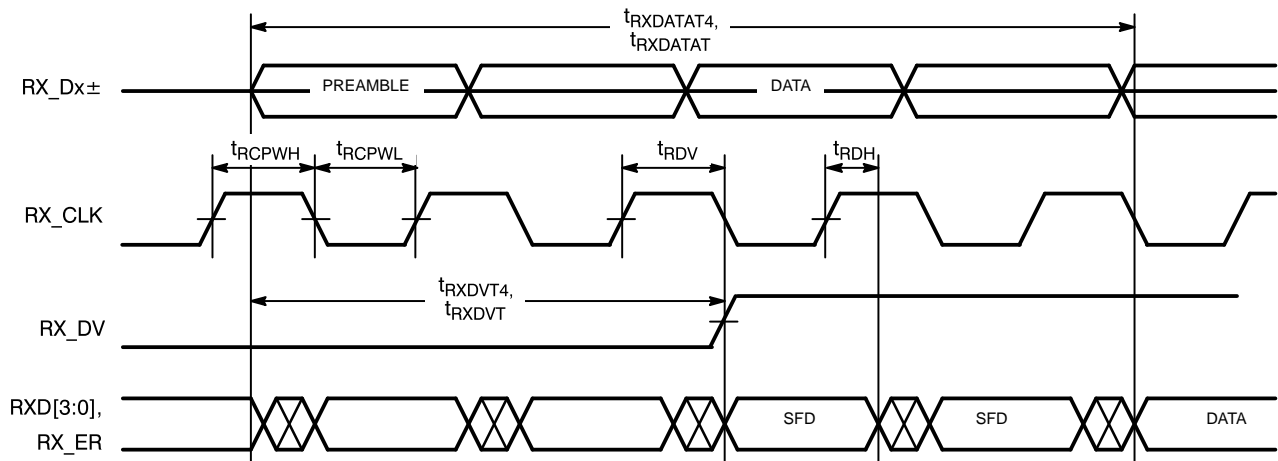
Switching Waveforms

MII Transmit Port Data Timing^[25]



7C971-11

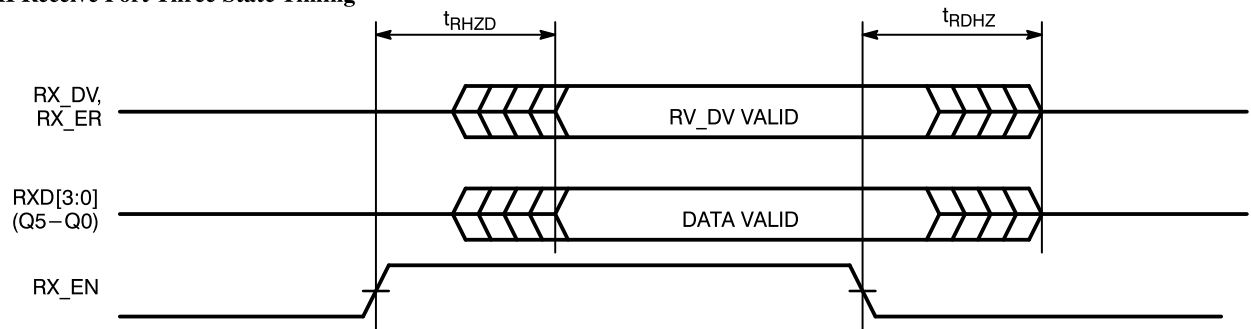
MII Receive Port Data Timing^[26, 27]



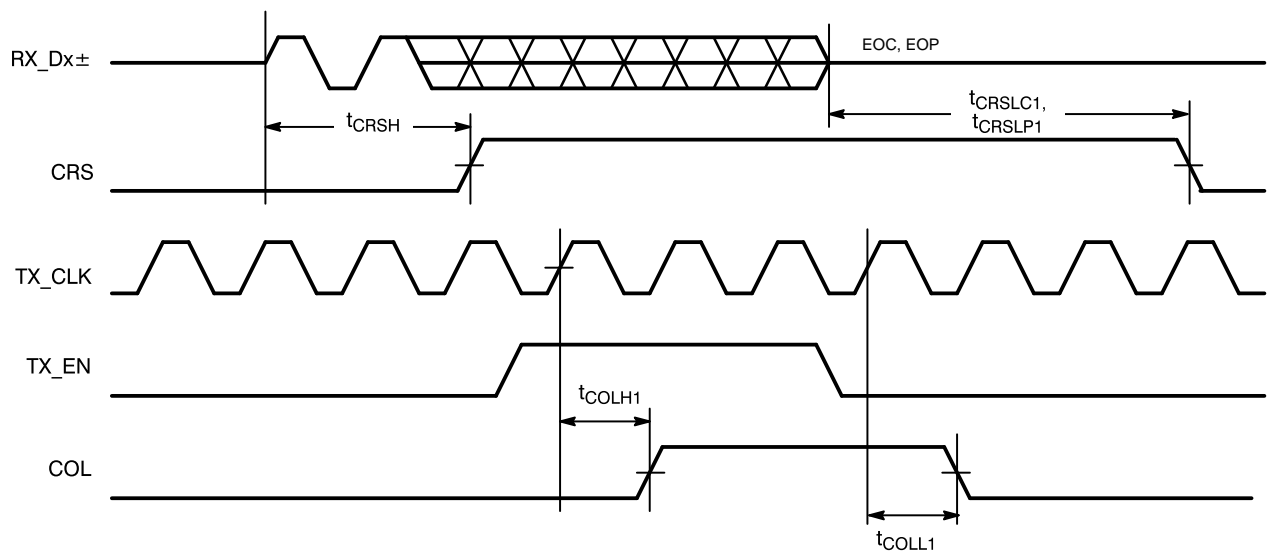
7C971-12

Notes:

25. t_{MI} is measured from the rising edge of TX_CLK to the 50% point of the TX_Dx± outputs at the MDI pins.
26. t_{RXDV} is measured from the first rising edge of the preamble at the MDI input pins to the rising edge of RX_DV. This includes up to 64 bits of preamble and SFD plus the latency of the receive circuitry.
27. t_{RXDATA} is measured from the first rising edge of the preamble at the MDI input pins to the rising edge of valid data at the RXD pins. This includes up to 64 bits of preamble and SFD plus the first 8 bits of data and the latency of the receive circuitry.

Switching Waveforms (continued)
MII Receive Port Three State Timing


7C971-13

MII Carrier Sense and Collision (100BASE-T4)


7C971-14



MII Carrier Sense and Collision (100BASE-T4)

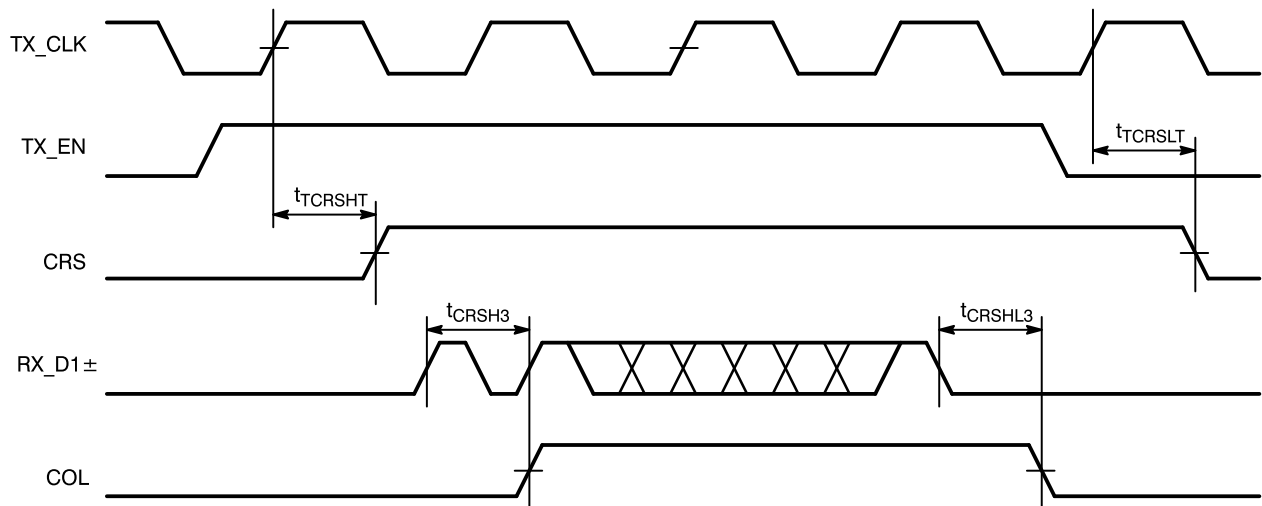


MII Carrier Sense and Collision (10BASE-T) [28]

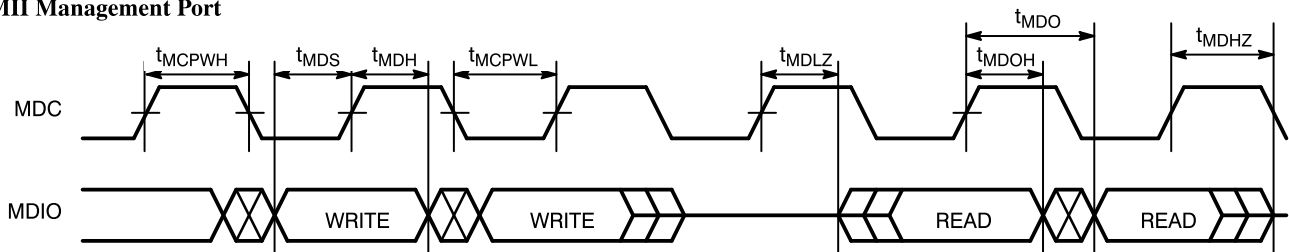


Notes:

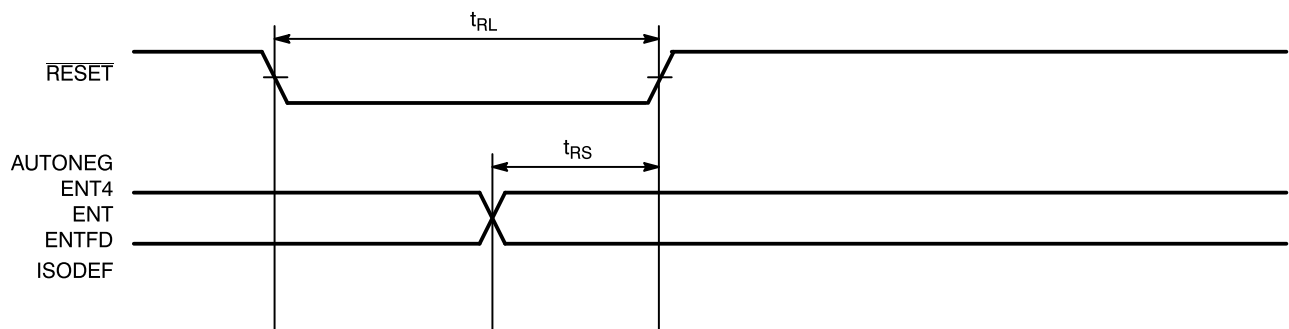
28. Switching waveforms show CRS and COL timing for a collision that is started and terminated by the transmit path (TX_EN HIGH).

Switching Waveforms (continued)
MII Carrier Sense and Collision (10BASE-T) ^[29]


7C971-17

MII Management Port


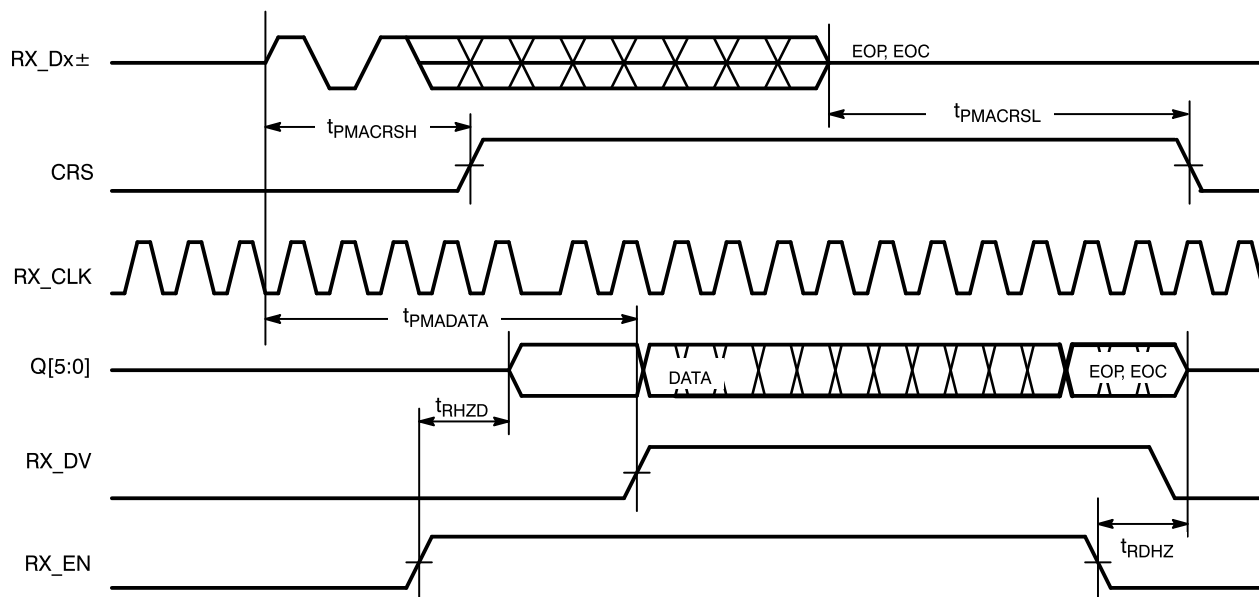
7C971-18

Control and Status Pins


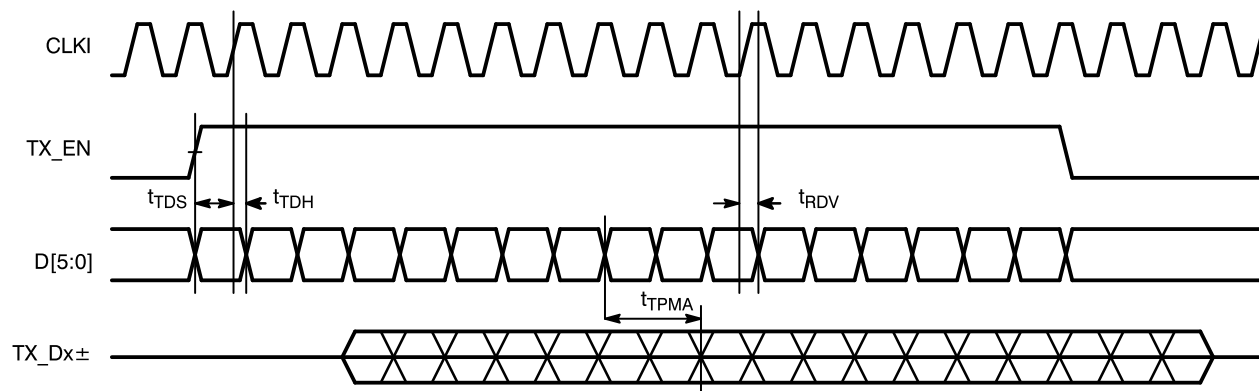
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Notes:

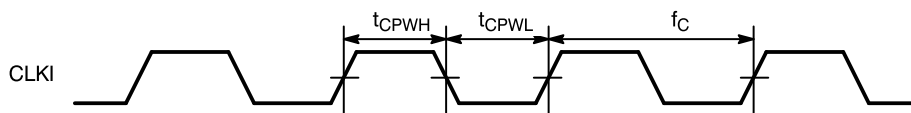
29. Switching waveforms show CRS and COL timing for a collision that is started and terminated by activity on the receive path.

Switching Waveforms (continued)
PMA Receiver Interface (MODE = LOW)


7C971-20

PMA Transmitter Interface (MODE = LOW)


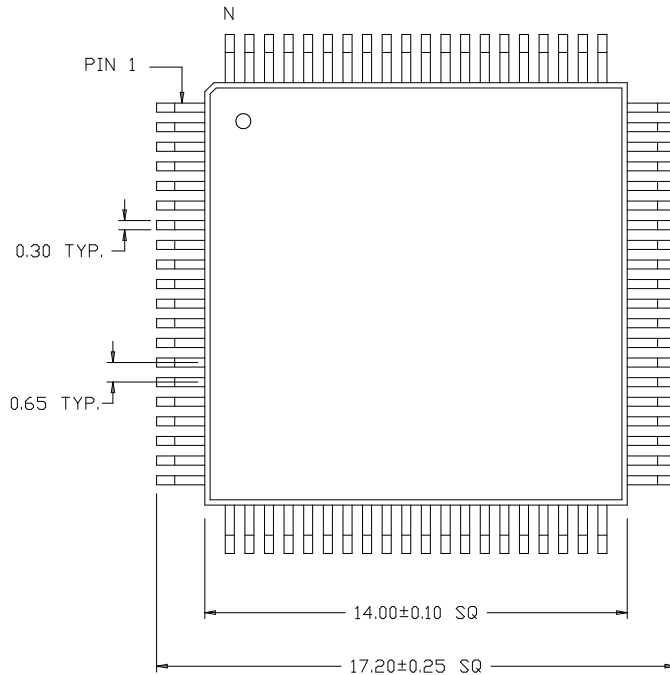
7C971-21

Reference Clock Pins


7C971-22

Package Diagram

80-Lead Plastic Quad Flatpack N80



DIMENSIONS ARE IN MILLIMETER;
LEAD COPLANARITY 0.102 MAX.

