100BASE-T4 / 10BASE-T Ethernet PCI Network Adapter

Background

This application note describes the design of a dual speed 100BASE-T4/10BASE-T Ethernet Network Adapter card for PCI systems using the Cypress CY7C971 PHY and the Digital Semiconductor 21140 MAC (Media Access Controller). The adapter card has the following features:

- Dual Speed 100BASE-T4/10BASE-T
- Full Duplex 10BASE-T
- IEEE Compliant Auto-Negotiation
- High Performance PCI Interface

The network adapter card's function is to interface the host computer to the network cabling. The adapter card plugs into the host computer's PCI bus. The twisted-pair network cable plugs into the end of the network adapter card via an 8-pin modular RJ−45 jack. *Figure 1* illustrates a PCI Network Adapter with a host motherboard.

The network interface card contains all of the circuitry for the Ethernet physical layer, MAC layer, and PCI interface. The Cypress CY7C971 contains all of the physical layer circuitry for 100BASE-T4, 10BASE-T, and Auto-Negotiation. The DEC 21140 contains all of the logic for Ethernet MAC and the PCI bus interface. The CY7C971 and the DEC

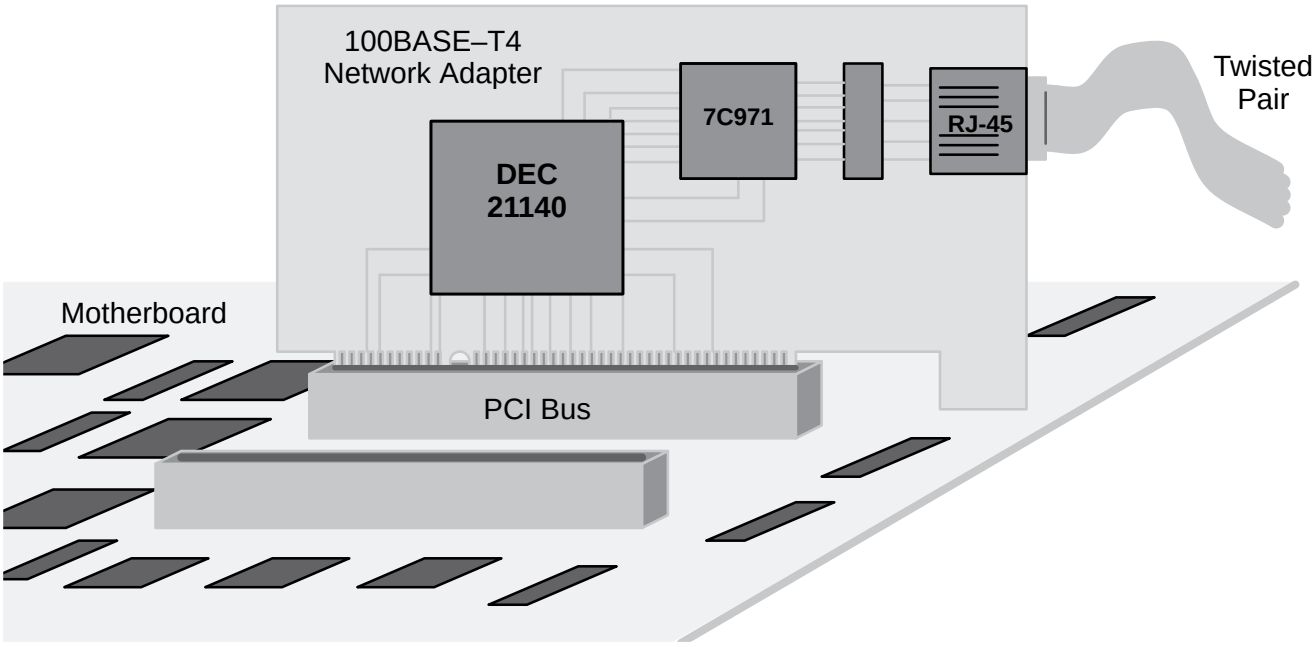


Figure 1. PCI Network Adapter Card

21140 interface to each other through the Media Independent Interface (MII). The MII is an IEEE standard interface between the Ethernet physical layer and the MAC layer.

CY7C971

Media Dependent Interface (MDI)

The CY7C971 provides a simple interface to the 8-pin modular RJ−45 jack. No expensive external filters or components are necessary because all transmit filtering and equalization are performed on-chip. All CY7C971 media interface pins are dual speed, allowing shared magnetics to be used. A quad 1:2 transformer for electrical isolation and termination resistors to match the cable impedance are all that is required.

The output buffer design uses a feedback voltage driver that minimizes power consumption and controls the common mode output voltage. The transformer provides sufficient common-mode rejection over the frequencies of interest so that an external common mode choke is not needed. *Figure 2* shows a schematic of the media interface with the CY7C971.

The characteristic impedance of the twisted pair medium is a nominal 100Ω The 1:2 transformer reduces (by the square of the turns ratio) medium load impedance to 25Ω on the primary (971) side. The termination resistors and the output buffer impedance together form a matching 25Ω load. The matching load insures that maximum signal is transferred to the medium and minimizes reflections due to impedance mismatch.

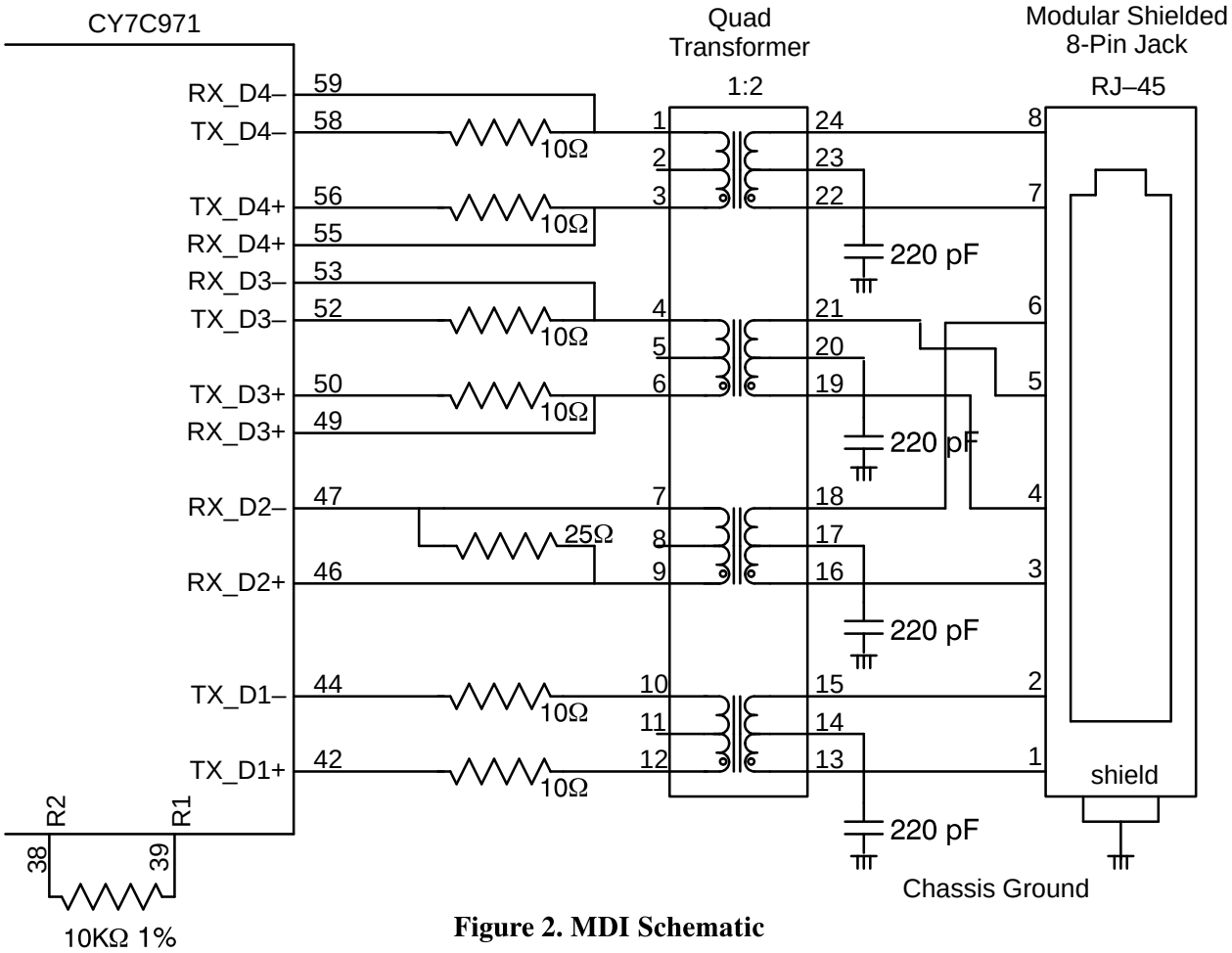


Figure 2. MDI Schematic

The center taps on the media side of the transformer are connected to the chassis ground through 220-pF (minimum) high-voltage (2 KV) capacitors. These capacitors help absorb common-mode noise that is picked up or generated on the twisted-pair medium. The capacitors must be capable of withstanding the isolation requirements specified in the 100BASE-T4 standard. High-voltage ceramic disc capacitors are economical and work well in this application.

The high precision currents needed for the transmit DAC and equalizer are derived from the external 10KΩ 1% resistor on pins R1 and R2. An internally generated band-gap voltage reference is used by the CY7C971 for all internal reference voltages.

Media Independent Interface (MII)

The Media Independent Interface (MII) is the IEEE Ethernet standard interface for communication between the MAC and PHY devices. The MII supports both 100 Mb/s and 10 Mb/s data transfer modes. In 100 Mb/s mode, the MII transfers nibble wide data groups at 25 MHz transfer rate yielding 100 Mb/s throughput. In 10 Mb/s mode, the transfer rate is reduced to 2.5 MHz for a 10 M/s throughput. During all transfers, the receive and transmit reference clock are continuously sourced from the CY7C971 PHY to the 21140 MAC. *Figure 3* shows the MII connections between the CY7C971 and the DEC 21140.

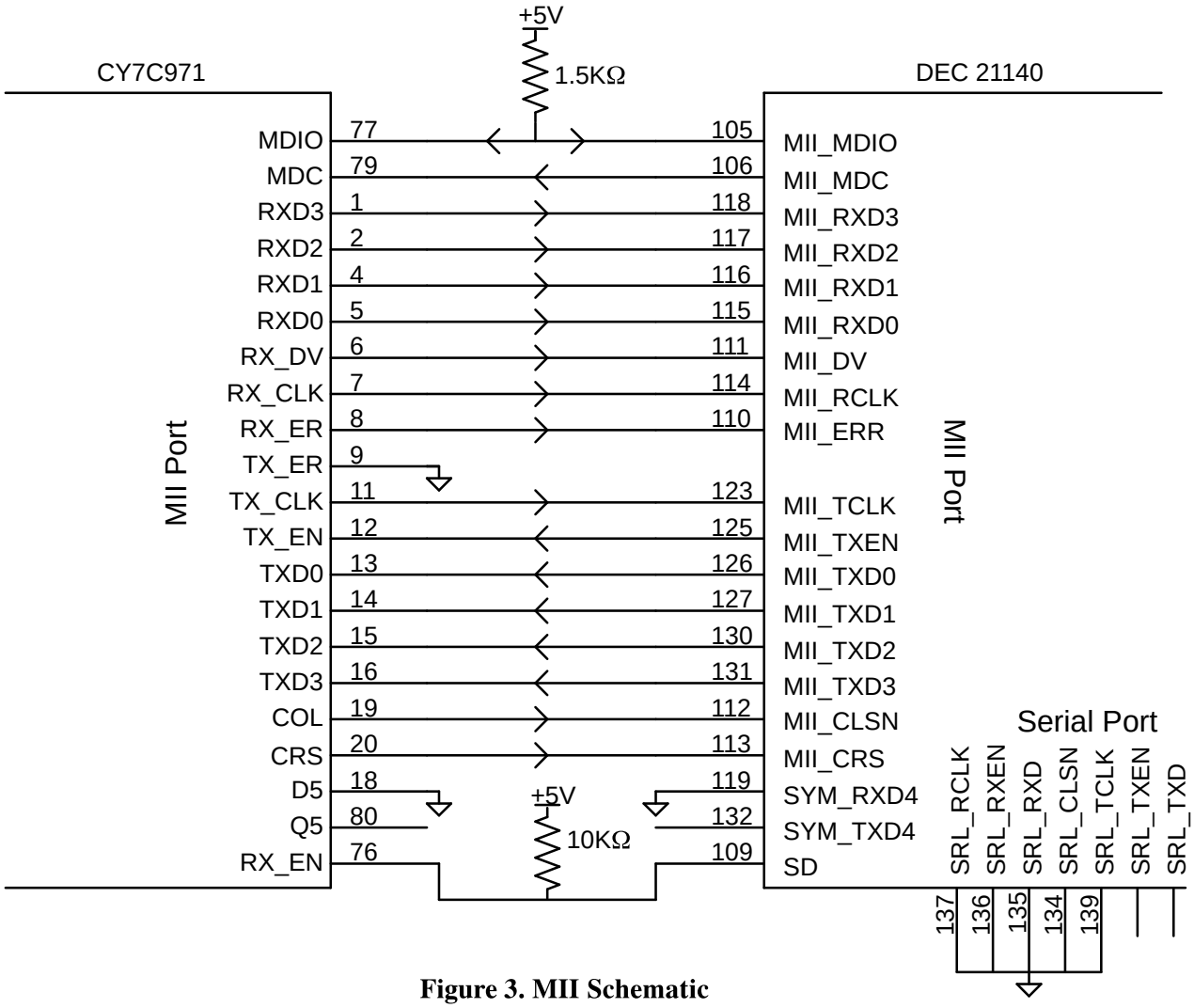


Figure 3. MII Schematic

All data transfers between the CY7C971 and the DEC 21140 are over the MII interface. The DEC 21140 has an additional 7-wire serial interface for an external 10 Mb/s transceiver. This port is not used in conjunction with the CY7C971 and these port pins are tied inactive as shown in the schematic (Appendix A).

The CY7C971 has a buffer enable input signal, RX_EN, that is not part of the MII standard. This pin is used to place the MII output buffers in high impedance. In this application, RX_EN should be tied HIGH to permanently enable the MII output buffers. The Q5 and D5 pins on the CY7C971 are not used in MII mode. D5 can be tied either HIGH or LOW. Since the DEC 21140 does not support explicit transmit error generation over the MII interface, the 971 TX_ER pin should be tied LOW to prevent inadvertent transmit error generation.

The MDC and MDIO pins form a simple two-wire serial management interface between the 7C971 and 21140. MDC is a clock signal sourced from the 21140. The MDIO line is a bidirectional data line used to transfer management data frames. The MDIO signal requires a 1.5 Kohm pull-up resistor to VCC. This interface is used to transfer standard management frames that control and monitor the behavior of the CY7C971. Management frames contain a PHY address, register number, op code, and a 16-bit data field.

Clock Pins

The CY7C971 generates all internal and external clock signals from its on-board oscillator circuit. The oscillator circuit requires an external 25 MHz parallel resonant crystal connected between the CLKO and CLKI pins. The external load capacitors (C_{load}) should be chosen so that the total load capacitance matches the parallel resonant capacitance of the crystal. The load capacitors form a series capacitance network. The required load capacitance is derived from the following equation:

$$C_{xtal} = (C_{pin} + C_{load} + C_{trace}) / 2$$

$$C_{load} = 2 \bullet C_{xtal} - C_{pin} - C_{trace}$$

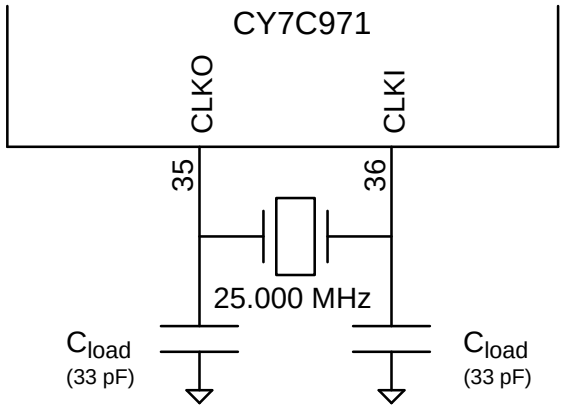


Figure 4. Clock Pins

The package pins contribute approximately 1.5 pF to the parallel load capacitance. Board trace and pads contribute between 1−2 pF of parasitic capacitance depending on trace length, width and dielectric thickness. According to this formula, an 18-pF parallel resonant crystal would require 33-pF load capacitors.

The crystal should have frequency stability of 100 ppm or less in order to comply with the Ethernet standards *Figure 4* shows the CY7C971 clock pin connections. The load capacitors are connected between the Clock pins and ground.

LED Pins

The CY7C971 can drive LEDs directly. The LED pins use an open drain output buffer that can sink up to 12 mA. The buffers have a weak internal pull-up resistor. *Figure 5* shows how the LED pins connect to the LEDs.

The $\overline{\text{LTX}}$ and $\overline{\text{LRX}}$ pins indicate when the CY7C971 is actively transmitting or receiving Ethernet frames. $\overline{\text{LTX}}$ indicates that the transmitter is active, and $\overline{\text{LRX}}$ indicates that the receiver is active. These signals are time stretched to at least 25 ms so that light pulses emitted from the LED can be detected by the human eye. These pins may be tied together in a wire-or fashion to form a generic activity indicator.

The $\overline{\text{LINKT4}}$, $\overline{\text{LINKT}}$, and $\overline{\text{LINKFD}}$ pins indicate when the CY7C971 is in the link pass state for

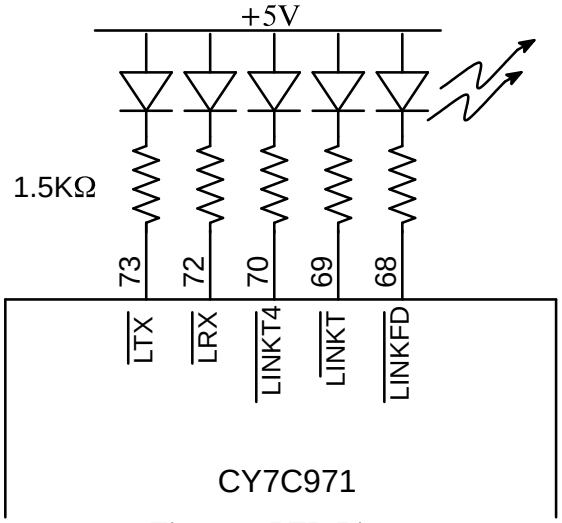


Figure 5. LED Pins

100BASE-T4, 10BASE-T, or 10BASE-T Full Duplex. The operating mode is determined either through the Auto-Negotiation process or by manual configuration with the control register (see section on MDC/MDIO Management Interface). The CY7C971 will enter a link pass state when an operating mode has been selected (either through Auto-Negotiation or manually) and properly formed technology dependent link integrity pulses are received from the medium. If only a single link indication is needed, the link indicator pins may be tied together in a wire-or fashion to form a generic link pass signal. These signals may also be individually connected to the 21140's General Purpose pins in order to quickly inform the MAC of any changes in the link status.

Configuration Pins

The configuration pins are wired for the adapter card application as shown in *Figure 6*. The ENT4, ENT, ENFD, AUTONEG are wired HIGH to enable all of the 7C971 operating modes. At power-up or during a hard reset, the logic values on these pins are loaded into their corresponding ability bits in the MII Status Register. The ability bits in the Status Register dictate whether an operating mode can be become active. After the power-up or reset cycle completes, the Auto-Negotiation process will advertise all operating modes that the Status Register reports as enabled. Management can alter the advertised abilities by changing the code word in the Auto-Negotiation Advertisement Register (Reg. 4).

The ISODEF (Isolate Default) pin is tied LOW in order to force the CY7C971 to power up with the MII ready for normal operation (not isolated). The Isolate Bit (0.10) will indicate normal operation as the default setting. The address pins (A0−A4) are wired for PHY address 01H. Address 00H is reserved for external transceivers and should not be used. The CY7C971 will respond to PHY management frames that use the assigned address. The values on the ISODEF and A0−A4 pins are latched into the 7C971 during a hard reset or power-on reset.

The MODE pin is tied HIGH to force the 7C971 into MII mode. MII mode enables the MII, PCS (Physical Coding Sublayer), and PLS (Physical Layer Signaling) logic. The PCS performs the 8B6T encoding/decoding and serial/parallel conversion for 100BASE-T4. The PLS performs Manchester encoding/decoding and serial/parallel conversion for 10BASE-T. When the MODE pin is LOW (PMA Mode), the MII, PCS, and PLS are disabled and the 100BASE-T4 PMA (Physical Medium Attachment) interface is exposed on the MII I/O pins. PMA Mode is used only in repeater applications.

The Test pin is tied LOW to permanently disable the CY7C971 test mode. Test mode is used for factory ATE testing only.

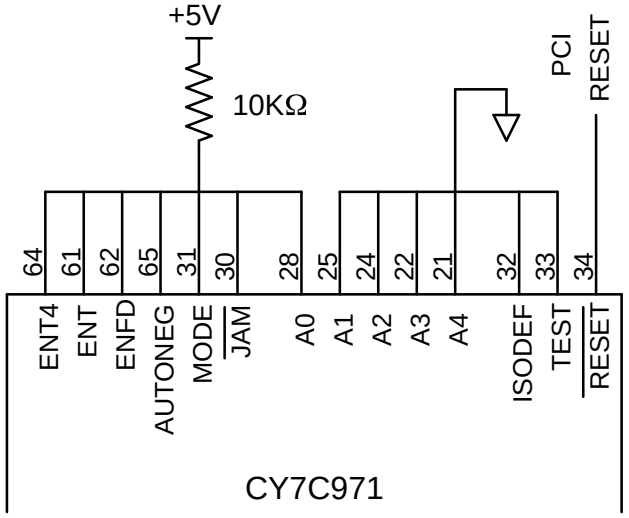


Figure 6. Configuration Pins

The $\overline{\text{RESET}}$ pin should be connected to the PCI reset pin on the card edge. Power-on reset is taken care of by an internally generated reset signal. During a hard or power-on reset, the values on the ENT4, ENT, ENFD, AUTONEG, ISODEF, and A0−A4 are loaded into the CY7C971 and all of the logic and analog circuits are forced to their default states. During a soft reset all of the logic and analog circuits are reset but the values on the configuration pins are ignored. The software drivers can issue a soft reset by setting the Reset Bit (0.15) in the Control Register. This bit is self clearing.

Layout Considerations

The adapter card design is simple enough to fit on a standard PCI short card (3.5" x 5") or smaller PCB. A 4 layer PCB construction with dedicated power and ground planes is recommended. The DEC 21140 requires a 3.3V power supply. The CY7C971 requires a 5V supply. Separate 5V and 3.3V power planes can be partitioned on a single power layer. *Figure 7* shows an example of partitioned power planes with component placement. The ground plane runs under both the 5V and 3.3V planes. There is a cutout in both the power and ground planes under the RJ−45 and transformer.

The media interface components can be neatly placed behind the RJ−45 connector. *Figure 8* illustrates the physical layout of the media interface with a 4-layer board. 0.027 µF decoupling capacitors are used on each of the CY7C971 power pins. These 0805 SMT capacitors are placed in a row as close to the pins as possible. The termination resistors fit neatly in a row behind the decoupling capacitors. Tantalum 10 µF capacitors are placed on opposite corners of the CY7C971. The CY7C971 media interface and power pins were placed in such a way to minimize the use of vias and simplify board layout.

Software Considerations

Software drivers are responsible for configuring registers within the DEC 21140 for proper operation with the CY7C971. The software drivers are also responsible for transferring Ethernet packets between the host computer's local memory and the

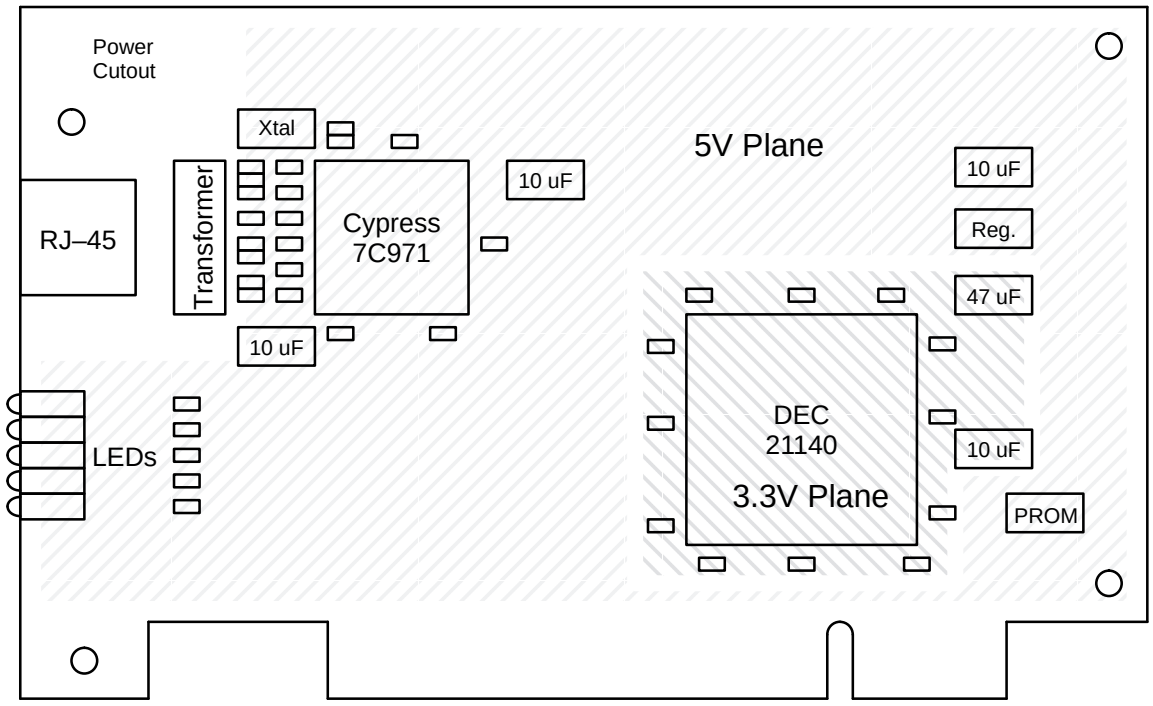


Figure 7. Power Plane and Component Placement

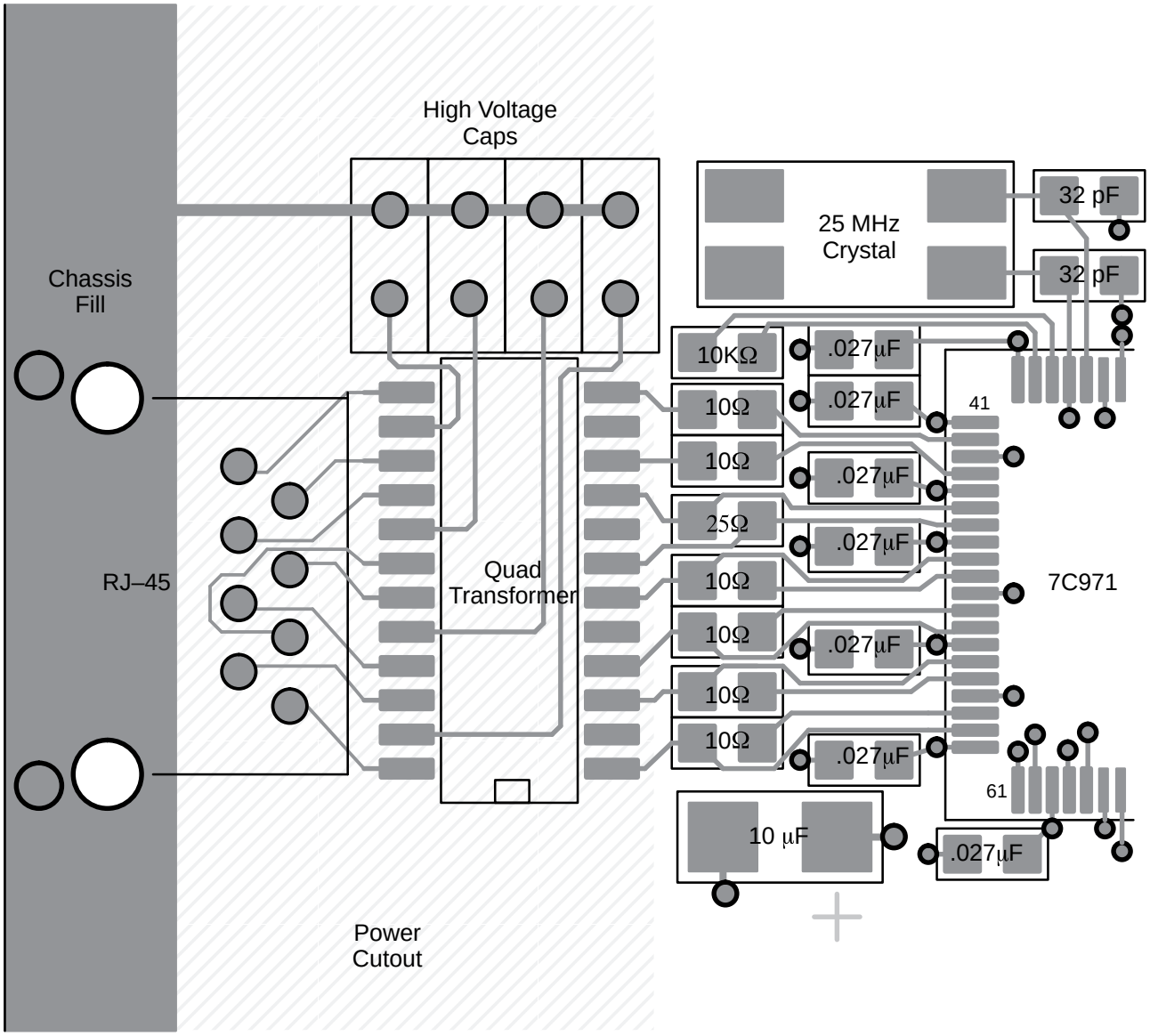


Figure 8. Media Interface Layout

21140's data buffers, and for managing the 21140 and CY7C971 resources during normal operation.

The CY7C971 contains an on-chip management facility that is accessed through its serial management port on the MII. The management facility consists of registers that report and control basic activities of the PHY such as Auto-Negotiation and link status.

The CY7C971 management facility acts as a slave device to management accesses from the MAC. Management data is transferred between CY7C971 and the DEC 21140 MAC with the MDC and MDIO pins on the MII. This connection is shown in *Figure 3*.

The DEC MAC emulates the management agent with its software drivers. During power-up, reset, or a down link, the drivers should poll the management registers to determine the result of Auto-Negotiation and the state of the link. While the link is up, the drivers should poll the CY7C971 Status Register on a timely basis to make sure the link is active. The CY7C971 was designed so that standard MII compliant software drivers can support the management facility.

DEC Register Set-Up

The 21140 Command and Status Registers (CSR) must be configured so that the 21140 communicates with the CY7C971 through the MII port. Register CSR6 in the 21140 controls the MAC-PHY interface configuration. The 21140 parallel MII port is enabled with the Port Select bit in CSR6 (CSR6, bit 18). When set, the MII port is enabled and the serial 10-Mb/s port is disabled.

The PCS Function and Scrambler Mode inside the 21140 must be disabled for proper operation with MII based transceivers such as the CY7C971. PCS and scrambler modes are used with 100BASE-X physical layer devices only. The PCS Function is disabled by clearing the PCS bit in CSR6 (CSR6, bit 23). The scrambler is disabled by clearing SCR bit in CSR6 (CRS6, bit 24).

The Transmit Threshold Mode (TTM) must be adjusted according to the operating speed of the link. This bit determines the number of bytes in a frame that must be stored in the transmit FIFO before the transmission process is initiated. In 10-Mb/s mode, the TTM bit (CSR6, bit 22) should be set. In 100-Mb/s mode, the TTM bit should be cleared. The link operating speed can be determined by polling the CY7C971 management Auto-Negotiation and Control registers or by monitoring the LED Link pins through the General Purpose Register.

MDC/MDIO Management Interface

The CY7C971 contains all of the standard and extended registers defined in the MII standard (Registers 0−7). There is also an additional CY7C971 specific register (Reg.16).The MAC can perform write and read operations to the CY7C971 management registers by transferring management frames over the MDIO serial interface. The MDC signal serves as the management data clock and is sourced from the MAC. The MDIO signal is bidirectional. The frame structure is shown in *Figure 9*.

The management frame is comprised of several fields. The start sequence 01 is used to identify the start of a frame. The op-code field determines whether a read, write, or no-op will be performed. The address field determines the target PHY. The CY7C971 will only respond to management frames whose address matches the address assigned to the CY7C971 by the address pins A0−4. In this application, the CY7C971 address has been permanently wired to 01H. All management accesses to the CY7C971 should use this address.

The register field determines the target register for the operation. The turn around field provides time to switch the direction of the bus during a read operation. The next 16 bits are the data field. During a read operation, the PHY will drive the MDIO line with the target register contents. During a write operation, 16 bits are transferred to the PHY from the MAC and written in the target register.

The CY7C971 can accept management frames that are not preceded by a 32-bit preamble. A sequence of 32 ones will force a reset on the CY7C971 management facility. It is recommended that the MAC issue this 32-bit sequence after power-up and periodically during normal operation.

The CY7C971 supports the standard and expanded MII register set. The Expanded Register set includes the OUI (Organizationally Unique Identifier) and Auto-Negotiation registers (registers 2−7). *Figure 10* shows the CY7C971 register map.

Control Register (Reg. 0)

The Control Register is used to manually set the operating modes and enable/disable certain features. Auto-Negotiation can be enabled/disabled through this register with bit 0.12. When Auto-Negotiation is enabled, the speed of the link is determined automatically, and the speed selection bit (0.13) has no effect. When Auto-Negotiation is disabled, the speed selection bit determines the speed of the link.

The loop back bit (0.14) is used to internally loop the transmit signal path to the receive signal path. Placing the CY7C971 in loopback mode will cause the

	Start	Op Code	PHY Address	Register Number	Turn Around	Data
Read	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD
Write	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD

Figure 9. Management Frame Structure

link to be broken and the transmit drivers will be forced to idle. The power-down bit (0.11) places the CY7C971 in low power stand-by mode. All of the analog circuits are placed in low power mode and the clock is stopped to all of the CMOS digital logic. Only the MDC/MDIO port is active. When power-down mode is exited, the CY7C971 will reset all of the registers to their default values. Any register setting other than the default value must be restored by the driver.

Status Register (Reg. 1)

The Status Register is a read-only register that reports the capabilities and status of the CY7C971. The status of the Auto-Negotiation process can be monitored through bit 1.5. This bit reports when Auto-Negotiation has completed. The Remote Fault bit (1.4) will indicate if Auto-Negotiation has detected a remote fault at the other end of the link. The Link Status bit indicates whenever any technology (i.e., the 10BASE-T or the 100BASE-T4 circuits of the CY7C971) has entered the Link Pass State. This means that the link is available for data transmission and reception.

OUI Registers (Reg. 2−3)

Registers 2 and 3 contain the Cypress Semiconductor Organizationally Unique Identifier and the CY7C971 part and revision number. The OUI is a 24-bit sequence that is uniquely assigned to organizations for identification purposes by the IEEE.

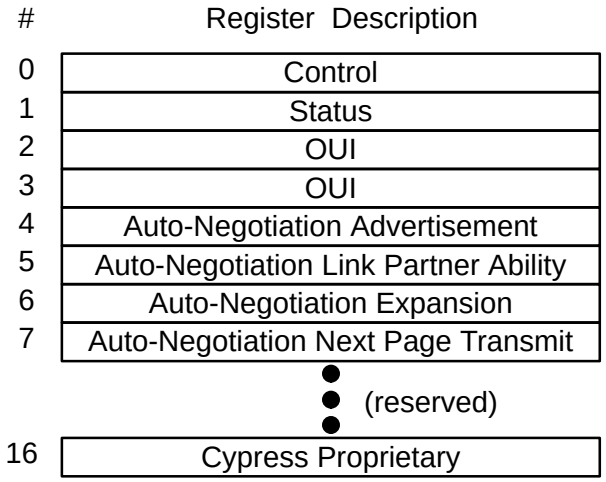


Figure 10. Register Map

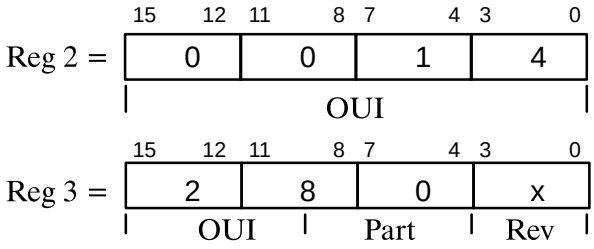


Figure 11. OUI Registers

The Cypress OUI is 00A050h. According to the Ethernet MII standard, twenty-two bits of the OUI are split between Registers 2 and 3. Register 2 contains 16 bits of the OUI and register 3 contains the other 6. Register 3 also contains 6 bits for the CY7C971 part number and 4 bits for the revision number. The register mapping and contents are shown in *Figure 11*.

Auto-Negotiation Registers (Reg. 4−7)

Registers 4 through 7 manage the Auto-Negotiation process. These registers only have meaning when Auto-Negotiation is enabled. Management intervention is not required during the normal Auto-Negotiation process. Management should only intervene with the Auto-Negotiation process in order to influence the outcome.

The Auto-Negotiation Advertisement Register (Reg. 4) holds the 16-bit code word that the CY7C971 advertises over the medium. This code word encodes the capabilities of the CY7C971, the LAN technology (CSMA/CD Ethernet), and fault indications. During power-up or reset, this register will set to the default conditions of the CY7C971 that are dictated by the enable pins. This causes Auto-Negotiation to only advertise the capabilities that are enabled. These enabled capabilities are reflected in the Status register. Management may intervene in the Auto-Negotiation process by writing to this register. Only the operating modes that are enabled in the Status Register will be advertised. Any attempt to advertise a disabled mode (disabled when ENx pin is LOW) by writing to the Advertisement Register will be ignored. Management should restart the Auto-Negotiation process by setting bit 0.9 (Restart Auto-Negotiation Bit) if the contents of the Advertisement Register are changed. *Figure 12* shows a block diagram of how the enable pins affect

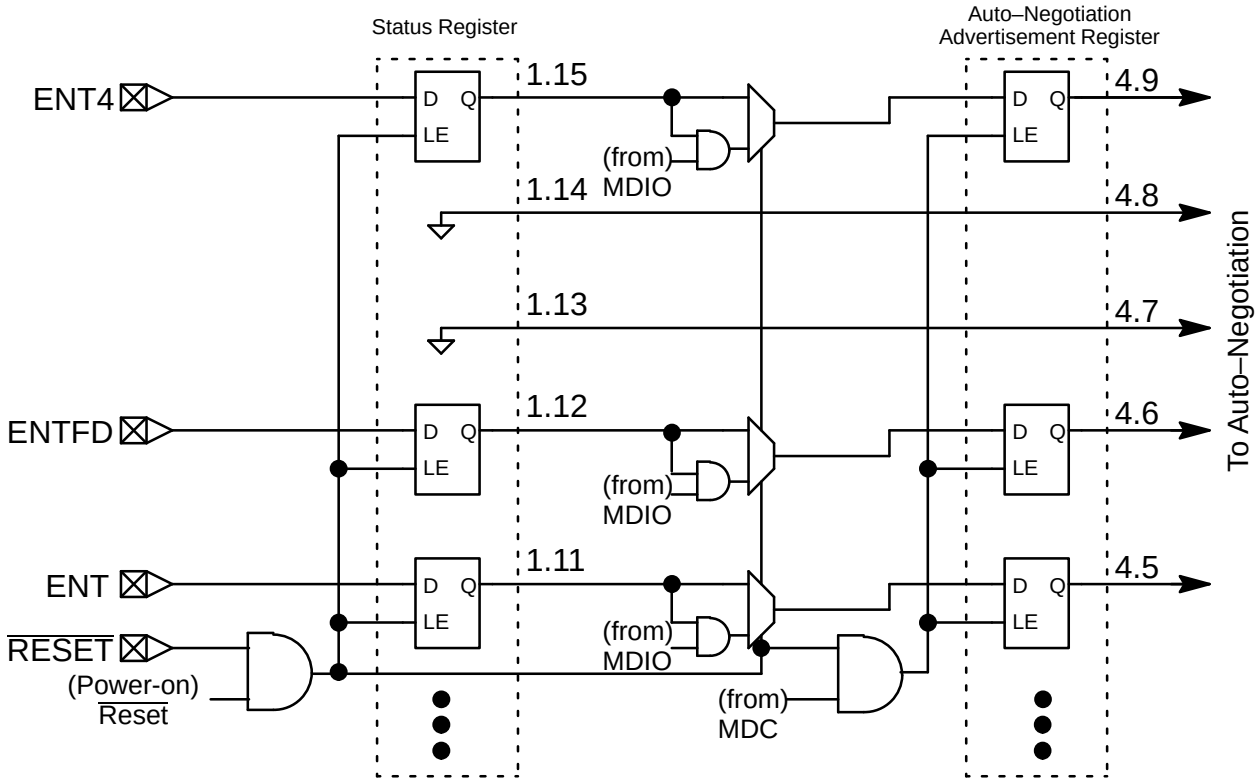


Figure 12. Register Block Diagram

Auto-Negotiation Advertisement and Status Registers.

The Auto-Negotiation Link Partner Ability Register (Reg. 5) contains the code word that has been consistently received from the PHY at other end of the medium. This register is valid when the Page Received bit (6.1) is set in Register 6. Auto-Negotiation uses the received code word to decide the operating mode of the link. The choice is based on the priority resolution table in the Auto-Negotiation standard. 100BASE-T4 has the highest priority. If Auto-Negotiation completes through parallel detection, the contents of this register are invalid. (Parallel Detection part of the Auto-Negotiation process. Its function is to detect the presence of Ethernet transceivers that do not support Auto-Negotiation.)

The Auto-Negotiation Expansion Register (Reg. 6) is a Read-Only register that reports the status of the Auto-Negotiation process. This register should be monitored during the Auto-Negotiation process in order to make sure that code words are being received and that there is not a Parallel Detection fault.

Register 7 is used to hold the Next Page code word that is to be transmitted during next page exchanges. Next Pages are code words that can be sent in addition to the base code word in the advertisement register. The Next Page facility is intended to be used as a simple scheme for passing messages between the PHYs on the medium before the link becomes active. The messages may contain information such as the presence of a fault, for example. The Next Page Transmit Register defaults to 2001H (Null Message) after power-up or a reset.

Cypress Proprietary Register (Reg. 16)

The Cypress Proprietary Register (Reg. 16) contains specific information about the CY7C971. Bit 15 indicates the polarity of the RX_D2± signal pair. When clear, this bit indicates that the polarity of RX_D2± is correct or undetermined. When set, this bit indicates that inverted polarity on RX_D2± was detected and has been corrected. Inverted po-

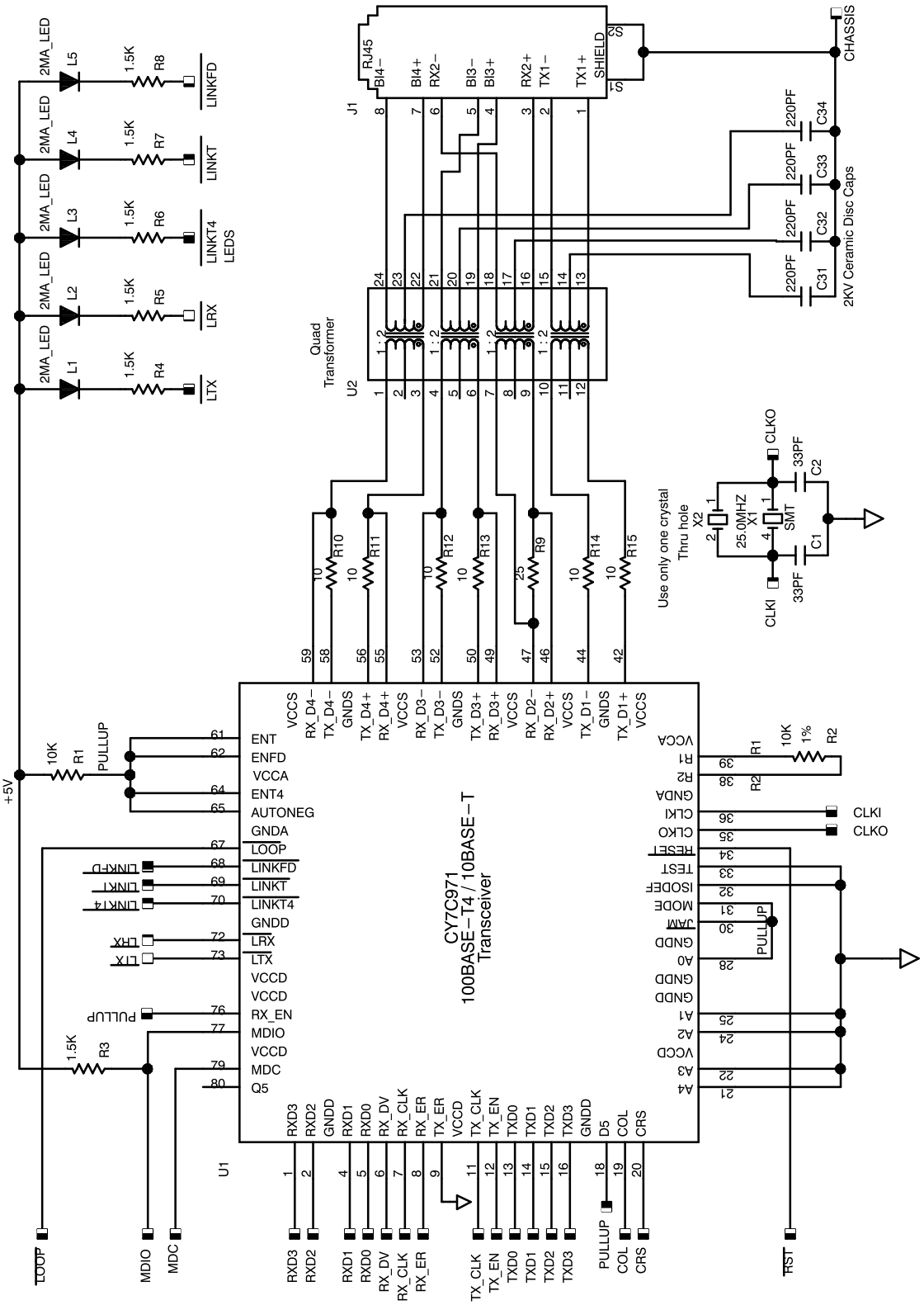
larity is most likely caused by inadvertently reversing the signal wires at the medium connector.

Conclusion

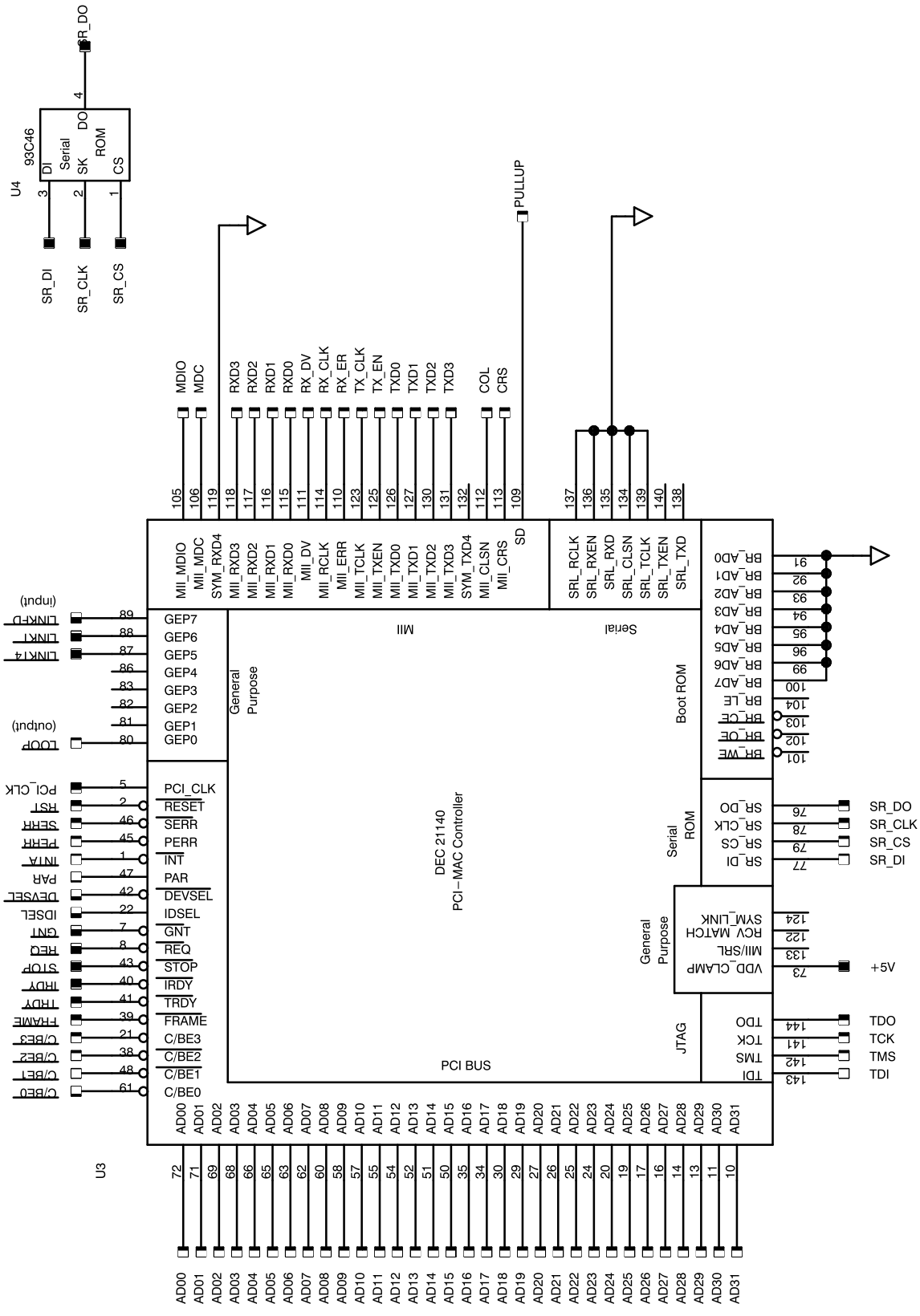
This application note covers the major issues for a dual speed Ethernet/PCI Bus adapter card design using the CY7C971 100BASE-T4/10BASE Transceiver and DEC21140 MAC. The high degree of integration in the CY7C971 keeps the number of external components to a minimum helping to reduce system cost and design effort.

The complete adapter card schematics and a bill of materials are included at the end of this application note (Appendix A and Appendix B, respectively). More information on the CY7C971 can be found in the data sheet. For more information on 100BASE-T4, MII and Auto-Negotiation standards, consult the IEEE 802.3u document: “MAC Parameters, Physical Layer, Medium Attachment Units and Repeater for 100Mb/s Operation.”

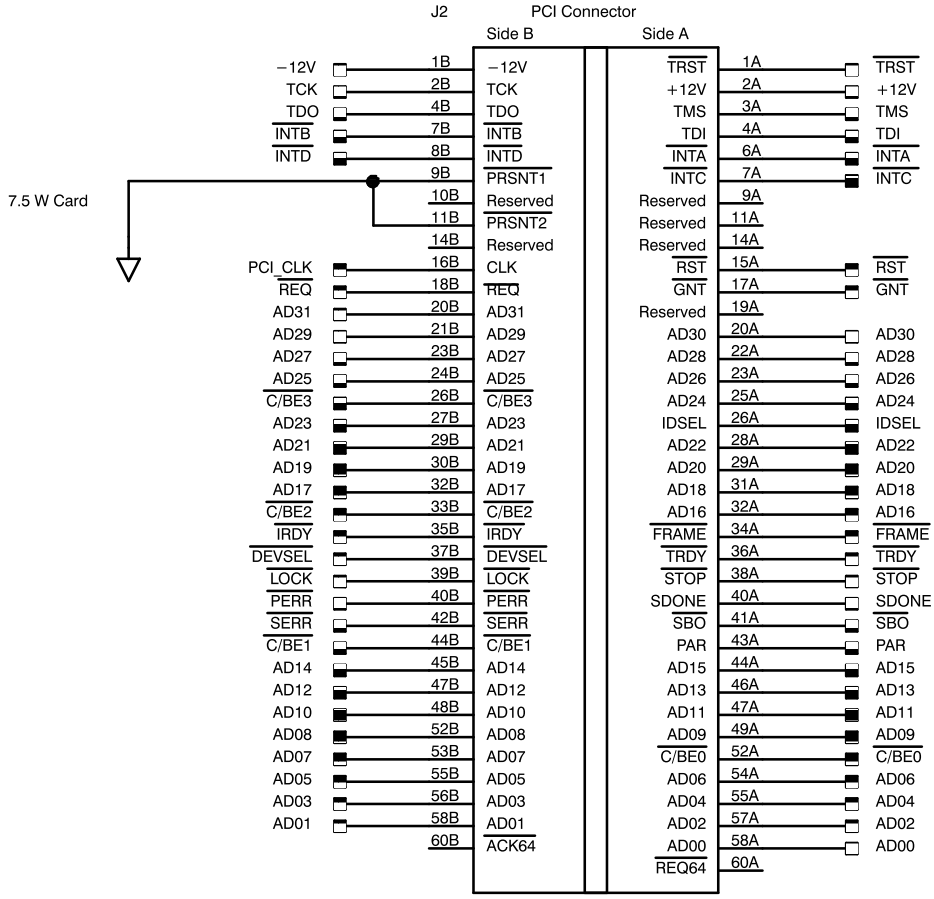
Appendix A. Schematics (Sheet 1 of 4)



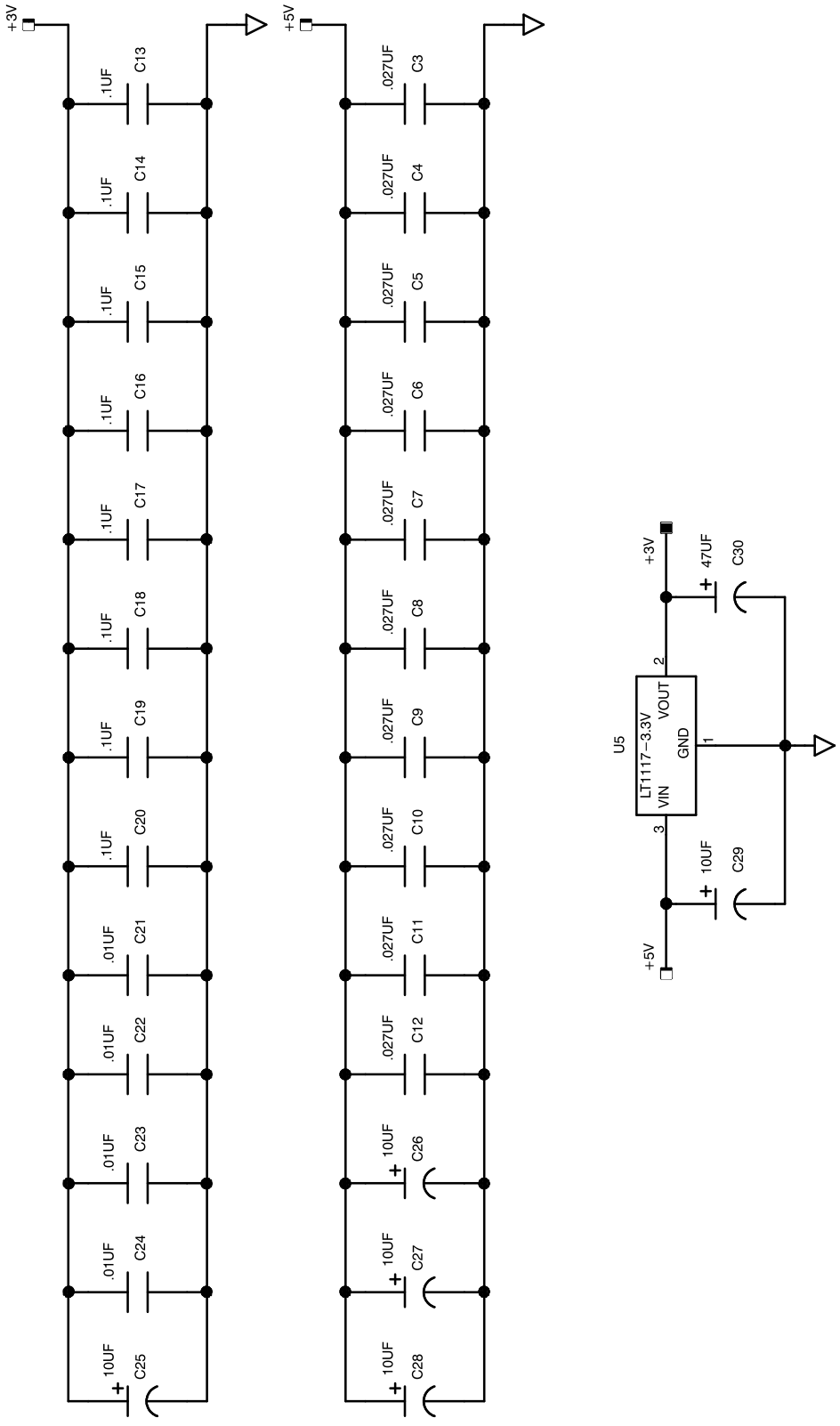
Appendix A. Schematics (Sheet 2 of 4)



Appendix A. Schematics (Sheet 3 of 4)



Appendix A. Schematics (Sheet 4 of 4)



Appendix B. Parts List

Description, Vendor, Part Number	Qty	Reference Designator
10 µF/16V Tantalum Capacitor (EIA Size C) Sprague Elec. 293D106X9016C2	6	C25, C26, C27, C28, C29, C31
47 µF/16V Tantalum Capacitor (EIA Size D) Sprague Elec. 293D476X9016D2	1	C30
.1 µF/50V Ceramic Capacitor (Size 1206) Panasonic ECU−V1H104KBW	8	C13, C14, C15, C16, C17, C18, C19, C20
.01 µF/50V Ceramic Capacitor (Size 1206) Panasonic ECU−V1H103KBM	4	C21, C22, C23, C24
.027 µF/50V Ceramic Capacitor (Size 0805) Panasonic ECU−V1H273KBX	10	C3, C4, C5, C6, C7, C8, C9, C10, C11, C12
33 pF/50V Ceramic Capacitor (Size 0805) Panasonic ECU−V1H330JCG	2	C1, C2
220 pF/2KV Ceramic Disk Capacitor Murata/Erie DE0405B2212KV	4	C31, C32, C33, C34
10.0K ohm 5% 1/8W Resistor (Size 0805) Panasonic ERJ−6GEYJ10.0K	1	R1
10.0K ohm 1% 1/10W Resistor (Size 0805) Panasonic ERJ−6ENF10.0K	1	R2
10.0 ohm 1% 1/10W Resistor (Size 0805) Panasonic ERJ−6ENF10.0	6	R10, R11, R12, R13, R14, R15
24.9 ohm 1% 1/10W Resistor (Size 0805) Panasonic ERJ−6ENF24.9	1	R9
1.50K ohm 5% 1/10W Resistor (Size 0805) Panasonic ERJ−6ENF1.50K	6	R3, R4, R5, R6, R7, R8
2 mA Green LED, PC Board Side Mount IDI 5350T5LC	3	L3, L4, L5
2 mA Yellow LED, PC Board Side Mount IDI 5350T7LC	1	L2
2 mA Red LED, PC Board Side Mount IDI 5350T1LC	1	L1
25.0000 MHz SMT Crystal, Parallel Res 18 pF Epson Amer MA−506 25.000M−AD Epson Amer MA−406 25.000M−G	1	X1
25.0000 MHz HC−49/U Crystal, Parallel Res 18 pF Ecliptek EC250−25.0000	1	X2
Quad 2:1 Transformer, 330 µH Primary, 1500V Valor ST6115 Pulse PE−69001 Bel S553−1204−00	1	U2
CY7C971 100BASE-T4/10BASE-T Transceiver Cypress Sem. CY7C971−NC	1	U1

Appendix B. Parts List (continued)

Description, Vendor, Part Number	Qty	Reference Designator
LT1117 3.3V Regulator Linear Tech. LT1117CST−3.3	1	U5
RJ−45 Modular 8-Pin Shielded Jack Amp 555141−1	1	J1
DEC21140 Fast Ethernet PCI MAC Digital Sem. 21140−AA	1	U3
93C46 1K Serial EEPROM (8-Pin SOIC) National Sem. NM93C46M8	1	U4

Assembly Instructions

1. Assemble only 1 crystal (X1 or X2).