CY7C42X/46X FIFO Interface to the CY7B923 (HOTLink™)

Transmitter Interface Description

This application note considers the interface between a Cypress CY7B923 (HOTLink™) Transmitter and generic FIFOs. Minimal interface logic is required to achieve a high-performance interface. A block diagram of the HOTLink Transmitter and generic FIFO interface is shown in *Figure 1*.

The FIFO operates as an asynchronous data rate buffer between the HOTLink Transmitter and the data source. The data is continually read from the FIFO into the transmitter when the Transmit signal is asserted. Reading continues until the FIFO is empty.

Critical Timing Analysis

The following equations describe the critical timing relationships. They have been solved for the minimum bit time t_B. The clock period time is $10t_B$. A timing diagram is provided in *Figure 2*. The critical timing equations are shown at the bottom of the diagram.

Read Pulse Width

$$t_{PR(min)} \leq 6t_B - 3\text{ ns} - 2\text{ns} \qquad \text{Eq. 1}$$
$$t_B \geq (t_{PR(min)} + 5\text{ ns}) / 6$$

The read pulse width for the FIFO is t_{PR}.

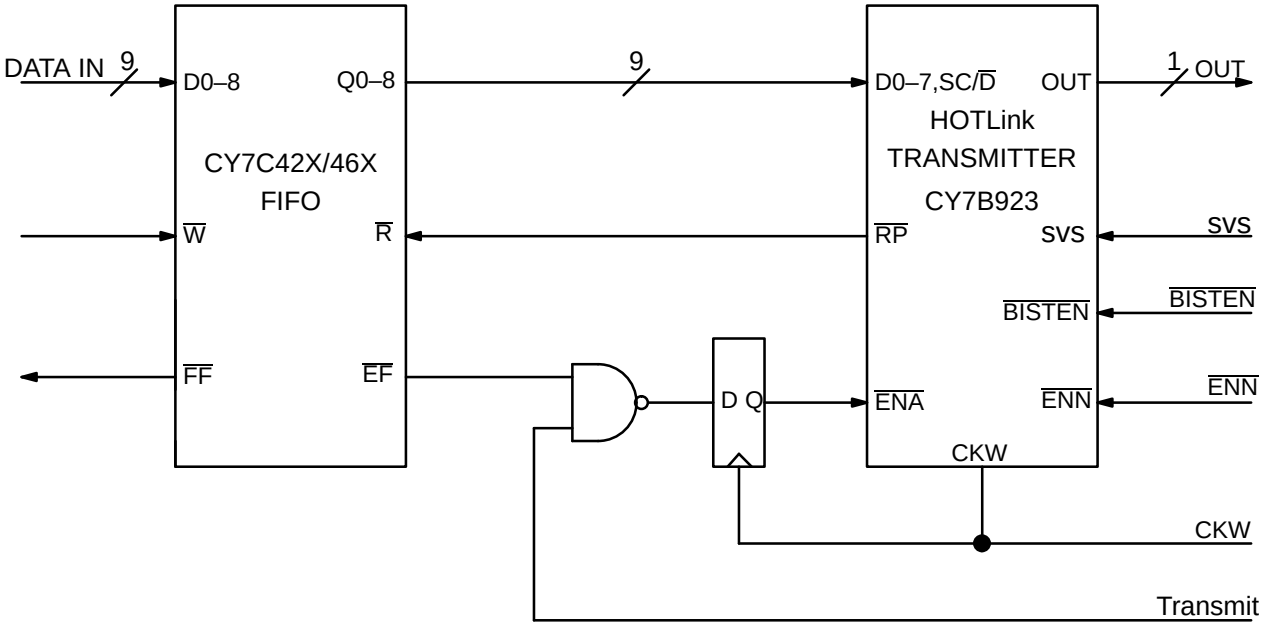
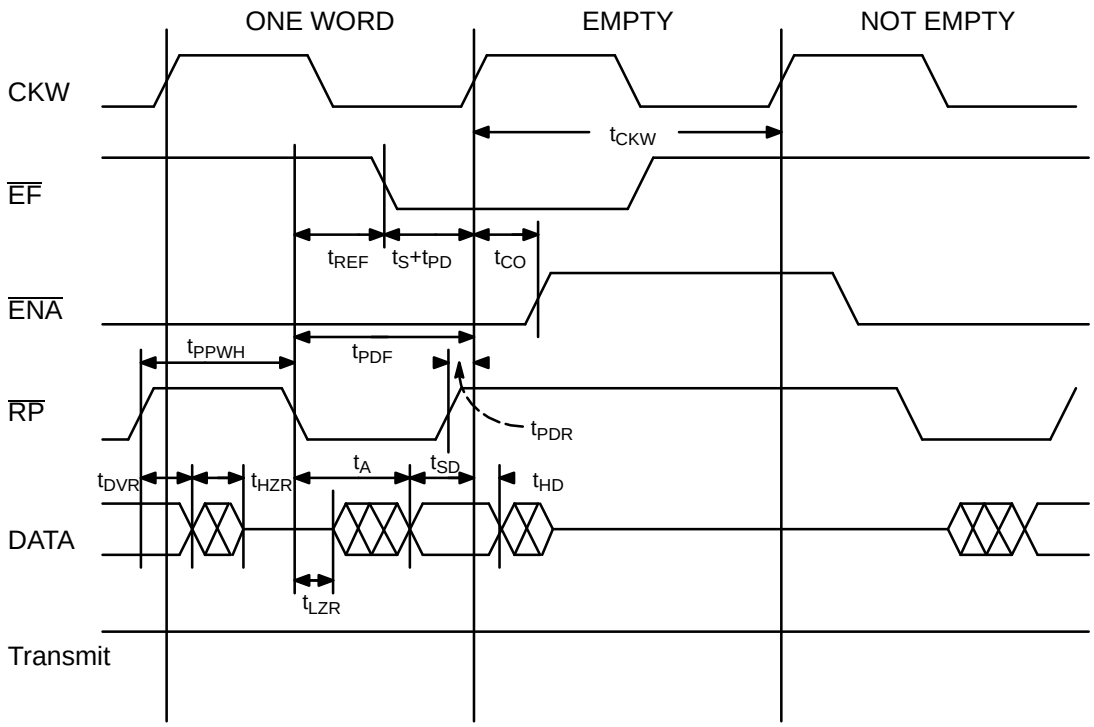


Figure 1. Transmitter Interface Diagram



Critical Timing Analysis

1. Read pulse width:
$$t_{PR(min.)} \leq t_{PDF(min.)} - t_{PDR(max.)}$$
2. Read recovery time:
$$t_{RR(min.)} \leq t_{PPWH(max.)}$$
3. Data set-up time:
$$t_{A(max.)} + t_{SD(min.)} \leq t_{PDF(min.)}$$
4. Empty flag to register set-up time:
$$t_{REF(max.)} + t_{PD(max.)} + t_{S(min.)} \leq t_{PDF(min.)}$$
5. Transmit enable to HOTLink set-up time:
$$t_{CO(max.)} \leq 10\ t_B - t_{SENP(min.)}$$
6. Data hold time:
$$t_{PDR(max.)} + t_{HD(max.)} \leq t_{DVR(min.)}$$

Figure 2. Interface Timing Diagram

Read Recovery Time

$$t_{RR(min.)} \leq 4t_B - 3\ ns \qquad \text{Eq. 2}$$
$$t_B \geq (t_{RR(min.)} + 3\ ns) / 4$$

The read recovery time for the FIFO is t_{RR}.

Data Set-Up Time

$$t_{A(max.)} + 5\ ns \leq 6t_B - 3\ ns \qquad \text{Eq. 3}$$
$$t_B \geq (t_{A(max.)} + 8\ ns) / 6$$

The data access time for the FIFO is t_A and it is the basis of FIFO speed ratings.

Empty Flag to Register Set-Up Time

$$t_{REF(max.)} + t_{PD(max.)} + t_{S(min.)} \leq 6t_B - 3\ n \qquad \text{Eq. 4}$$
$$t_B \geq (t_{REF(max.)} + t_{PD(max.)} + t_{S(min.)} + 3\ ns) / 6$$

The Empty flag delay from the FIFO is t_{REF}. The register set-up time for the external register is t_S.

Transmit Enable to HOTLink Set-Up Time

$$t_{CO(max.)} + \leq 4t_B - 8\ ns \qquad \text{Eq. 5}$$
$$t_B \geq (t_{CO(max.)} + 8\ ns) / 4$$

The register clock to output delay is t_{CO}. The propagation delay of the external control logic is t_{PD}.

Data Hold Time

$$t_{DVR(min.)} \geq 2\ ns \qquad \text{Eq. 6}$$

The valid data hold time from a FIFO read is t_{DVR}. HOTLink has a zero data hold time.

Table 1. Critical FIFO Timing Parameters

Parameter	FIFO Speed Rating		
	−10	−15	−20
$t_{PR(min)}$	10 ns	15 ns	20 ns
$t_{RR(min)}$	10 ns	10 ns	10 ns
$t_{A(max)}$	10 ns	15 ns	20 ns
$t_{REF(max)}$	10 ns	15 ns	20 ns
$t_{DVR(min)}$	3 ns	3 ns	3 ns

Table 1 shows the critical timing parameters for various speed grades of generic FIFOs. The FIFO timing parameters are taken from a hypothetical CY7C42X−10, a CY7C46X−15, and a CY7C46X−20.

Table 2 shows the maximum frequency of CKW associated with each of the timing equations for the different speed grades of generic FIFOs. The maximum interface operating frequency is shown in italics. A PAL20−5 (t_{PD} = 5 ns, t_{CO} = 5 ns, t_S = 2.5 ns) is used for the flag register and enable control logic.

Equation 6 is independent of the clock frequency and is satisfied by all of the considered FIFOs.

Equation 4 is the critical timing relationship for all of the FIFO speed grades. Timing margins can be increased by using faster control logic (PAL20−4).

Table 2. Maximum Transmitter Interface Frequency with Asynchronous FIFOs

Eqn. #	−10	−15	−20	Units
1	40.0	30.0	24.0	MHz
2	30.7	30.7	30.7	MHz
3	33.3	26.1	21.4	MHz
4	29.2	23.5	19.7	MHz
5	30.8	30.8	30.8	MHz
bit rate	292	235	197	Mbits/s

Summary

With available CY7C46X−15 FIFOs, the HOTLink-FIFO interface can operate at a frequency of 23.5 MHz with minimal interface logic. This corresponds to a serial bit rate of 235 Mbits/s.

When −10 FIFOs become available, the maximum interface frequency will increase to 29.2 MHz (292 Mbits/s).