HOTLink™ CY7B933 $\overline{\text{RDY}}$ Pin Description

This application note describes the behavior of the $\overline{\text{RDY}}$ (Ready) pin in several modes of operation: Encoded, Bypass, and BIST (Built-In Self-Test). The $\overline{\text{RDY}}$ pin indicates the status of the HOTLink™ Receiver control logic and output pins. Its function and timing are dependent on the state of the MODE, $\overline{\text{BISTEN}}$ (Built-In Self-Test Enable), and RF (Reframe) pins. The following sections describe $\overline{\text{RDY}}$ behavior in detail.

Normal $\overline{\text{RDY}}$ Timing

The HOTLink CY7B933 datasheet specifies signal transitions for the receiver in bit-times relative to the rising edge of CKR. A bit-time refers to the period of the internal receiver bit-rate clock. The period of the recovered byte-rate clock, CKR, is ten times the bit period (bit period $t_B = t_{CKR} \div 10$). In the following discussions on timing, the rising edge of CKR is referenced as bit-time zero. The next rising edge of CKR occurs ten bit-times later (unless CKR stretches due to reframing). Transitions on other signal pins are defined in bit-times relative to bit-time zero. These timing conventions are adhered to throughout this application note.

The normal timing of the $\overline{\text{RDY}}$ pin refers to its behavior in Encoded or Bypass mode with $\overline{\text{BISTEN}}$ HIGH (Built-In Self-Test disabled). In either of these modes, $\overline{\text{RDY}}$ rests HIGH in its inactive state. During its active state, $\overline{\text{RDY}}$ transitions LOW on bit-time five and then transitions HIGH on bit-time one of the next clock cycle. *Figure 1* illustrates $\overline{\text{RDY}}$ timing in relation to CKR and DATA. For the exact timing margins[1] of these signals, refer to the HOTLink datasheet. In BIST mode, $\overline{\text{RDY}}$ assumes much different behavior and timing. These differences are explained later in the sections on BIST.

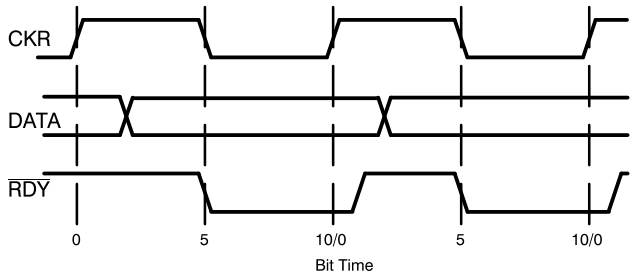

Figure 1. Normal $\overline{\text{RDY}}$ Timing

$\overline{\text{RDY}}$ in Encoded Mode

This section describes the operation of $\overline{\text{RDY}}$ in Encoded mode (MODE = LOW). In Encoded mode, the raw ten-bit serial data is decoded in the 8B/10B decoder and then presented at the parallel output pins.

Normal Operation

The normal operation of the $\overline{\text{RDY}}$ pin in Encoded mode (MODE = LOW, RF = LOW, $\overline{\text{BISTEN}}$ = HIGH) is to signal when new data is available at the parallel output pins (Q_{0-7}, SC/$\overline{\text{D}}$, RVS). $\overline{\text{RDY}}$ pulses LOW with a 60% LOW/40% HIGH duty cycle only when new data is present at the output. The timing of $\overline{\text{RDY}}$ is optimized for a seamless interface to industry standard FIFOs (First-In First-Out memories). $\overline{\text{RDY}}$ does not pulse LOW in a field of SYNC (K28.5) characters; however, $\overline{\text{RDY}}$ does pulse LOW for the last K28.5 in the field or for any single K28.5. This behavior helps prevent a FIFO from filling with meaningless strings of SYNC characters. *Figure 2* illustrates normal $\overline{\text{RDY}}$ behavior in Encoded mode.

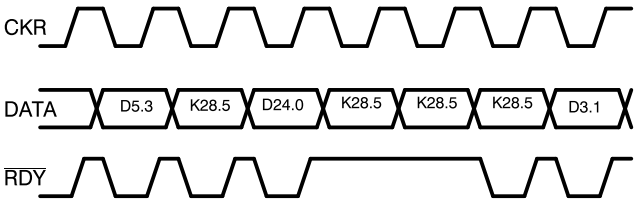

Figure 2. Normal $\overline{\text{RDY}}$ Operation in Encoded Mode

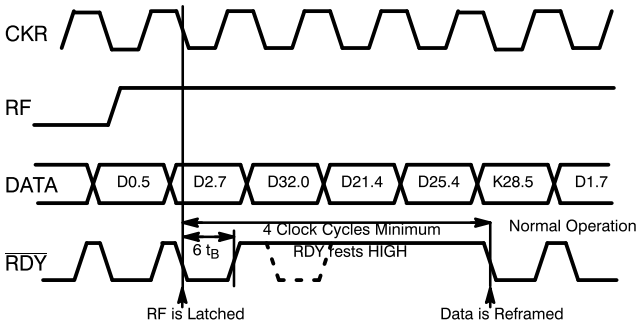

Figure 3. $\overline{\text{RDY}}$ During Framing in Encoded Mode

Entering Framing

When the RF pin is asserted HIGH, the receiver byte framer is enabled and the $\overline{\text{RDY}}$ pin leaves normal Encoded mode operation. The receiver latches the RF signal on the falling edge of CKR. When RF is latched HIGH, $\overline{\text{RDY}}$ is forced HIGH one bit time after the next rising edge of CKR (approximately $6t_B$ later). The exception to this is when there is a K28.5 in the framer when RF is asserted HIGH. In this case, an additional $\overline{\text{RDY}}$ pulse will occur after RF is latched HIGH. $\overline{\text{RDY}}$ will then pulse LOW when the data byte boundary is framed to an incoming SYNC character (K28.5). The latency of the receiver data pipeline and control logic insure that $\overline{\text{RDY}}$ will not pulse LOW any earlier than the fourth clock cycle after RF is latched HIGH. External framing logic should be designed to examine the $\overline{\text{RDY}}$ pin only after the 4 clock cycle delay.

After the data has been framed, $\overline{\text{RDY}}$ will assume its normal Encoded mode behavior (pulsing LOW for every character except strings of K28.5s). If RF remains HIGH, the framer still continues to frame the data to any K28.5 pattern found in the data stream. If RF is asserted HIGH for more than 2048 REFCLK cycles, the framer converts to a double-byte framer requiring two K28.5s within five bytes for framing. The function and timing of $\overline{\text{RDY}}$, however, remain unchanged. The timing of $\overline{\text{RDY}}$ while entering framing is outlined in *Figure 3*.

Leaving Framing

When RF is deasserted, the framer is disabled and the $\overline{\text{RDY}}$ pin assumes its normal Encoded mode operation. If the data was framed during the assertion of RF, $\overline{\text{RDY}}$ will have already assumed its normal operation. If the framer is disabled without having framed the data, one clock cycle will pass before $\overline{\text{RDY}}$ assumes normal operation. *Figure 4* shows the framer being disabled before the data is framed. $\overline{\text{RDY}}$ resumes normal operation one cycle after RF is latched LOW.

$\overline{\text{RDY}}$ in Bypass Mode

This sections describes the operation of $\overline{\text{RDY}}$ in Bypass mode (MODE = HIGH). In Bypass mode, the raw ten bit serial data bypasses the 8B/10B decoder and is presented at the parallel output pins.

Normal Operation

The normal operation of the $\overline{\text{RDY}}$ pin in Bypass mode (MODE=HIGH, RF=LOW, $\overline{\text{BISTEN}}$=HIGH) is to signal when a data pattern matching K28.5 character is present on the receiver's parallel output pins (Q_{a-j}). $\overline{\text{RDY}}$ will remain HIGH during all other data patterns. *Figure 5* shows an example of $\overline{\text{RDY}}$ in Bypass mode.

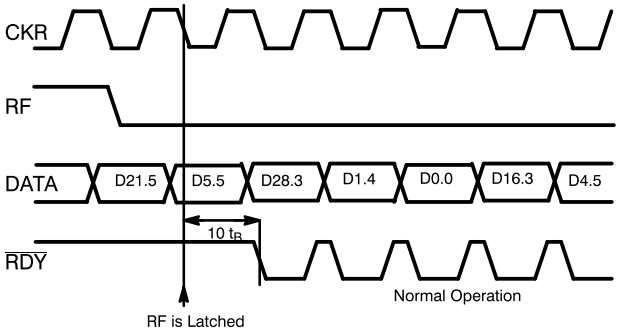

Figure 4. $\overline{\text{RDY}}$ While Leaving Framing

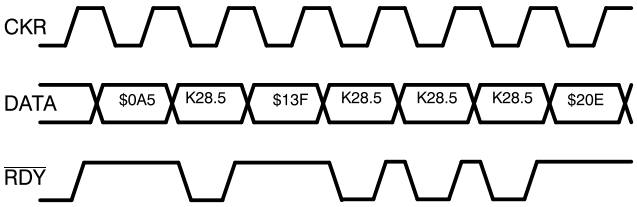

Figure 5. Normal $\overline{\text{RDY}}$ Operation in Bypass Mode

Entering Framing

The behavior of $\overline{\text{RDY}}$ while entering framing from Bypass mode is very similar to entering from Encoded mode. When RF is latched HIGH, $\overline{\text{RDY}}$ leaves normal Bypass mode operation and is forced HIGH one bit time after the next rising edge of CKR. When the framer is enabled, a LOW pulse on $\overline{\text{RDY}}$ indicates that the serial data has been framed to an incoming SYNC character (K28.5). The latency of the data pipeline and control logic insure that $\overline{\text{RDY}}$ does not pulse LOW any earlier than the fourth clock cycle after RF is latched HIGH. External framing logic should be designed to examine the $\overline{\text{RDY}}$ pin only after the 4 clock cycle delay. After the data has been framed, $\overline{\text{RDY}}$ assumes its normal Bypass mode behavior (pulsing LOW only on K28.5 characters). While RF is HIGH, the framer continues to frame the data to any K28.5 pattern in the data stream. The timing of $\overline{\text{RDY}}$ while entering framing from Bypass mode is outlined in *Figure 6*.

Leaving Framing

When RF is deasserted (LOW), the framer is disabled and the $\overline{\text{RDY}}$ pin assumes normal Bypass mode behavior. If the data was framed during the assertion of RF, $\overline{\text{RDY}}$ will have already assumed its normal operation. If Reframe is exited without having framed the data, one clock cycle passes before $\overline{\text{RDY}}$ assumes normal operation. *Figure 7* shows RF deasserted before the serial data has been framed.

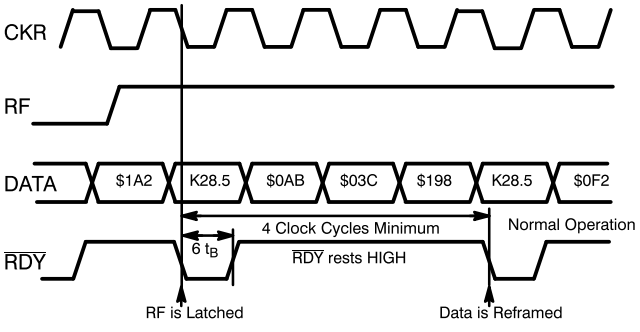

Figure 6. $\overline{\text{RDY}}$ During Framing in Bypass Mode

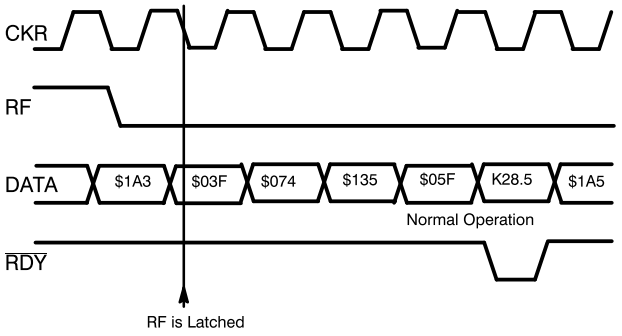

Figure 7. $\overline{\text{RDY}}$ While Leaving Framing

$\overline{\text{RDY}}$ and CKR Stretching

During framing (RF = HIGH), $\overline{\text{RDY}}$ and CKR may stretch as the byte boundary is synchronized to an incoming K28.5 character. If a K28.5 pattern is found in the serial data stream that is not aligned with the current byte boundary, the framer will realign the phase of CKR so that the receiver shift register properly deserializes the K28.5 character (and the following data). The HIGH or LOW phase of CKR and $\overline{\text{RDY}}$ will be stretched so that these signals maintain proper byte synchronization with the data. *Figure 8* shows $\overline{\text{RDY}}$ and CKR being stretched during framing due to a K28.5 character in the data stream. In this example, RF is held HIGH so that the framer remains enabled after has $\overline{\text{RDY}}$ assumed its normal operation according to the MODE pin (Encoded mode). The period of $\overline{\text{RDY}}$ and CKR

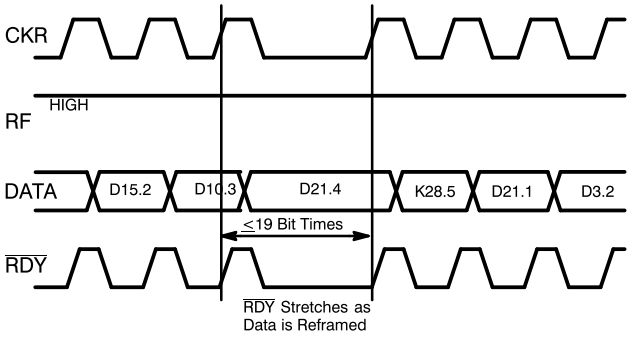

Figure 8. $\overline{\text{RDY}}$ and CKR Stretching (Encoded Mode)

may stretch up to a length of 19 bit-times depending on the position of the K28.5 character relative to the old byte boundary. Note that the K28.5 character comes out of the receiver one cycle after the CKR and $\overline{\text{RDY}}$ stretch due to the receiver pipeline.

$\overline{\text{RDY}}$ in BIST Mode

The Built-In Self-Test (BIST) feature provides a simple but exhaustive method for testing the integrity of the physical link. BIST Mode is entered by asserting the $\overline{\text{BISTEN}}$ pin LOW in either Encoded or Bypass mode. $\overline{\text{RDY}}$ has two normal modes of operation while in BIST. $\overline{\text{RDY}}$ initially rests HIGH when BIST is entered, signaling that the BIST logic has not started checking the received data. When a valid start of BIST sequence is received, the $\overline{\text{RDY}}$ pin will rest LOW, indicating that BIST checking is in progress. The timing of these transitions is discussed below. For more information on BIST, consult the "HOTLink Built-In Self-Test" application note.

Entering BIST Mode

BIST mode is entered by asserting $\overline{\text{BISTEN}}$ LOW. $\overline{\text{BISTEN}}$ is latched into the receiver on the falling edge of CKR. When $\overline{\text{BISTEN}}$ is latched LOW, $\overline{\text{RDY}}$ leaves its current mode of operation (Encoded or Bypass) and is asserted LOW for one full CKR cycle. On bit-time one of the next clock cycle, $\overline{\text{RDY}}$ is forced HIGH. The BIST logic will check the incoming data stream for the start of BIST sequence (D1.0 followed by D0.0). $\overline{\text{RDY}}$ rests HIGH while the BIST logic waits for this sequence. *Figure 9* shows the behavior of $\overline{\text{RDY}}$ when $\overline{\text{BISTEN}}$ is asserted LOW.

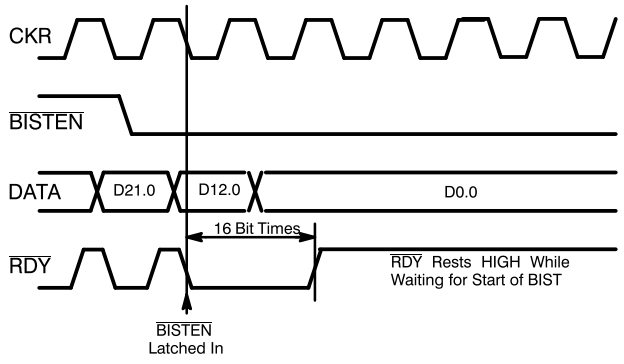

Figure 9. $\overline{\text{RDY}}$ while Entering BIST

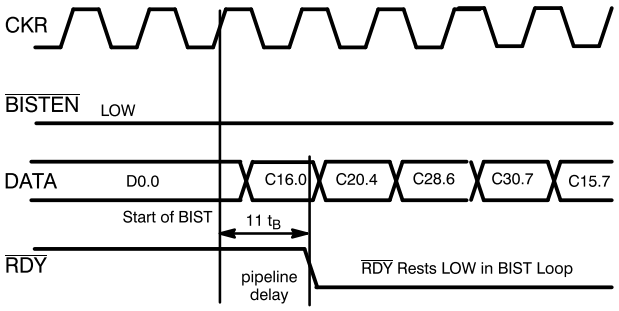

Figure 10. $\overline{\text{RDY}}$ at Start of BIST

Start of BIST

When the start of BIST pattern is found, $\overline{\text{RDY}}$ will transition LOW one bit time after CKR rises. Due to the pipeline nature of the receiver, there is a one cycle delay from when start of BIST is detected and when $\overline{\text{RDY}}$ is asserted LOW. $\overline{\text{RDY}}$ will remain LOW for the duration of BIST except to pulse HIGH for one clock cycle each time a BIST Loop starts (once every 511 bytes). *Figure 10* shows the $\overline{\text{RDY}}$ pin during the start of BIST sequence.

BIST Loop

Figure 11 shows $\overline{\text{RDY}}$ behavior once BIST checking has begun. $\overline{\text{RDY}}$ rests LOW and pulses HIGH at the start of each new BIST loop. During this pulse, $\overline{\text{RDY}}$ rises on bit time one and then falls one cycle later on bit time one. This pulse is useful for counting the number of BIST loops completed.

Leaving BIST

BIST is disabled by setting $\overline{\text{BISTEN}}$ HIGH. $\overline{\text{RDY}}$ will assume the behavior dictated by the MODE pin

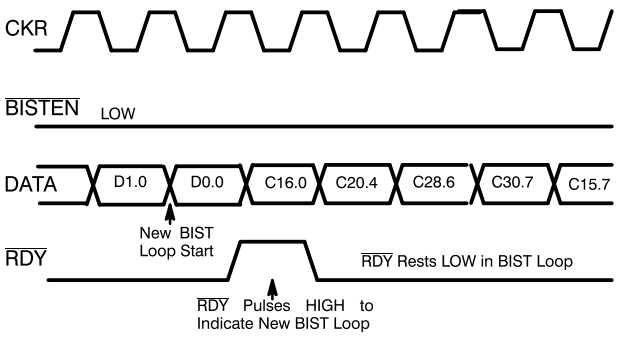

Figure 11. $\overline{\text{RDY}}$ in BIST Loop

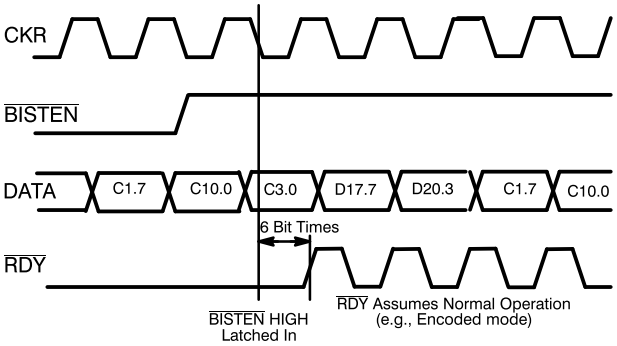

Figure 12. $\overline{\text{RDY}}$ While Leaving BIST

(Encoded or Bypass) one clock cycle after $\overline{\text{BISTEN}}$ is latched HIGH. *Figure 12* shows the $\overline{\text{RDY}}$ pin while leaving BIST Mode.

Framing While in BIST

Framing may be performed while in BIST Mode. The BIST pattern includes one alias K28.5 and several instances of byte aligned SYNC characters. If the framer is enabled (RF = HIGH), the data byte boundaries are aligned to any incoming K28.5 characters found in the serial data. $\overline{\text{RDY}}$ ceases its normal BIST behavior and rests HIGH while the framer waits for a K28.5 character. The timing for the $\overline{\text{RDY}}$ pin to be forced HIGH is the same as the timing discussed in the preceding sections on entering framing (i.e., $6t_B$ after RF is latched HIGH). When a K28.5 character is found, $\overline{\text{RDY}}$ will pulse LOW for one clock cycle. During this cycle, $\overline{\text{RDY}}$ falls on bit time five and then rises on bit time one of the next clock cycle. $\overline{\text{RDY}}$ then resumes its normal BIST behavior after one more clock cycle (see *Figure 13* and *Figure 14*).

Figure 13 shows RF asserted HIGH (framer enabled) while BIST is in the middle of checking the data. $\overline{\text{RDY}}$ initially rests LOW and then transitions HIGH when the framer is enabled. When a K28.5 character is found, $\overline{\text{RDY}}$ pulses LOW and then rests HIGH again. One cycle later, $\overline{\text{RDY}}$ transitions LOW as it resumes its normal BIST behavior (resting LOW during BIST).

Figure 14 shows $\overline{\text{RDY}}$ behavior while BIST is waiting for the start of BIST sequence. Initially, $\overline{\text{RDY}}$ rests HIGH while waiting for the start of BIST sequence. When RF is asserted HIGH, the framer checks the

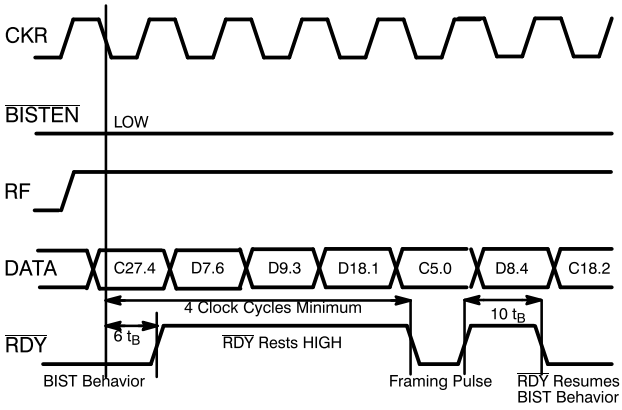

Figure 13. $\overline{\text{RDY}}$ While Framing in BIST

serial data for a K28.5 character. $\overline{\text{RDY}}$ pulses LOW when a K28.5 is encountered and then returns HIGH. $\overline{\text{RDY}}$ then returns to its normal mode of operation (resting HIGH until start of BIST is received).

If RF is deasserted before a K28.5 is found by the framer, $\overline{\text{RDY}}$ will resume its normal BIST behavior on the next clock cycle.

Enabling the framer while in BIST Mode may cause the BIST data to become temporarily misaligned. If the enabled framer encounters the alias K28.5 character in the BIST data stream, the BIST data will be aligned to the incorrect byte boundary. This will result in a large number of errors reported on the RVS (Receive Violation Symbol) pin until the data is framed again to one of the properly aligned K28.5s. If RF is asserted HIGH for less than 2048 clock cycles, the BIST data will be misaligned each time the alias K28.5 is found (once per BIST loop).

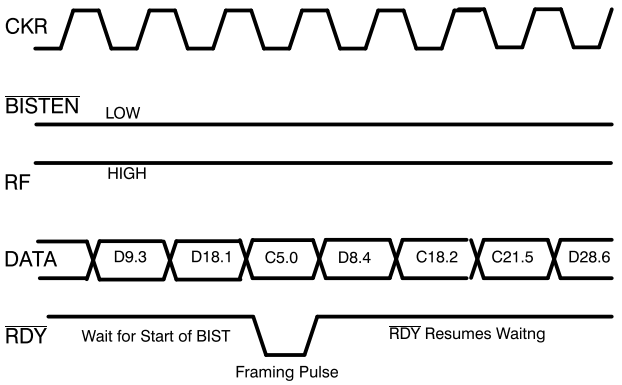

Figure 14. $\overline{\text{RDY}}$ While Framing in BIST

If RF is asserted for more than 2048 clock cycles (>4 BIST Loops), the double-byte framer will be enabled, and the framer will no longer frame the data to the alias K28.5 character.

Conclusion

The Receiver $\overline{\text{RDY}}$ pin indicates the status of the control logic and data pins in various modes of operation. The behavior and timing of the $\overline{\text{RDY}}$ pin have been optimized for easy integration with interface control logic and FIFO memories. The detailed information contained in this application note should serve as an aid when integrating the $\overline{\text{RDY}}$ pin into the interface logic.

Notes

1. Datasheet timing parameters that are defined in terms of bit times (t_B) include additional timing margin to account for internal buffer and routing delays and output load (e.g., $t_A = 2t_B +4/-2$ ns).