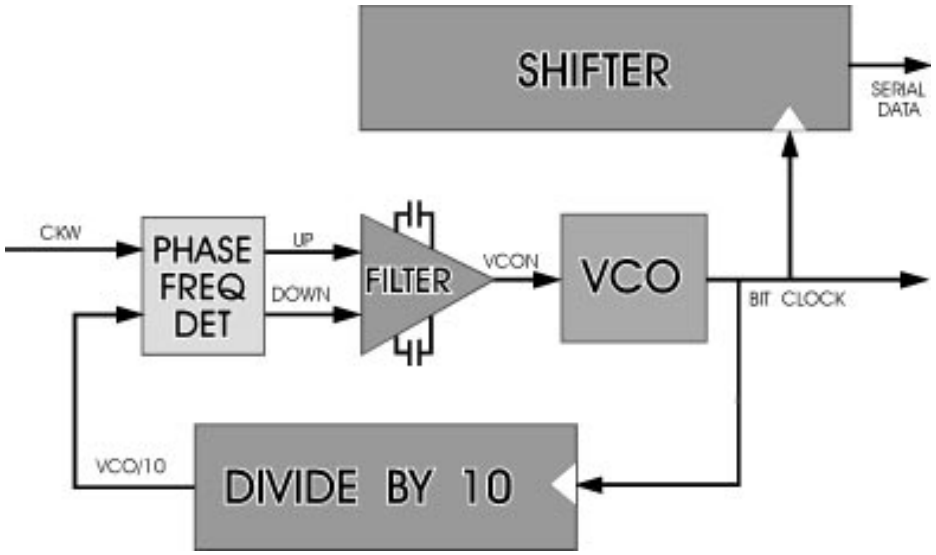


Figure 13. HOTLink Transmitter PLL Block Diagram

HOTLink Transmitter Jitter

The PLL used in a Transmitter application (clock multiplier) is intended to provide a high-speed, stable clock that tracks a low-speed reference (CKW in *Figure 13*). This clock (Bit Clock) is used to run the parallel to serial converter and all of the internal logic in the HOTLink Transmitter.

Jitter is an undesirable and often unpredictable misplacement of any particular transition from its ideal position. Transmitter output jitter can be characterized as Random or Deterministic Jitter, RJ and DJ respectively. It can further be subdivided into Intrinsic Jitter, Transferred Jitter, or Injected Jitter.

To separate the various types of jitter, carefully designed tests were performed on HOTLink parts selected from the full spectrum of manufacturing tolerances. Tests were designed to separate the effects of Power Supply, Clock Sources, and various PLL characteristics. Manufacturing tolerances include variations in all types of resistors used in the design, characteristics of Bipolar and CMOS transistors, and other normal process variations. Environmental effects include V_{CC} variation over at least the full specified range, and ambient temperature variation over the full military and commercial ranges.

Unless otherwise noted in the following text, static variations in power supply levels (4.5V to 5.5V), ambient temperature (−55°C to 125°C), and process variations (within manufacturing tolerance limits) cause virtually no change (within the accuracy of the measurement system) to any jitter tolerance or PLL characteristic. This should be true for any *well-designed* PLL, though it is often not true for all products in the marketplace.

Transmitter Random Jitter

Random Jitter is an undesirable and unpredictable misplacement of any particular transition from its ideal position that cannot be correlated to either data-stream content, or parameters of the hardware. To separate Random Jitter from the other effects, the HOTLink is configured to send various square-wave patterns. This minimizes any possible deterministic (DJ) effects caused by loading or variations in internal circuit delays. The set-up used to measure HOTLink Random Jitter is shown in *Figure 14*. The clock source was a combination of an HP 8656B and HP 8131 generator chosen to give the lowest possible input jitter. Other generators, described later in this application note are also satisfactory for this clock source. The output was measured on both an HP 54720D and a Tektronix 11801 Digital Sampling Scope, each of which have sufficient sampling bandwidth to accurately show the performance characteristics of the device under test.

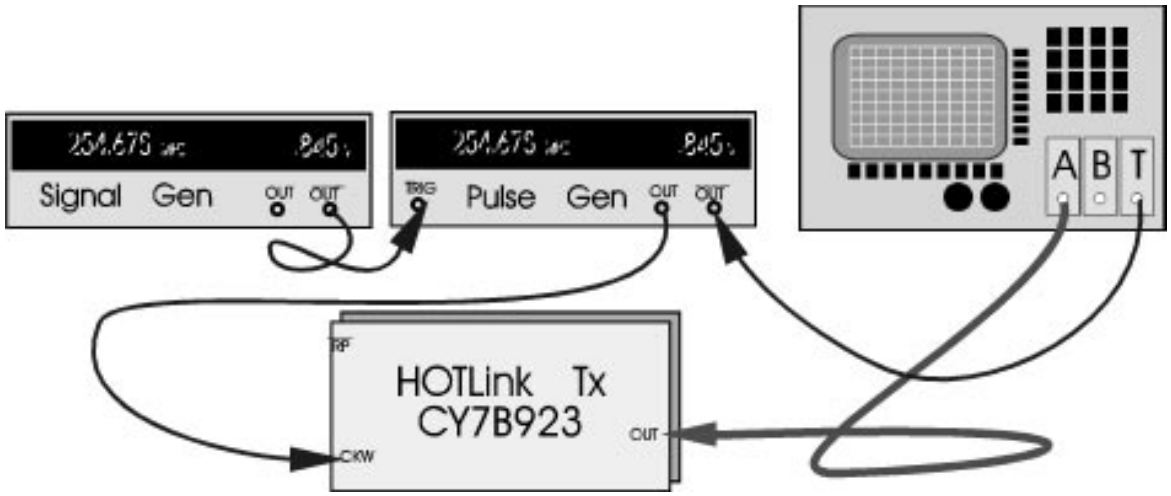
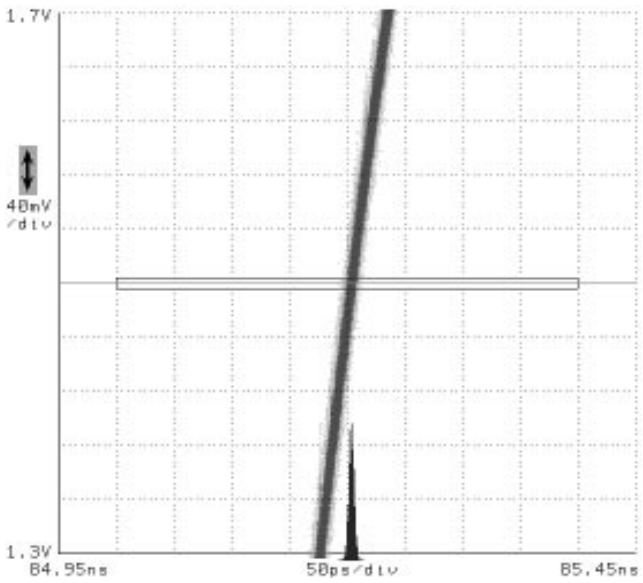


Figure 14. HOTLink Transmitter Random Jitter Set-Up

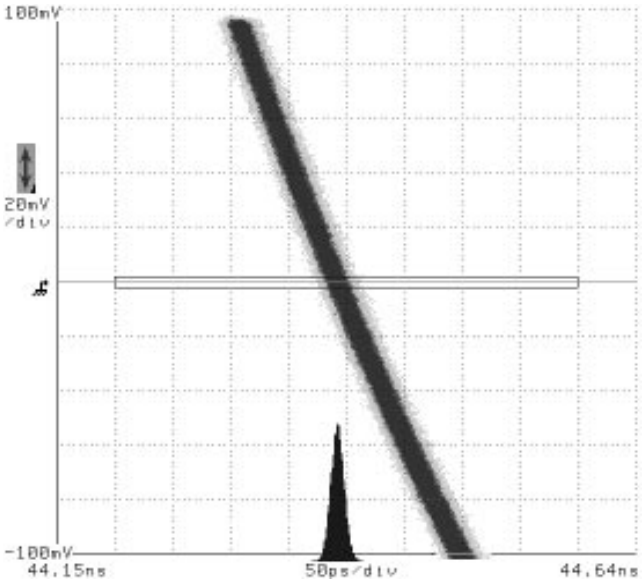
Random jitter measured in this way is shown in *Figure 15*. In virtual time, the "random" characteristic can be seen in these histograms taken on a Tektronix 11801 Digital Sampling Oscilloscope.

The left histogram in *Figure 15* shows the quality of the signal used to gather the data that follows. The input clock coming from an HP8656B frequency synthesizer, buffered through an HP8131 Pulse generator, has minimal jitter. This TTL input clock source adds a negligible amount of jitter to the output jitter measurements that follow. Other generator/buffer combinations are possible, but if there is any appreciable jitter at this point, it will be impossible to separate the input jitter from the jitter accumulated in the part under test. Other tests (described later) will show the effect of noise at the CKW input.

Cycle-to-cycle jitter out of the HOTLink while sending a "perfect" bit-rate square wave, measured one bit away from the output edge used to trigger the scope, is very small. This is a measure of the jitter that can accumulate between adjacent VCO clocks



RMS = 2.39 ps Pk−Pk = 22 ps



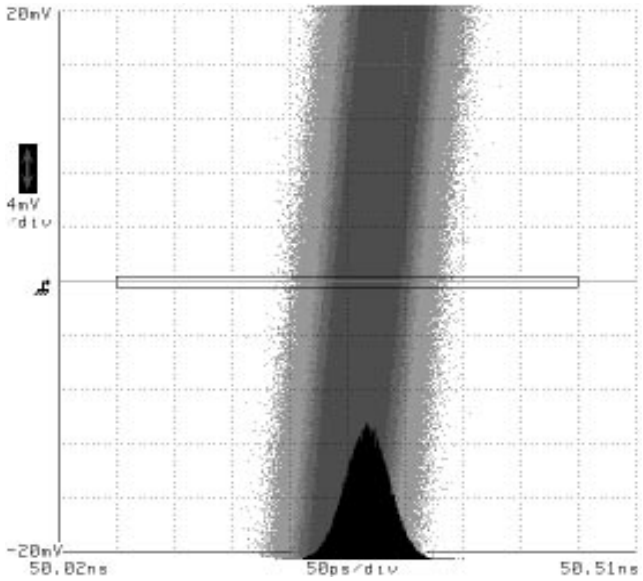
RMS = 5.89 ps Pk−Pk = 44 ps

Figure 15. Histograms of CKW Source and OUTA± One Cycle Away

in the multiplier PLL. Since this measurement (right histogram in *Figure 15*) was triggered and measured on the same output, and the scope was not constrained to sample at any particular rate, this photo shows the superposition of all possible bit positions. It also shows the (small) magnitude of Deterministic jitter built into the output circuitry.

The serial outputs of HOTLink are PECL differential signals that must be combined differentially in the front end of the sampling scope to provide an accurate measurement of both the signal transition and any jitter present on those transitions. *Figure 16* displays the differential measurement of the accumulated jitter on the OUTA± outputs of the HOTLink Transmitter. This is a measure of the total jitter accumulation through the entire PLL and output circuit while sending a "perfect" byte-rate square wave.

The wide vertical bar shows the accumulated jitter measured in 100,000 samples of the 0-to-1 transition while being triggered by the CKW reference. The different shades of gray in the vertical bar represent different concentrations of signal samples that occurred at that specific time/amplitude coordinate. The darker the sample point, the more samples that occurred at that point. The very center of *Figure 16* contains a narrow rectangle centered around the



RMS = 19.13 ps Pk−Pk = 164 ps

Figure 16. HOTLink Transmitter OUTA± Rj vs. CKW

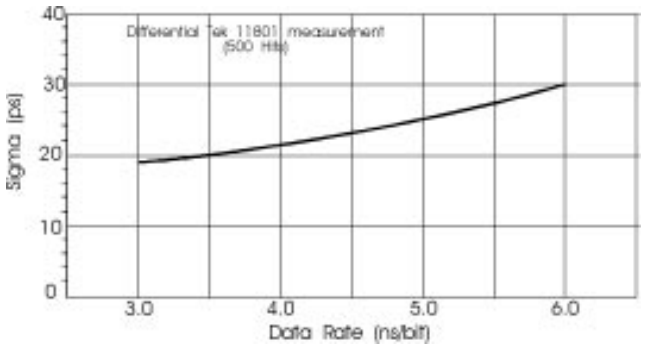


Figure 17. HOTLink Transmitter Random Jitter as a Function of Frequency

HOTLink Receiver threshold region. All samples that occur within this rectangle are plotted in the black histogram at the bottom of the figure. The Gaussian shape of this curve confirms that the jitter is truly random in nature.

While there is a slight increase in output jitter as the operating frequency decreases (see *Figure 17*), there is no appreciable change in HOTLink jitter due to V_{CC}, temperature or process variation.

In contrast to the virtual-time measurements illustrated in the previous figures, real-time measurements allow an insight to the behavior of the HOTLink Transmitter in terms of sequential events. *Figure 18* shows the edge displacement from the ideal location of all sequential rising edges of a continuous data stream. In this sequential, real-time measurement, it can be seen that there is no obvious or repetitive pattern to the jitter, confirming the validity of the virtual-time measurement. A minor pattern is visible in the running-average histogram, that shows a small amplitude, continuous oscillation in the sign of the edge misplacements. Peak-to-peak deviation in the real-time illustration is smaller than that indicated in the virtual-time measurement. This is consistent with the large difference in the number of samples in each, and the fact that many of the extreme excursions that occupy the tails of the distribution may not be PLL variations, but are probably caused by pulse-noise injected into some logical or measurement function.

The pattern of jitter does not change appreciably when the output pattern changes from one cycle-per-byte to one cycle-per-bit (see *Figure 19*). The peak excursion remains about the same, and the distribution is similar.

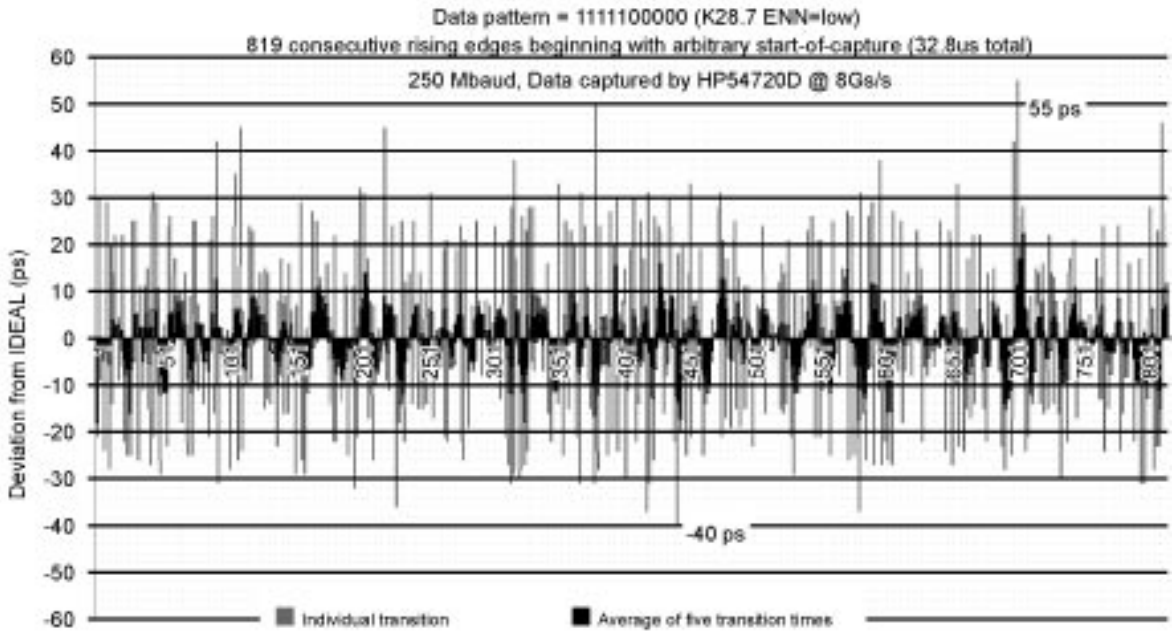


Figure 18. Real-Time HOTLink Transmitter-Output Byte-Rate Jitter

Transmitter Deterministic Jitter

Deterministic jitter is an undesirable and often difficult-to-predict misplacement of any particular transition from its ideal position that can be correlated to the content of the data stream or some characteristic of the circuit or hardware. To measure deterministic jitter attributable to the internal circuitry of the HOTLink Transmitter, the parts were measured in several ways to separate the different possible DJ sources. (For all of the following DJ measurements, repetitive output patterns are averaged to remove RJ effects.)

The basic Deterministic Jitter tests fall into two categories:

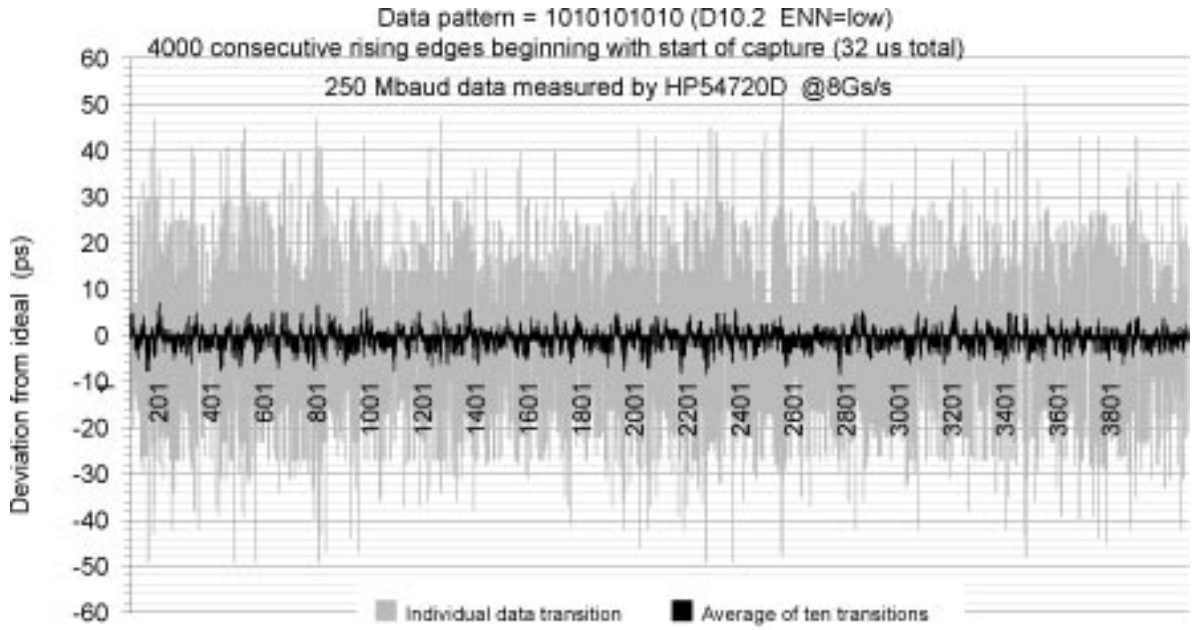


Figure 19. Real-Time HOTLink Transmitter Bit-Rate Jitter Output

1. There could be DJ that causes edges to be misplaced because of variations of internal rising and falling delay or variations of internal delays caused by the spacing between adjacent transitions (e.g., internal logic swing limitations or flip-flop metastable-delay effects).
2. There could be DJ that is caused by some deterministic PLL-multiplier effect which misplaces the internal clock edges from their ideal transition time (e.g., PLL phase corrections might cause bit-0 to be always early, bit-2 always late, and the others on time).

Deterministic Jitter as a Function of Data Pattern

To check for internal delay effects and sensitivity to data content, the HOTLink transmitter was configured to send various data patterns. *Figure 20* shows how the bit position is affected by pulsewidth and pattern-content of the serial bit-stream. This test is performed by measuring the exact timing of a single data transition as other transitions occur at various other bit positions and pulse spacings. By plotting the exact transition time against the expected transition-time, variations in internal delay become apparent. This is a test of the output buffer and circuits in the serial output logic, because it checks the position of a single transition as the pulse width preceding it changes from nine bits to one bit LOW.

HOTLink manages to place any particular edge within ±10 ps of the ideal location regardless of data pattern. In this test it is impossible to separate pulse distortion from slight propagation delay changes. The 50% duty cycle pattern was used as the reference location for the "ideal" pulse position. The absolute position of the rising edge was measured as the ten-bit data pattern was stepped through all nine of the possible pulse widths. Edge placement is not significantly affected by temperature or process variation. The change in edge displacement in the figure above is mostly caused by V_{CC} variation and may be related to output load currents variation.

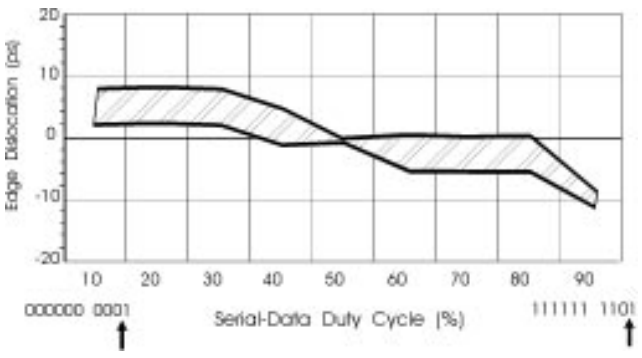


Figure 20. Data Dependent Edge Displacement

Deterministic Jitter Caused By PLL Corrections

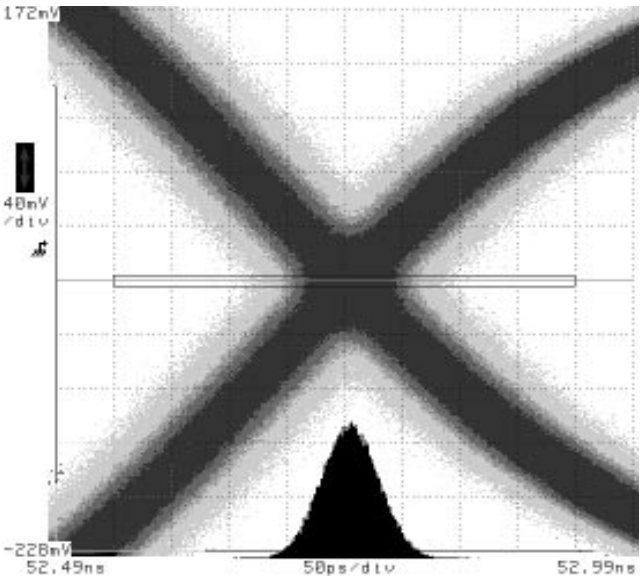
By causing the Transmitter to send an alternating 1-0-1-0... bit pattern and synchronizing the measurement system to the byte rate clock, it is possible to detect misplacement of internal clock transitions. In this test, performed by measuring the exact time of each voltage transition (averaged to remove random jitter effects), and plotting it against its expected transition-time, PLL phase corrections and clock-synchronous noise will appear as fixed, repetitive displacements from the ideal position. The square-wave bit pattern minimizes delay effects which might otherwise be present.

The results of this evaluation showed that there were no deviations observable within the measurement accuracy of the test equipment. Extensive testing showed less than 2 ps deviation from the ideal position of all ten of the output transitions, regardless of frequency.

Total Transmitter Jitter While Sending BIST

As a measure of total transmitter jitter, the tests were repeated while sending the built-in self-test (BIST) sequence. In contrast to the special patterns which were used to measure the various components of overall jitter, this test is a more comprehensive measure of real HOTLink performance, since it would highlight any effect that might have been obscured by the individual jitter-component tests.

The scope photo in *Figure 21* shows the jitter characteristics of the HOTLink output while sending the BIST pattern. This 511-byte pseudo-random pattern includes all of the legal data patterns in the 8B/10B code, and is a good representation of a typical data transmission. The resulting jitter includes all of the random and deterministic jitter accumulated by the clock source, the multiplying PLL, and the internal logic and output circuits.



RMS = 25.1 ps Pk−Pk = 228 ps

Figure 21. HOTLink Transmitter OUTA± Total Jitter in BIST vs. Bit Rate Reference

Transmitter Jitter Transfer Function

PLL output jitter can be affected by the noise characteristics and stability of the clock source used as its reference. The closed-loop transfer function of this type of PLL is a low-pass filter. Noise components below the rolloff frequency (f_{-3dB}) of the PLL will be passed unattenuated and those above f_{-3dB} will be attenuated. By injecting a measurable and controlled amount of noise (jitter) into the clock reference as shown in *Figure 22*, the PLL transfer characteristic can be measured.

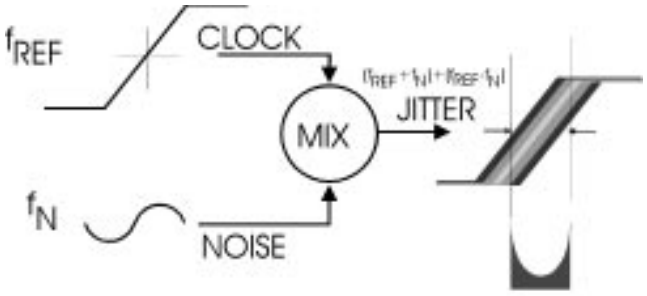


Figure 22. Clock-Jitter Generated by Mixing Noise into CKW

In this configuration (*Figure 22*), the noise source is added to the clock source with a resistive mixer. Because the clock source has a significant ramp rate, the addition of the noise will cause a controlled variation in the effective threshold crossing, thus causing jitter. The noise source can be any controlled source, but for this test, it was a good quality sinewave generated by a stable generator. The amplitude was adjusted to create the desired CKW jitter amplitude (ns Pk−Pk), and the frequency was varied over a wide range while the output jitter was monitored on OUTA±. The graph in *Figure 23* shows the relationship between input and output jitter at various input jitter frequencies as the jitter frequency is increased from about 10 kHz to over 70 MHz.

While the vertical axis of this type of chart usually is expressed as a "gain" term, and uses units of dB (i.e., 20 log out/in), this data is being presented as a pure ratio of input to output jitter. This allows a clearer visualization of jitter magnitude, and shows that for

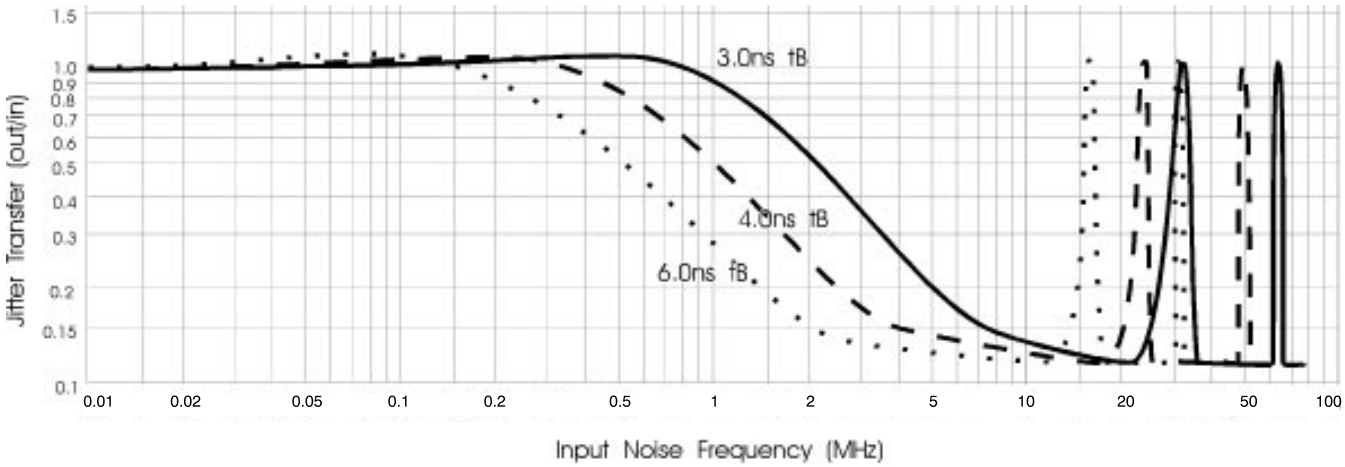


Figure 23. HOTLink Transmitter Jitter Transfer Function

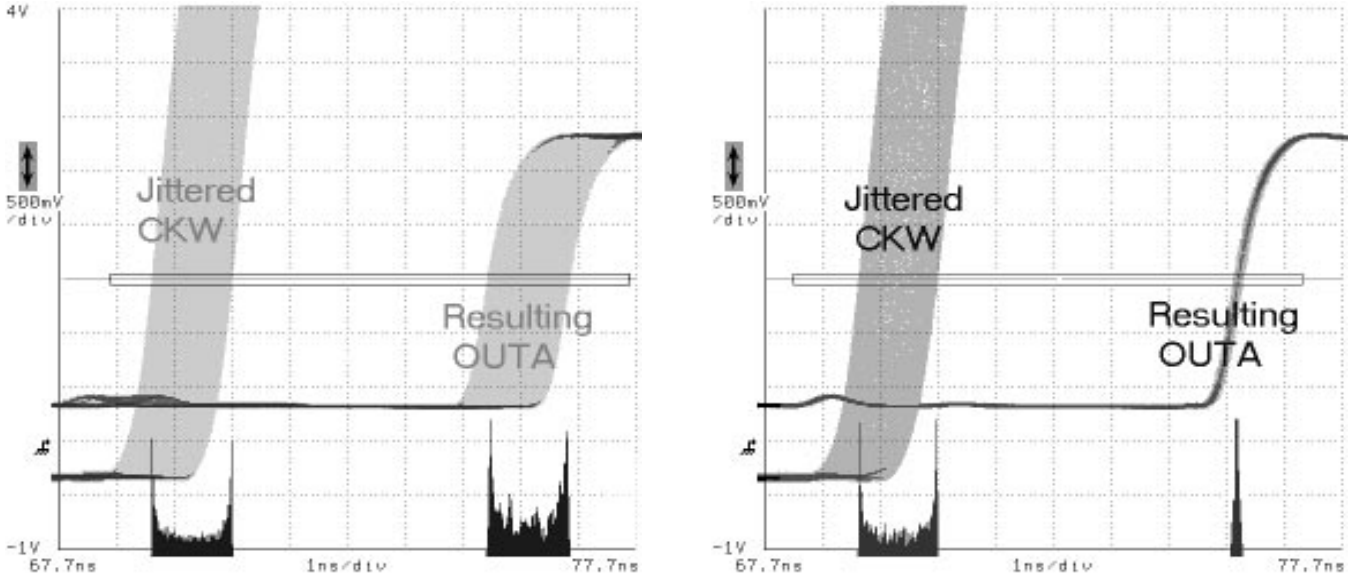


Figure 24. Serial Output Jitter Varies as a Function of Input Noise Frequency

all frequencies of operation and noise, the output jitter falls to approximately the same "noise-floor." By maintaining the vertical log scale, it is obvious that the effect being illustrated, is the same as the closed-loop PLL transfer function described earlier.

As expected, low-frequency jitter passes through the PLL unattenuated. Higher frequencies are attenuated until the jitter frequency approaches the Reference-Clock frequency. This jitter-feed-through peak at about the reference frequency is the result of the sum-and-difference frequencies that naturally result from mixing. A significant frequency component is generated at the "difference" between CLOCK (f_{REF}) and NOISE (f_N) sources. When this "difference" frequency falls within the PLL filter bandwidth, it passes unattenuated to the output of the PLL and appears as jitter exactly as if it was caused by an equivalent low-frequency input-noise source. This effect was enhanced by using a single frequency noise source. The energy at any particular frequency of a wide-band noise source is relatively small, but would feed through in exactly the same way. Narrow-band noise sources that operate synchronously with the HOTLink CKW input rate might cause more of these "mixed-down" frequency components that would also feed through and emerge as output jitter.

The bandwidth of the HOTLink Transmitter PLL varies slightly as a function of the operating frequency as is shown in *Figure 23*. (tB = 1/baud; tB = 6 ns = 160 Mbaud, etc.) This variation is attributable to variations in VCO gain that are a function of operating rate.

The scope traces in *Figure 24* graphically show the jitter feed through from the TTL-CKW input to the PECL outputs of the HOTLink Transmitter. Low jitter frequencies pass through unattenuated, and high frequencies are significantly attenuated. For high-frequency input jitter, the only jitter remaining on the output is roughly equivalent to the intrinsic jitter of an undisturbed PLL.

V_{CC} Jitter Transfer Function

To characterize HOTLink output jitter characteristics in the presence of noise carried on the power supply, the Random Jitter set-up was modified as shown in *Figure 25*.

In this test the power supply was intentionally disturbed. By injecting a measured amount of noise into the V_{CC} pins of the HOTLink Transmitter (using an external driver), the jitter effects of power supply noise could be observed.

As expected, when the power supply is disturbed, the output will contain some additional jitter. In-

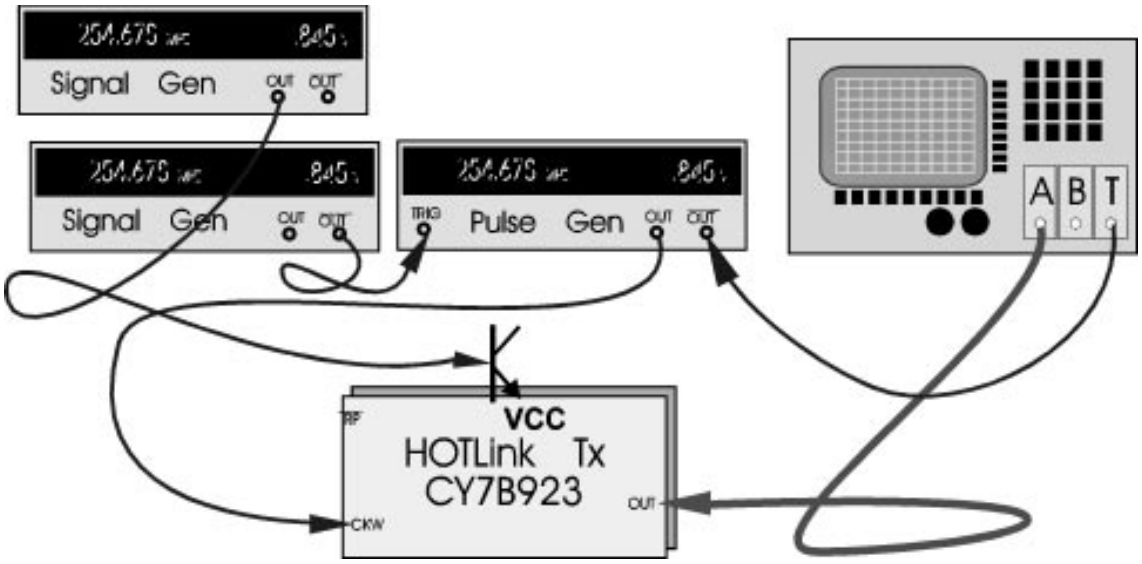


Figure 25. HOTLink Transmitter V_{CC} Coupled Jitter Set-Up

creasing amplitude disturbances cause increased jitter amplitudes. It would normally be difficult to create this much noise on normal system boards because of the normal power supply bypassing that is usually applied to this type of component. Large amplitude V_{CC} spikes are removed by the bypass capacitors.

As the V_{CC} noise frequency is varied across the various frequencies, the jitter out also varies. At low frequencies of noise, the jitter is small, and at high noise frequencies the jitter is also small. At about the PLL roll-off frequency (as measured in the previous analysis), the jitter output increases (see *Figure 26*).

Transmitter PLL Lock Time

Multiplying PLL lock characteristics are mostly a function of the internal loop dynamic characteristics. While the loop is changing the clock period

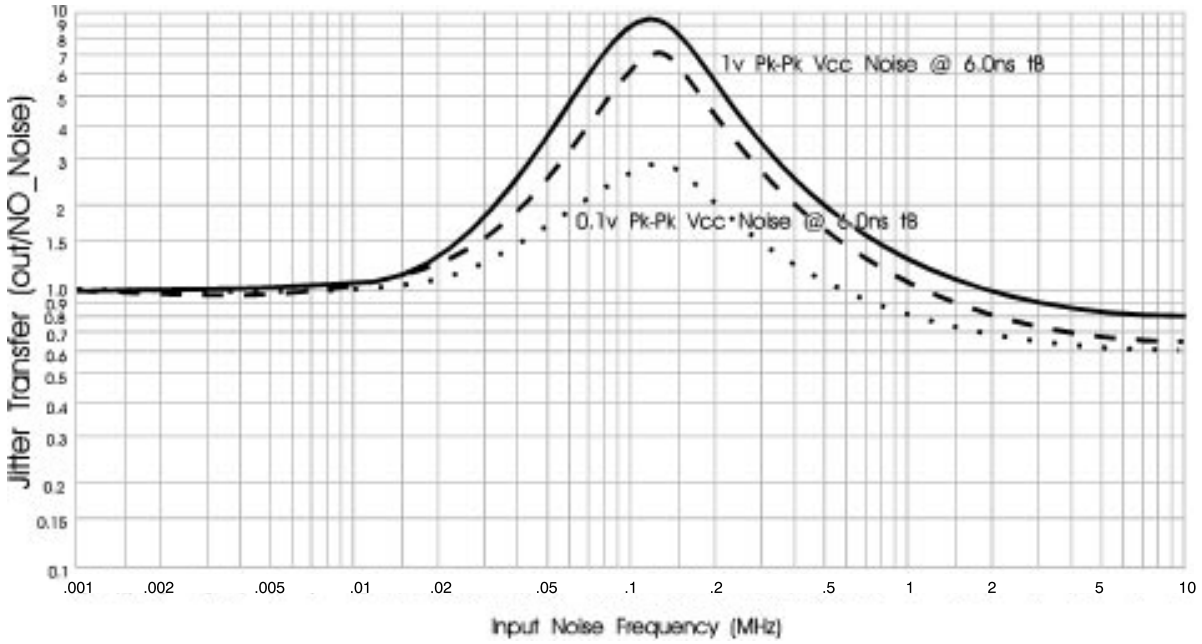


Figure 26. HOTLink Transmitter V_{CC} Coupled Jitter Transfer Characteristic

from one frequency to another, the transition is not monotonic as might be expected, but appears to oscillate about the acquisition-trend line until the frequency falls within the PLL "Lock Range." This effect is a result of the normal characteristics of the Phase Frequency Detector (PFD) and the Loop filter. The PFD output is a continuously varying series of pulses that cause the VCO to change frequency in the desired direction, but the resulting pulse widths are not constant. The graph in *Figure 27* shows each of the Bit-Clock periods during the PLL "re-lock" progression while the loop locks to a higher and a lower frequency.

The Bit-Clock period listed in *Figures 27* and *28* is the period of the internal VCO inside the HOTLink Transmitter. While this signal is not directly observable at a HOTLink Transmitter pin, its period may be directly calculated from measurements made at the serial output (OUTA±) pins. In this test the serial data pattern was set to the equivalent of a K28.7 special code (0000011111), fixing the bit-clock period at one tenth the interval between output rising transitions.

The two locked frequencies were selected to be the minimum and maximum actual operational limits of the part under test. Cycle-by-cycle times were recorded in a continuous stream using an HP54720D. The frequencies used for these illustrations are well outside the datasheet operational limits of HOTLink, but were the actual functional limits of this particular (typical) part. While all parts behave in a similar manner, some have slightly higher or lower operational frequency limits. The acquisition rates vary slightly with temperature, being slowest at higher temperatures.

The PLL behavior is slightly different when the reference clock has been absent for some time (see *Figure 28*). Instead of immediately beginning to acquire the new frequency, there is a time after CKW begins but before there is any change in the VCO frequency. This time is required for the internal control nodes to move from their "ranged-out" levels (resulting from the PLL trying to track to zero or infinity Hz) to within the compliance-limits of the amplifier and VCO. After the change begins, it moves at the same rate as for the previously described cases.

When CKW is removed, the loop immediately begins to slew toward the lowest possible speed. The transition does not have the "jaggies" typical of a loop tracking to another clock rate, because there are no reference clock edges to modulate the PFD output. The frequencies shown in this illustration are well outside the data sheet operational limits of HOTLink, but were the actual functional behavior of this particular (typical) part. While all parts behave in a similar manner, some have slightly higher or lower frequency limits. The acquisition and slew-rates were similar but vary slightly with temperature, being slower at higher temperatures.

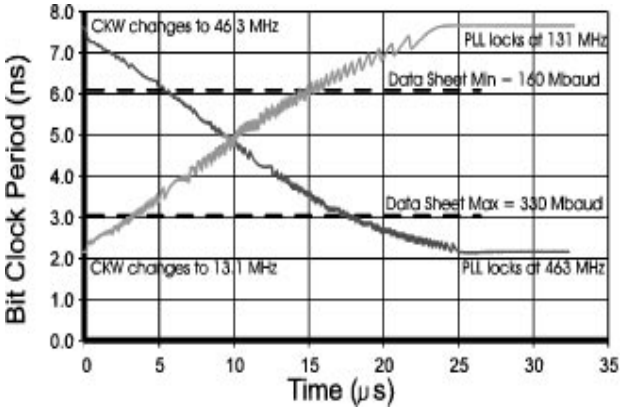


Figure 27. Transmitter PLL Acquisition Characteristic (from Locked to Locked)

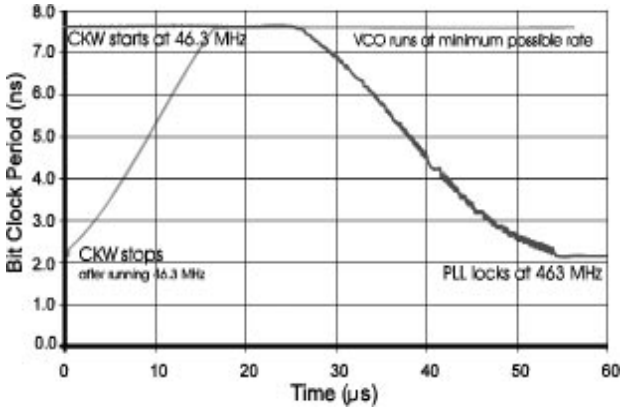


Figure 28. Transmitter PLL Time to Lock (Quiet to Locked)