Summary

The following summary data is representative of the sample tested and described in this report. This evaluation included parts from across the full manufacturing spread, which were tested over the full range of temperature, voltage and frequency of operation. This data is representative of HOTLink in-system performance, but because of the small sample size tested, it cannot necessarily be assumed to be worst case.

Table 4. Summary of HOTLink Jitter Characteristics

Parameter	Characteristic		Condition
Tx Cycle-Cycle Random Jitter	< 6 ps RMS	< 50 ps Pk−Pk	
Tx Input-Output Random Jitter	< 20 ps RMS < 22 ps RMS < 30 ps RMS	< 175 ps Pk−Pk < 190 ps Pk−Pk < 250 ps Pk−Pk	(330 Mbaud) (250 Mbaud) (160 Mbaud)
Tx Data Dependent Edge Displacement		< ±10 ps Pk−Pk	
Tx PLL Deterministic Edge Displacement		< ±2 ps Pk−Pk	
Tx Total Transmitted-Data Jitter	< 26 ps RMS < 28 ps RMS < 36 ps RMS	< 230 ps Pk−Pk < 250 ps Pk−Pk < 300 ps Pk−Pk	(330 Mbaud) (250 Mbaud) (160 Mbaud)
Tx Closed-Loop Bandwidth (3 dB)		1.5 MHz 0.6 MHz 0.3 MHz	(330 Mbaud) (250 Mbaud) (160 Mbaud)
Tx Re-Lock Rate (Locked to Locked)		> 11 MHz/µs > 9 MHz/µs	Typical Hot
Tx Crash Rate (From CKW Stop)		> (45 MHz +19 MHz/µs) > (21 MHz +16 MHz/µs)	Typical Hot
Tx Lock Time (Quiet to Locked)		< 45 ms < 60 ms < 80 ms	Typical (160 Mbaud) Typical (330 Mbaud) Hot (330 Mbaud)
Rx Error-Free-Window (Static Alignment)		> t_B − 250 ps	**Note:** t_B = 1/baud rate (ns)
Rx Random Jitter Tolerance (BER<$1x10^{-12}$)		> t_B − 500 ps	
Rx DCD Tolerance (BER < $1x10^{-12}$)		> 0.42 x t_B	
Rx DDJ Tolerance (BER < $1x10^{-12}$)		> 0.62 x t_B > 0.82 x t_B > 0.95 x t_B	(330 Mbaud) (250 Mbaud) (160 Mbaud)
Rx Total Jitter Tolerance (BER < $1x10^{-12}$)		> t_B − 500 ps	
Rx Input-Output Random Jitter	< 39 ps RMS < 25 ps RMS < 24 ps RMS	< 224 ps Pk−Pk < 180 ps Pk−Pk < 148 ps Pk−Pk	(330 Mbaud, no jitter BIST) (250 Mbaud, no jitter BIST) (160 Mbaud, no jitter BIST)
Rx CKR Cycle-Cycle Peak Jitter (does not include reframing CKR-stretch)		< 100 ps < 300 ps < 0.7 x t_B < 1.0 ns < 1.5 ns	(No input jitter, single data) (No input jitter, random data) (Worst case input DDJ) (Data Phase Hop only) (Loss of Lock)
Rx CKR Maximum Instantaneous Offset Freq.		< REFCLK ±5%	(Unstable, range control active)

Table 4. Summary of HOTLink Jitter Characteristics (continued)

Parameter	Characteristic		Condition
Rx CKR maximum continuous offset freq.		< REFCLK ±0.25%	(Stable, range control inactive)
Rx Run-Length Limit (without cycle slip)		> 200 t_B > 200 t_B > 200 t_B	(330 Mbaud) (250 Mbaud) (160 Mbaud)
Rx Phase Acquisition Time (BER < $1x10^{-12}$)		< 60 t_B < 250 t_B	(typical, <180 degree hop) (includes 180 degree hop)
Rx Frequency Acquisition Time (BER < $1x10^{-12}$)		< 50 t_B < 700 t_B	(delta−freq ≤ ±0.2%) (delta−freq > ±0.2%)
Rx Closed-Loop Bandwidth (3 dB)		9.0 MHz 4.5 MHz 2.5 MHz	(330 Mbaud) (250 Mbaud) (160 Mbaud)
Rx REFCLK Re-Lock Rate (Locked to Locked)		> 2 MHz/µs	
Rx Lock Time (REFCLK Quiet to Locked)		< 200 µs +2 MHz/µs	
Rx Crash Rate (from REFCLK & DATA stop)		> 80 ps/µs	

Hints to Improve Measurement Accuracy

- Use differential scope inputs instead of single-ended measurement systems to remove common-mode amplitude variations from timing jitter. Minor variations in power supply levels that are passed through to the complementary PECL outputs are ignored by the differential receiver, and so should be removed from the measurement. Systems with only single-ended scope inputs should carefully monitor V_{CC}-coupled signals, since a few millivolts of vertical shift can result in several picoseconds of apparent delay variation. Faster edges and minimal loading can minimize the problem, but not eliminate it.

- Random jitter measurements should be taken at the approximate center of the differential swing to minimize "scope arithmetic" and round-off errors that obscure actual performance.

- Bypass PECL load circuits to remove "load-ringing" effects. Power supply and PC board impedance adds directly to the impedance of the termination circuit. Careful attention to power supply bypassing minimizes load related errors.

- AC coupling of input, output, and measurement signals cause unexpected problems if the wave form is non-repetitive, not DC balanced, or if the signaling rate changes. The components used for blocking the DC voltage in the signal will exhibit impedance variations because of their reactive nature. They almost always have non-monotonic transfer functions, and often have self resonant characteristics that are not well documented. High quality DC-blocking modules from HP and other sources are typically specified to be effective over a very wide frequency range (e.g., HP 11742 Blocking Capacitor is useful at 0.01 through 26.5 GHz), but the more common "capacitor soldered on a board" is usually unsuitable for critical measurements.

- Simplified, high quality PECL measurements are possible using the connection shown in *Figure 48*. This a derivative of the standard 80Ω/130Ω Thévenin termination for PECL in which the lower 50Ω of the 130Ω is provided by the scope input impedance. By using low impedance, pas-

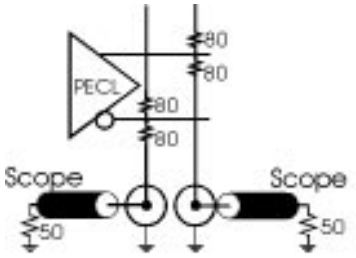

Figure 48. PECL Scope Probe

sive probes to maintain the full input bandwidth of the scope, and by separating the scope probes from the loads, a more representative measurement is possible. This connection yields a probe with an approximate attenuation of 2.6:1, instead of the more usual 10:1 probes. For critical voltage measurements, each such connection must be calibrated, because the actual attenuation factor will depend on the actual values of resistor used for the PECL termination. Since most AC measurements are differential and use only relative voltage levels, this connection is preferred to more expensive probe configurations. Of course, good low-capacitance layout and good quality 50Ω cables and connectors are required to maintain the bandwidth of the measurement system. When the scope is not connected to the test points, a substitute 50Ω resistor should be connected to allow the PECL outputs to operate correctly.

Test Equipment

Relevant Characteristics of Measurement Equipment

Good quality, high-bandwidth, measurement equipment is mandatory to determine the actual performance of the HOTLink and the systems used to test it. To gain an accurate insight into 300-MHz transmission lines, and the picosecond variations which characterize the components that define the limits of operation, it is necessary to use test systems capable of making accurate measurements up to multiple Gigahertz. The list that follows (and the short listing of their relevant attributes) are not the only applicable measurement systems, just the ones used by this design team.

HP54720D High-speed, Real-time, digital sampling scope

Sample Rate = 8 Gigasamples/second

Trigger Jitter < 10 ps

Bandwidth = 2 GHz

1 GHz on each channel with 54721A Input module

2 GHz on single channel with 54722A Input module

This high-performance scope offers the opportunity to observe the actual wave shape with its “real-time” capability. In contrast with the more traditional sampling scope, this instrument will record the signal on its inputs at 125 picosecond intervals until its input buffers are full. The 54720D has the ability to place the triggering event at the beginning, middle, or end of the stored waveform, which allows it to capture random and non-repetitive events.

Tek 11801A Digital Storage Oscilloscope

with SD−22, 12.5-GHz Sampling heads for precision low-impedance measurements

with SD−14, 3.0-GHz Sampling heads for low-load, high-impedance measurements

and DL−11, 5-GHz Delay Line for measurements at the time of the trigger event

Trigger Jitter < 3 ps

Bandwidth > 20 GHz, bandwidth on each channel limited by the sampling head. (SD−22 or SD−14)

This high-performance scope has sufficient bandwidth to observe the actual performance of the PECL outputs of HOTLink. Lower bandwidth scopes and probes often give an erroneous impression of the voltage waveform being measured. The 11801A is best used for measuring repetitive waveforms, since it only accumulates a “dot” for each trigger. Accumulated over

time, this is sufficient for observing repetitive wave forms, and its color-graded histogram ability is very useful for capturing jitter performance.

HP 8560A Spectrum Analyzer

50 Hz to 2.9 GHz

Used for monitoring jitter transfer tests and various clock source attributes to assure the accuracy of the bench setup. The displays that appear on a spectrum analyzer are often ambiguous, since frequency, phase and amplitude variations all cause similar indications. This is a fun instrument to use, but must be interpreted with care. It usually gives more information than can be fully understood, but does offer another view of the system under test from the frequency domain.

HP 54610 500-MHz, 2 channel oscilloscope

This is a small, relatively portable bench scope (i.e., about one cubic foot and can be carried with one hand, in contrast to the other scopes which require a dedicated cart) used for monitoring the function of various bench set-ups and the functionality of the part under test. It has sufficient bandwidth to give an accurate picture of the circuit under test, but is too slow to give accurate results in the previously described precision tests. These scopes are typically used for setting up the various generators, clock sources, and data generators, and for cross-checking the validity of many of the measurements. They were not used to gather actual data, but offer sufficient performance to see that the set-up is working as expected.

Clock Sources

Crystal oscillators are typically used in operational systems because of their stable, predictable, low noise characteristics (as well as their low cost). They were found to be unsuitable for the previously described tests, because of their low-frequency delay and wander characteristics. These unrepeatable effects obscure the jitter characteristic being measured. In operational systems, these effects will cause *no* reduction in link performance, and will merge into the unmeasurable, insignificant background characteristics of the system. To gather the precision information described in this application note, several clock and data sources were used. The list that follows (and the short listing of some relevant attributes) are not the only applicable clock sources, just the ones used by this design team.

RF Generators

HP 8656B Generator 0.1−990 MHz

HP 8647 Signal Generator 250 kHz−1000 MHz

Used as frequency reference generators because of their spectrally clean output, and their high frequency function. They generate small, ground referenced sine waves with great accuracy and are easily programmable from the panel or using a GPIB controller. These generators are typically used to trigger high-performance Pulse Generators, which produce the required levels and edge rates. The generators themselves have acceptable stability and jitter performance for most AC and functional evaluations, but are not sufficient for jitter related tests.

When triggered by a stable source, the jitter performance of the generator improves to almost that of the triggering reference.

Clock Generators

HP 8131A 500-MHz pulse generator

Pulse generators are used to generate the PECL and TTL clock and data sources for testing HOTLink products. The HP8131 can be used by itself or triggered by an RF source. It offers two independent channels with complementary outputs for each.

Wavetek 178 Function Generator
0−50 MHz Function generator

The Wavetek 178 is convenient for generating low frequency signals such as Receiver REFCLK and swept frequency-range tests. It has the capability to generate various wave shapes and can sweep its output fre-

quency across a wide range. It has good stability and is relatively "clean," but exhibits about 200 ps of low-frequency jitter.

Colby Instruments Pulse Generator PG−1000A

The Colby pulse generator is a very stable oscillator that is mechanically tuned, and offers very good spectral purity and good control. It suffers from slight frequency drift until it is fully warmed-up. The design of the instrument is very modular, and offers many specialized controls and options to meet various voltage translation and buffering needs.

Pattern Generators

Microwave Logic GigaBERT − 1400 TX

1.4 GHz max. clock rate

< 2 ps RMS clock jitter, < 20 ps Pk−Pk

No jitter added to output when divided by N to create Bit or Byte Clock

This instrument is actually a very high quality clock generator, packaged with a bit-rate data generator. It can be used for generating bit-clock inputs without the need of an external oscillator trigger source. It was used for many of the bit-rate referenced tests described in this application note by programming it to the required pattern.

Translators and Delay Generators

Colby Instruments
Custom clock buffer and translator box

This general-purpose translator box was used to convert between differential PECL and both true ECL (−5.2V referenced) and "zero-crossing" signals used in various tests. It can accept single-ended signals and return differential outputs with extremely fast edges and no appreciable increase in jitter noise. The inputs all include high quality transmission line terminators that simplify most bench configurations.

Colby Instruments Programmable Delay Line PDL−30A

This general-purpose, mechanical delay generator is capable of generating a repeatable and stable delay up to about 10 ns in increments as small as 1 ps. It is most useful for adjusting mismatched delay lines, and for creating desired skews between various signals. It is essentially a 50Ω transmission line that can be mechanically adjusted in small increments to change the delay. It is programmable by an external keyboard with a digital readout of programmed delay.

Home-Brew and Non-Commercial Test Equipment

Synthetic-DCD Jitter Generator

Duty Cycle Distortion (DCD) can be generated by the circuit shown in *Figure 49*. This circuit uses the stages in a 10H116 (ECL triple-differential amplifier) to perform

- Differential-PECL-input buffering
- Ramp generation
- Threshold shifting
- Level restoration
- Differential PECL output buffering

In this circuit the Transmitter data stream is fed through the Jitter Generator while the Receiver monitors and checks for correct operation. As the control voltage (Vj) input is varied between the 10KH V_{IL} and V_{IH} levels, the duty cycle of the data stream is corrupted in a repeatable and measurable manner. Either of the Vj inputs can be independently adjusted, or they can be differentially driven to get different jitter effects.

The first differential stage of the 10H116 is used as a differential-ramp generator with controlled output impedance and symmetrical rise and fall times. The series Resistor and Capacitor to ground are adjusted to provide a relatively long voltage transition ramp that can be used to manipulate the edge transition timing. The ECL output termination resistors

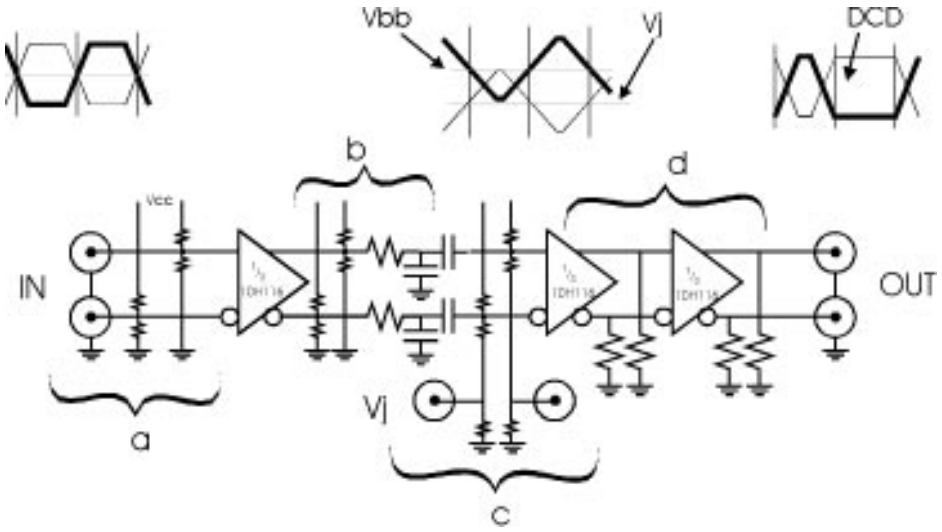

Figure 49. Duty Cycle Distortion Jitter Generator Schematic

shown at the outputs of each differential stage are part of the normal PECL output loads, and can be either the parallel terminations shown at (a) or the single pull-down shown at (d).

The R−C ramp generator at must be tuned to each data rate, to insure that 100% voltage swing is maintained for the narrowest pulses expected. If the Ramp is too long, it will be possible to raise Vj above the level of some data bits, thus "losing" data.

The second differential stage of the 10H116 serves as a voltage comparator that translates the differential, artificially extended voltage-ramps back to PECL swings. The differential (or single-ended) control voltage (Vj) level modifies the restored DC levels of the AC coupled ramps. By adjusting the DC levels at the input of stage two, the average (DC voltage component) of each ramp can be independently adjusted. This adjustment moves the "crossing voltage" which the differential inputs of stage two converts to changes in the timing of the data bit. Additional DC filtering may be required between the Vj input and its input to (d) to insure that high-frequency, single-ended noise does not corrupt the data flow.

The third differential stage of the 10H116 is used to restore crisp-edged, full-swing levels to the serial data, and to drive the subsequent transmission line. In some cases, the PECL output terminations of this stage are provided by the transmission line terminations.

Synthetic-DDJ Jitter Generator

Data Dependent Jitter (DDJ) that approximates the natural effect of long wire-transmission lines, can be generated by the circuit shown in *Figure 50*. This circuit uses the stages in a 10H116 (ECL triple-differential amplifier) to perform

- Differential-PECL-input buffering
- Ramp generation
- Threshold shifting
- Level restoration
- Differential PECL output buffering

In this circuit the Transmitter data stream is fed through the Jitter Generator while the Receiver monitors and checks for correct operation. As the control voltage (Vj) input is varied to cause variations in the "data-corruption" ramps, the data stream is corrupted in a repeatable and measurable manner.

The first differential stage of the 10H116 is used as a differential-ramp generator with controlled output impedance and symmetrical rise and fall times. The series Resistor and Voltage-variable Capacitor (c) are adjusted to provide a relatively long voltage

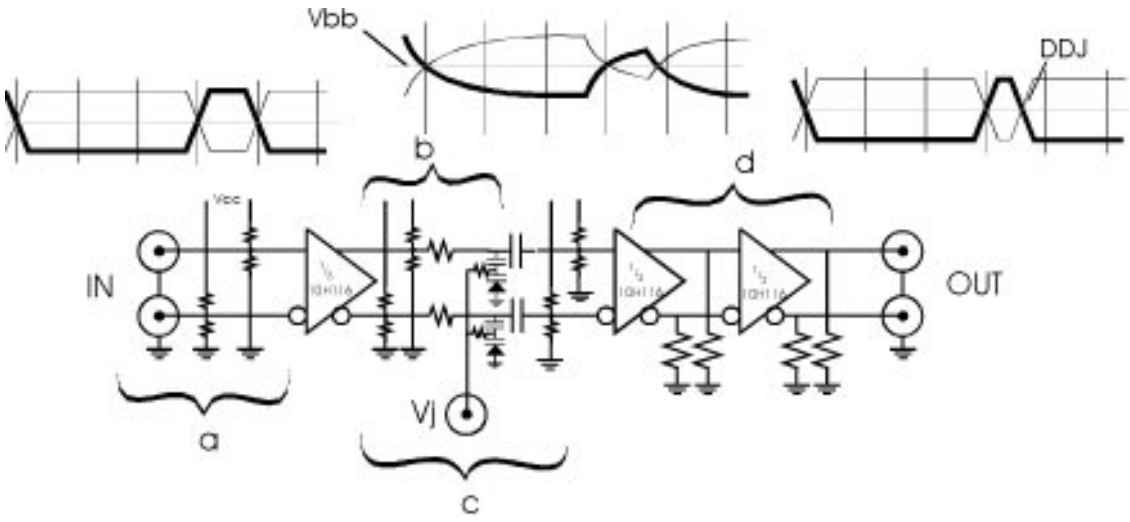

Figure 50. Data Dependent Jitter Generator Schematic

transition ramp that can be used to manipulate the edge transition timing. The ECL output termination resistors shown at the outputs of each differential stage are part of the normal PECL output loads, and can be either the parallel terminations shown at (a) or the single pull-down shown at (d).

The R−C ramp generator at (c) must be tuned to each data rate, to insure that the ramp covers the same number of bits for each speed. If the Ramp is too short, the full spread of pulsewidth dependent jitter will not be generated.

The second differential stage of the 10H116 serves as a voltage comparator that translates the differential, artificially extended voltage-ramps back to PECL swings. The differential restoration resistors put the degenerated waveforms at the optimal voltage so that the inputs of the receiver gate can make a proper logical translation.

The third differential stage of the 10H116 is used to restore crisp-edged, full-swing levels to the serial data, and to drive the subsequent transmission line. In some cases, the PECL output terminations of this stage are provided by the transmission line terminations.

Fiber-Optic Test Bed

The set-up that was used for testing fiber-optic interface capabilities of HOTLink is shown in *Figure 51*. It consists of a HOTLink Evaluation card, several lengths of fiber-optic cable, and appropriate measurement equipment.

A 3-km piece of fiber-optic cable, with only a single splice in it, was used to generate chromatic dispersion. The shorter pieces of fiber, with two connectors between every 500 meters, and the optical attenuator were used to add connector attenuation. The optical splitter and power meter were used to insure repeatability of the measurements. The limits of distance and speed were mostly set by the optical interfaces used, and by the number of connectors in the link.

Coax Test Bed

The set-up used to test wire links is shown in *Figure 52*. It consists of a HOTLink Evaluation Board with suitable connectors and a length of the cable to be used for testing. Various cable types have been tested for speed and distance characteristics. The HOTLink BIST function and the Evaluation Board error indicator combine to offer a clear and unambiguous system to determine the quality of an inter-

connect link, and its suitability to perform at a specified rate.

HOTLink Evaluation Board CY9266−C, CY9266−T, and CY9266−F

The HOTLink Evaluation Card was designed to facilitate early HOTLink system evaluation without expensive or hard to find test equipment. These cards (shown in *Figure 53*) have convenient interfaces for user data and control signals, using either the 48-pin connector used on the IBM OLC−266 card, or a 60-pin card edge connector.

The CY7B923 and CY7B933 include an exhaustive Built-In Self-Test function that can be used to effectively test link performance. It can also be used as a controlled and predictable data source, and as a grader for received data. The receive comparator assures correct functionality of the HOTLink Transmitter, the internal logic in the HOTLink Receiver, and the interconnect link that joins them. These are the essential components of a Bit-Error-Rate tester, except for the reporting mechanism. To fill this need, the Evaluation Cards include a PLD programmed to be a two-digit accumulator and display driver. The Error Display will show the number of Error Bytes received during the BIST sequence, by counting the HOTLink RVS outputs.

BIST

HOTLink Transmitter and Receiver include a comprehensive link test function, as part of the functionality of the basic chips. When the HOTLink Transmitter $\overline{\text{BISTEN}}$ is enabled, the part creates a continuous 511 byte (2^9-1 bytes) pseudo-random stream of 8B/10B-encoded data patterns which the HOTLink Receiver checks byte-by-byte. The 256 possible data patterns are sent once each, and the 12 Special Characters and the 4 specified error codes are sent sixteen times each (except C0.0 which is sent only 15 times) for a total of another 255 data patterns. For a complete list of codes used in the 8B/10B encoder and the Special Character and Error Codes, see the CY7B923/933 HOTLink Tx/Rx Data Sheet.

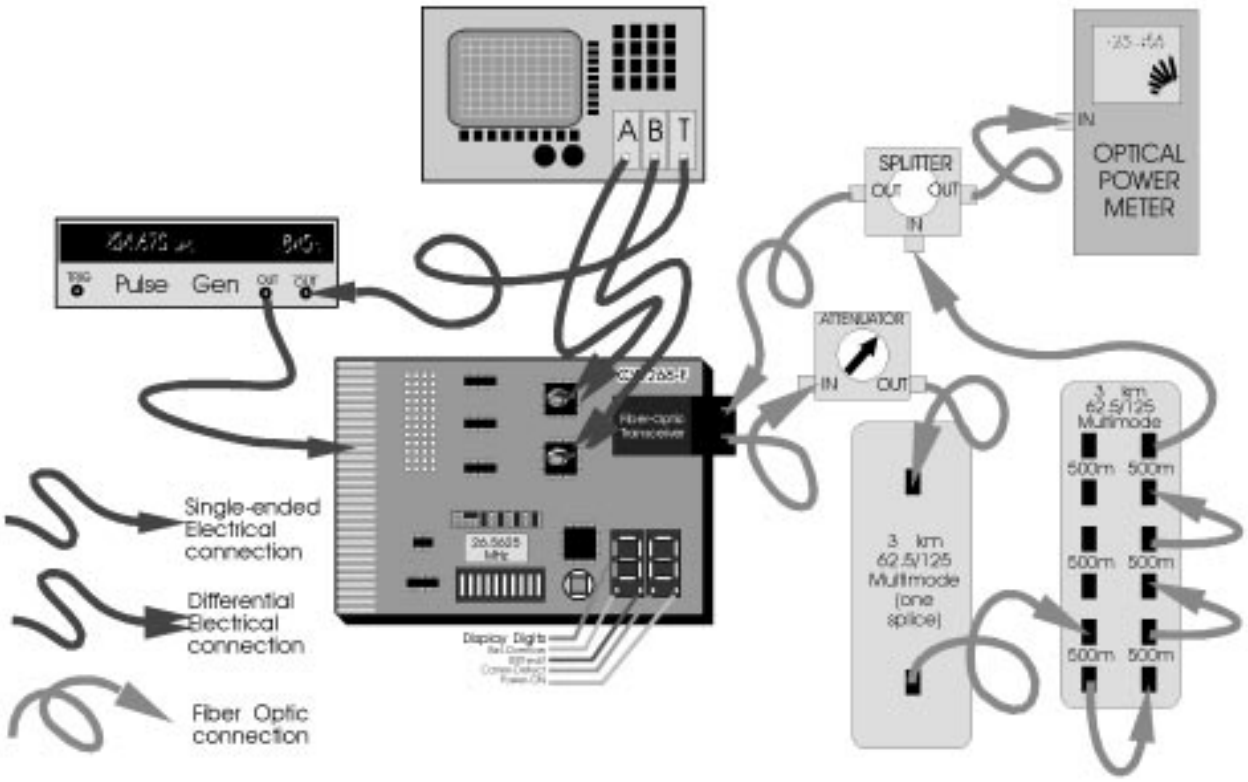

Figure 51. Fiber-Optic Test Bed Facilitates Random-Jitter Testing

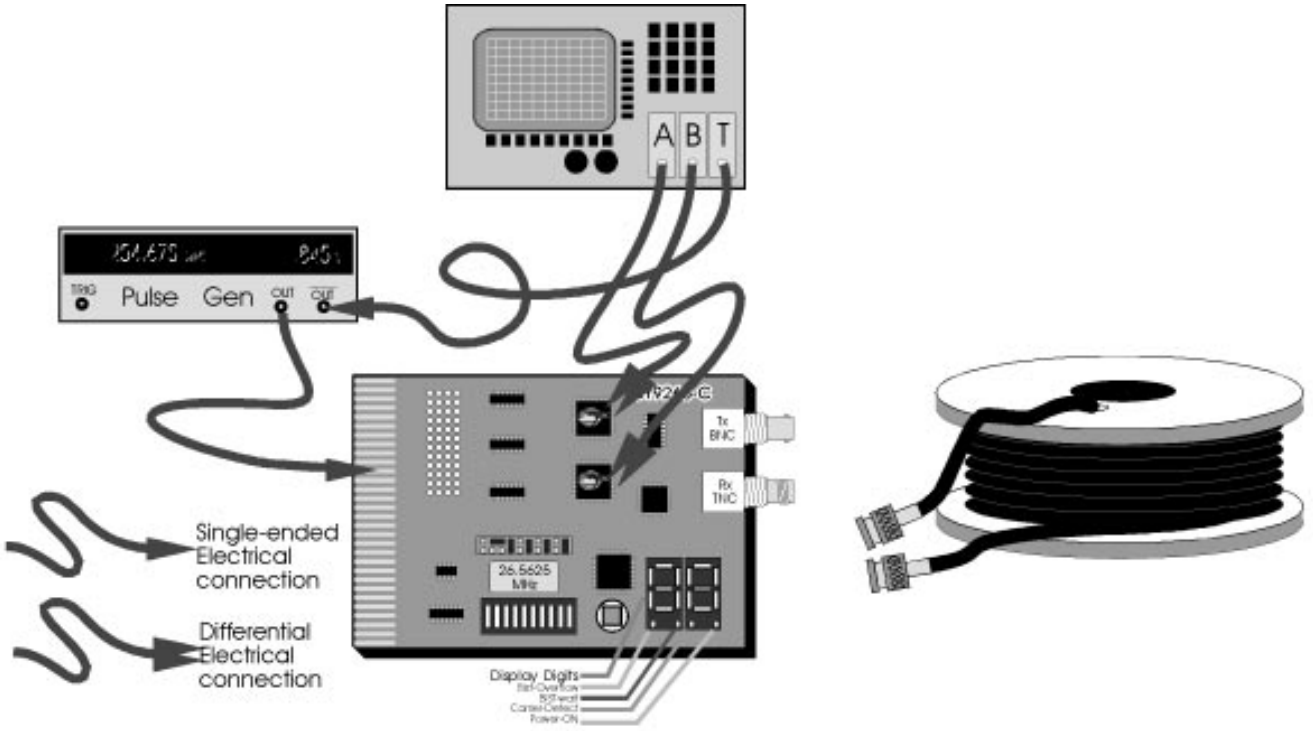

Figure 52. Coax Test Bed to Test for Deterministic Jitter

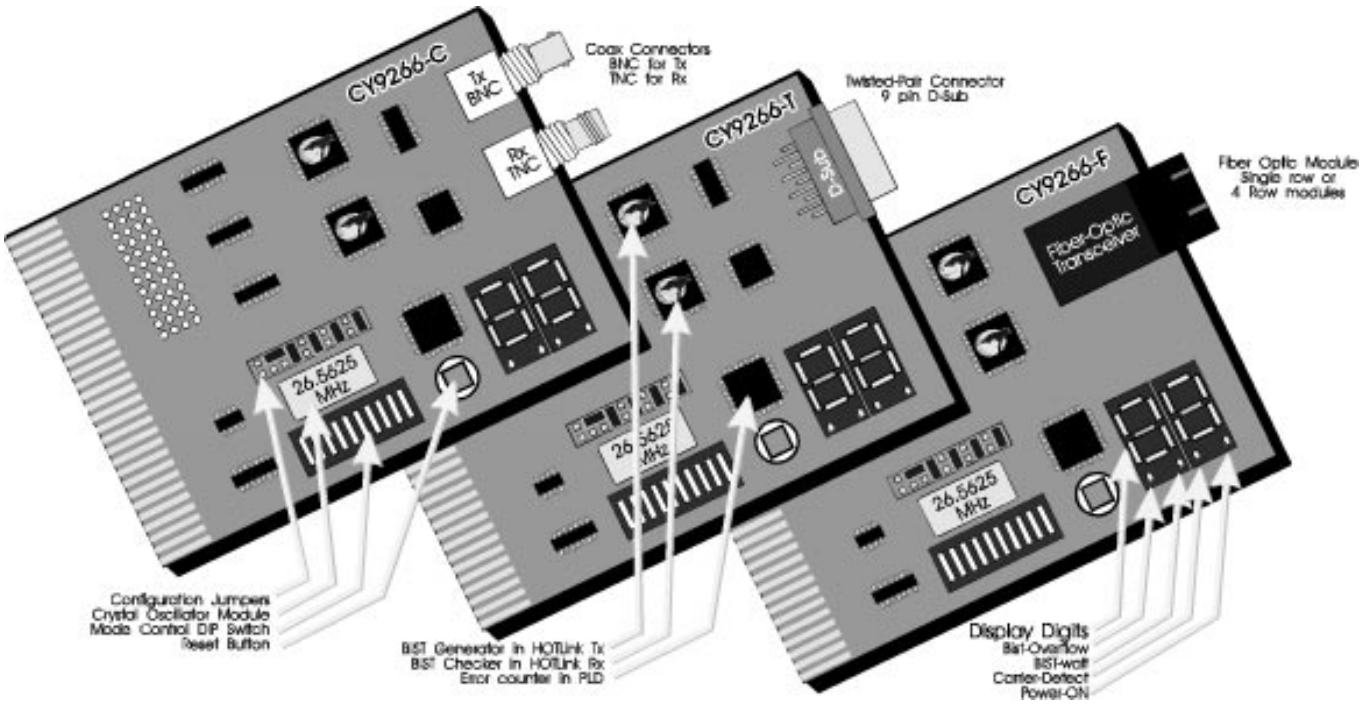

Figure 53. HOTLink Evaluation Boards Form the Core of a Comprehensive Evaluation System

If errors are discovered in the received sequence, received running disparity, or received transmission codes, they are flagged by the RVS output of the HOTLink Receiver. A full discussion of the BIST function of HOTLink is contained in the "HOTLink Built-In Self-Test (BIST)" application note.

For Further Information

HOTLink User's Guide

Hewlett-Packard Catalog
Hewlett-Packard Test & Measurement Division
Mail Station 51LSJ P.O. Box 58199
Santa Clara, CA 95052-9943
(800) 452-4844 or (408) 553-7271

Tektronix Catalog
Tektronix
26600 Southwest Parkway P.O. Box 1000
Wilsonville, OR 97070-1000
(800) 426-2200 or (503) 627-1916

Microwave Logic
285 Mill Rd
Chelmsford, MA 01824
(508) 256-6800

Colby Instruments, Inc.
1810 14th St,
Santa Monica, CA 90404
(310) 450-0261