100BASE-T4 Ethernet Repeater

Background

This application note describes the design of a 100BASE-T4 Ethernet Network Repeater using the Cypress CY7C971 PHY and CY7C388P for the core logic. The repeater has the following features:

- 100-Mb/s Shared Bandwidth over Cat. 3 UTP
- 8 Unmanaged Ports
- Integrated Transmit Filters
- Compact Layout
- Low Latency

The function of the repeater is to create a logically shared communication channel between the end stations in the network. The end stations (computer, printer, etc.) communicate with the repeater over dedicated twisted pair links. The repeater listens to the signal being received on one port and "repeats" the restored signal to the other ports. *Figure 1* illustrates the function of the repeater in a 100BASE-T4 Ethernet Network. The repeater in this application note has eight communication ports.

The functional requirements of the 100BASE-T4 repeater are defined in the IEEE 802.3u Standard "MAC Parameters, Physical Layer, Medium Attachment Units and Repeater for 100 Mb/s Operation," Clause 27. The repeater functional requirements are summarized below:

- Detect port activity and receive Ethernet packets
- Restore the shape, amplitude, and timing of the received signals prior to retransmission

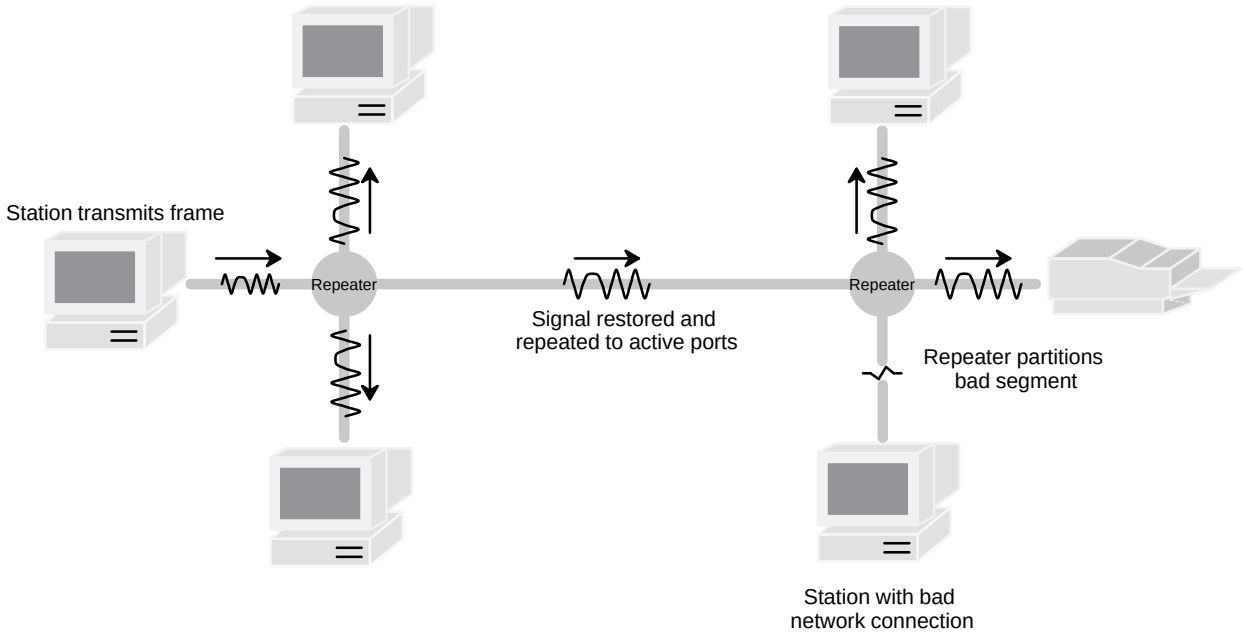

Figure 1. Ethernet Network Built with Repeaters

- Regenerate preamble sequence and prepend it to the received frame
- Forward the Ethernet frame to each of the ports
- Detect collisions between ports and generate jam sequence to all ports
- Protect network from long carrier events (jabber) and repeated collisions (partition)
- Allow installation (removal) of station without network disruption
- Provide basic port control (enable/disable)

Repeater Block Diagram

A block diagram of the 8-port repeater is shown in *Figure 2*. The CY7C971 functions as the physical layer device that interfaces the digital core logic to the twisted-pair medium. Each CY7C971 requires a quad 1:2 transformer for electrical isolation from the medium. The core logic is implemented with a CY7C388A FPGA. This device takes care of the basic repeater functions such as data retiming, sequence generation, and port control.

CY7C971

The CY7C971 (see *Figure 3*) has a special low latency repeater mode that is enabled when the MODE pin is LOW. In this mode, the MII (Media Independent Interface), PCS (Physical Coding Sublayer), and 10BASE-T are disabled. Only the 100BASE-T4 PMA (Physical Medium Attachment) circuits are active. These circuits perform the analog functions required to interface to the twisted-pair media such as transmit filtering, adaptive equalization, and clock recovery. A block diagram of the PMA interface is shown in *Figure 4*.

Media Dependent Interface (MDI)

The CY7C971 provides a simple interface to the 8-pin modular RJ−45 jack. No expensive external filters or components are necessary because all transmit filtering and equalization are performed on-chip. A quad 2:1 transformer for electrical isolation and termination resistors to match the cable impedance are all that is required.

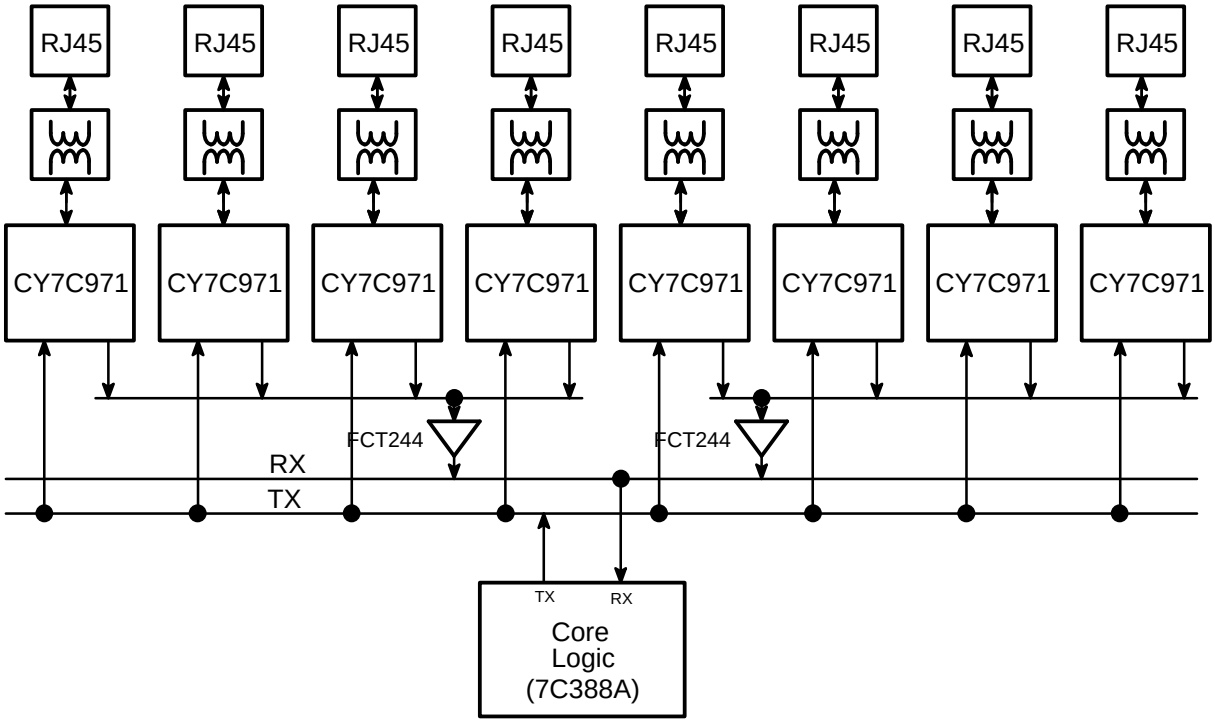

Figure 2. Repeater Block Diagram

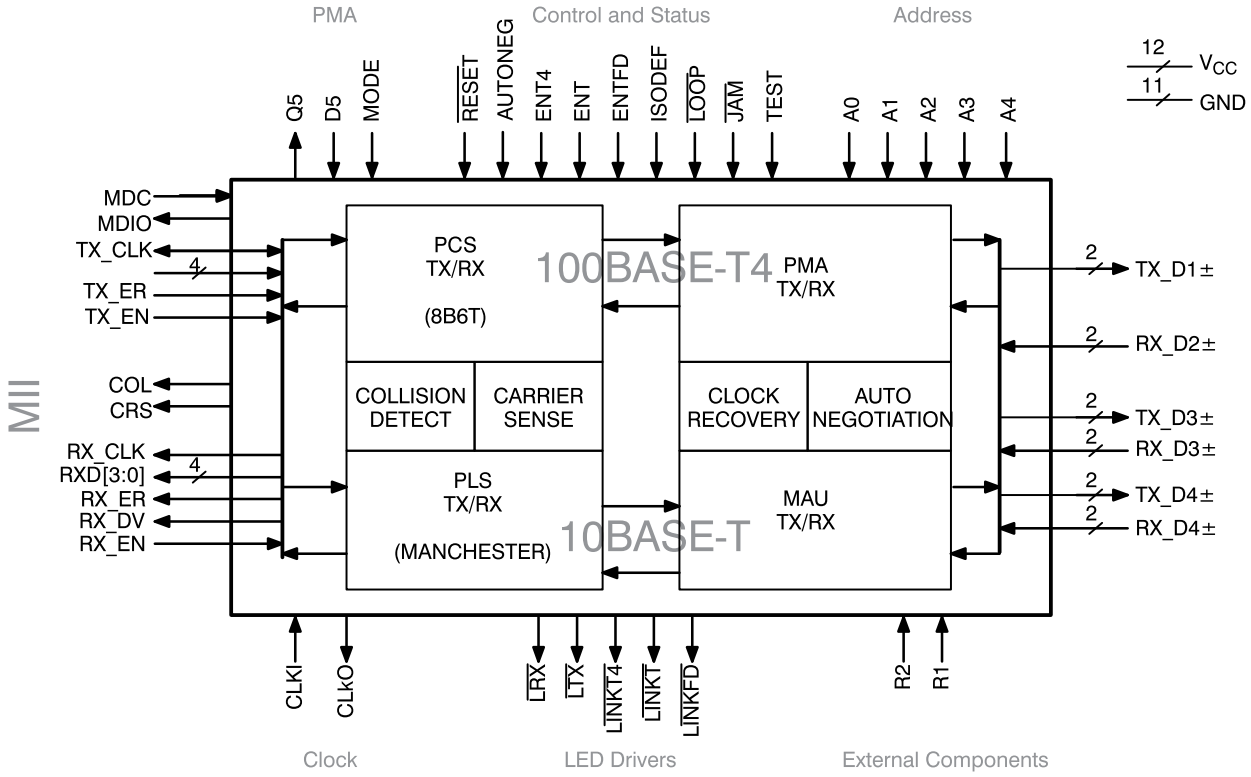

Figure 3. CY7C971 Block Diagram

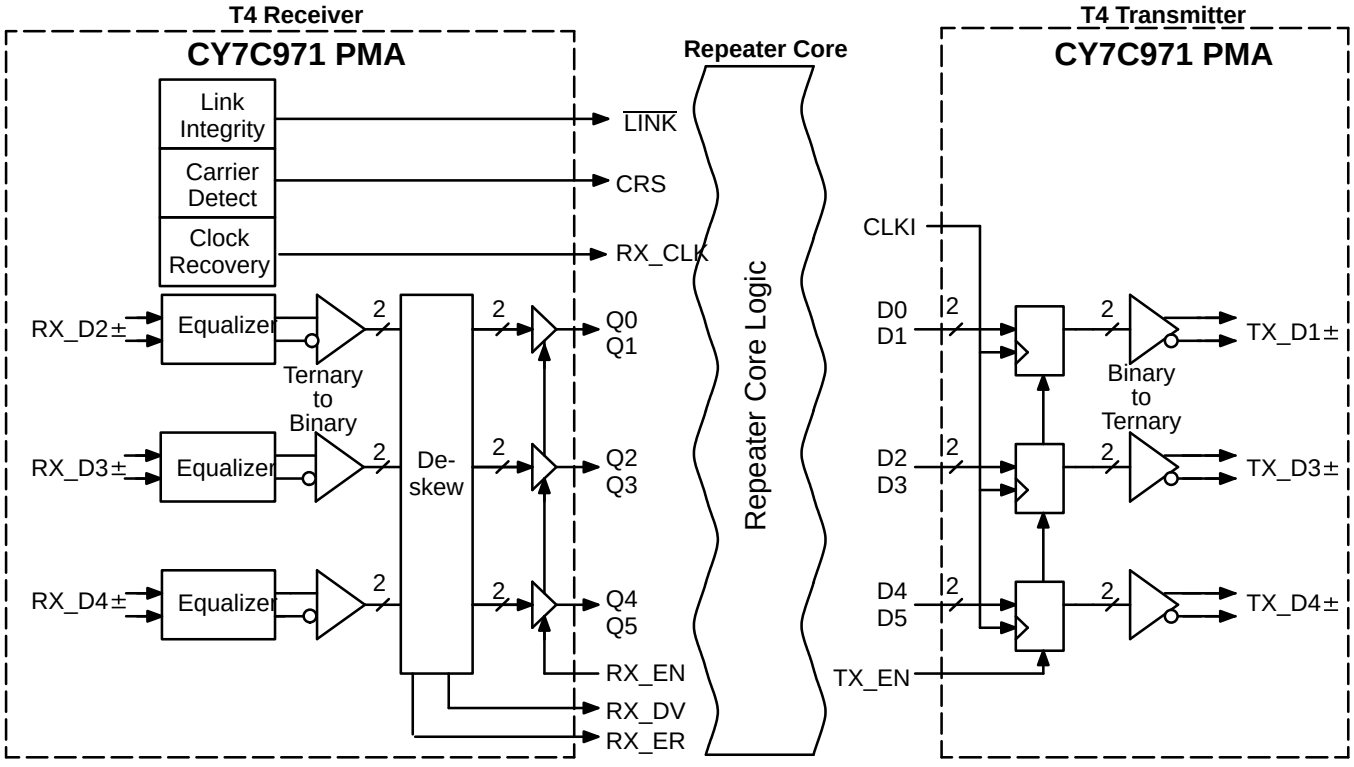

Figure 4. CY7C971 PMA Interface

The output buffer design uses a feedback voltage driver that minimizes power consumption and controls the common-mode output voltage. The transformer provides sufficient common mode rejection over the frequencies of interest so that an external common mode choke is not needed. *Figure 5* shows a schematic of the media interface with the CY7C971.

The characteristic impedance of the twisted pair medium is a nominal 100Ω. The 1:2 transformer reduces (by the square of the turns ratio) medium load impedance to 25Ω on the primary (971) side. The termination resistors and the output buffer impedance together form a matching 25-ohm load. The matching load insures that maximum signal is transferred to the medium and minimizes reflections due to impedance mismatch.

The center taps on the media side of the transformer are connected to the chassis ground through 220-pF (minimum) high-voltage (2 KV) capacitors. These capacitors help absorb common mode noise that is picked up or generated on the twisted pair medium. The capacitors must be capable of withstanding the isolation requirements specified in the 100BASE-T4 standard. High voltage ceramic disc capacitors are economical and work well in this application.

The high precision currents needed for the transmit DAC and equalizer are derived from the external 10KΩ 1% resistor on pins R1 and R2. An internally generated band-gap voltage reference is used by the CY7C971 for all internal reference voltages.

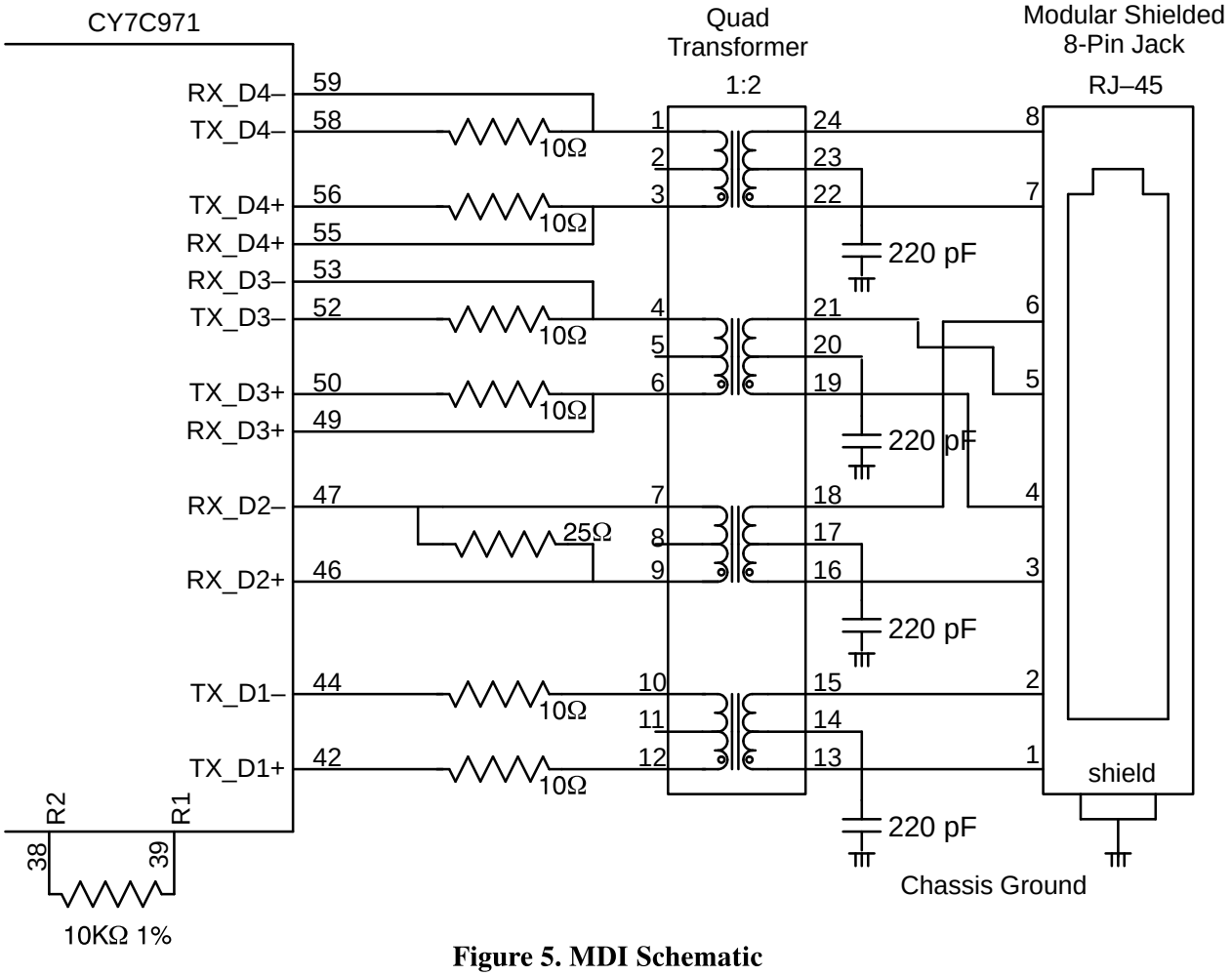

Figure 5. MDI Schematic

LED Pins

Figure 6 shows how the LED pins connect to the LEDs. The $\overline{\text{LINKT4}}$ pin indicates when the CY7C971 is in the link pass state for 100BASE-T4. The CY7C971 will enter a link pass state when properly formed technology dependent link integrity pulses are received from the medium. The $\overline{\text{LINKT}}$ and $\overline{\text{LINKFD}}$ signals remain inactive.

Configuration Pins

The configuration pins are wired for the repeater application as shown in *Figure 7*. The MODE pin is tied LOW to force the CY7C971 into 100BASE-T4 PMA mode. PMA mode disables the MII, PCS (Physical Coding Sublayer), and 10BASE-T. The 100BASE-T4 PMA performs all of the analog functions required to interface to 4 pair Cat. 3 UTP.

The ENT4 pin is wired HIGH to enable 10BASE-T4. The ENT and ENFD pins are wired LOW to disable 10BASE-T and Full Duplex operation. The AUTONEG pin is wired to a header block and pull-up. When a jumper is installed in the header block, Auto-Negotiation is disabled. When the jumper is absent, Auto-Negotiation is enabled.

The ISODEF (Isolate Default) pin is tied LOW in order to force the CY7C971 to power up with the MII ready for normal operation (not isolated). This

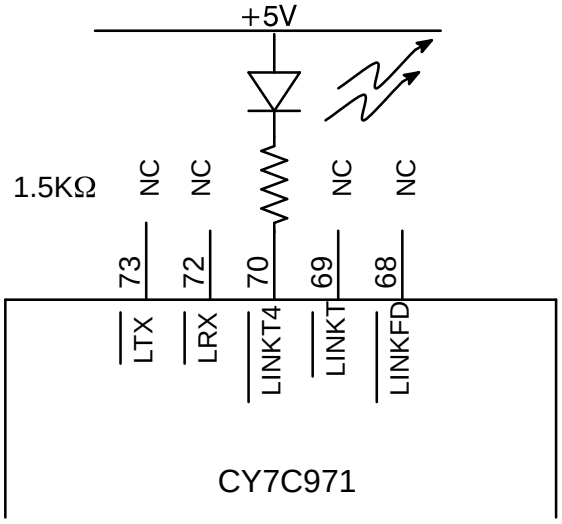

Figure 6. LED Pins

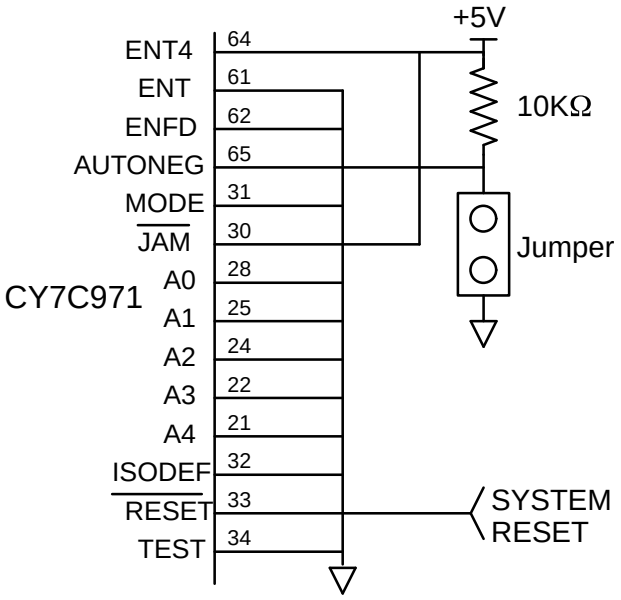

Figure 7. Configuration Pins

repeater application does not use the management port. The address pins can be assigned any address configuration.

The Test pin is tied LOW to permanently disable the 971 test mode. Test mode is used for factory ATE testing only.

The $\overline{\text{RESET}}$ pin should be connected to the system reset pin from the core logic. A system reset is issued at power-up or when the reset button is pushed. If a port is disabled by the core logic, the reset to the port will be active.

Layout Considerations

The repeater design is simple enough to fit on a small 7.75 in x 6.0 board using top-side-only placement. A four-layer PCB construction with dedicated power and ground planes is recommended. The CY7C971 requires a 5V supply. *Figure 8* shows an example of component placement.

The media interface components can be neatly placed in-line with the CY7C971. 0.027 µF decoupling capacitors are used on the CY7C971 power pins. These 0805 SMT capacitors are placed in a row as close to the pins as possible. The termination resistors fit neatly in a row behind the decoupling capacitors. The CY7C971 media interface and power

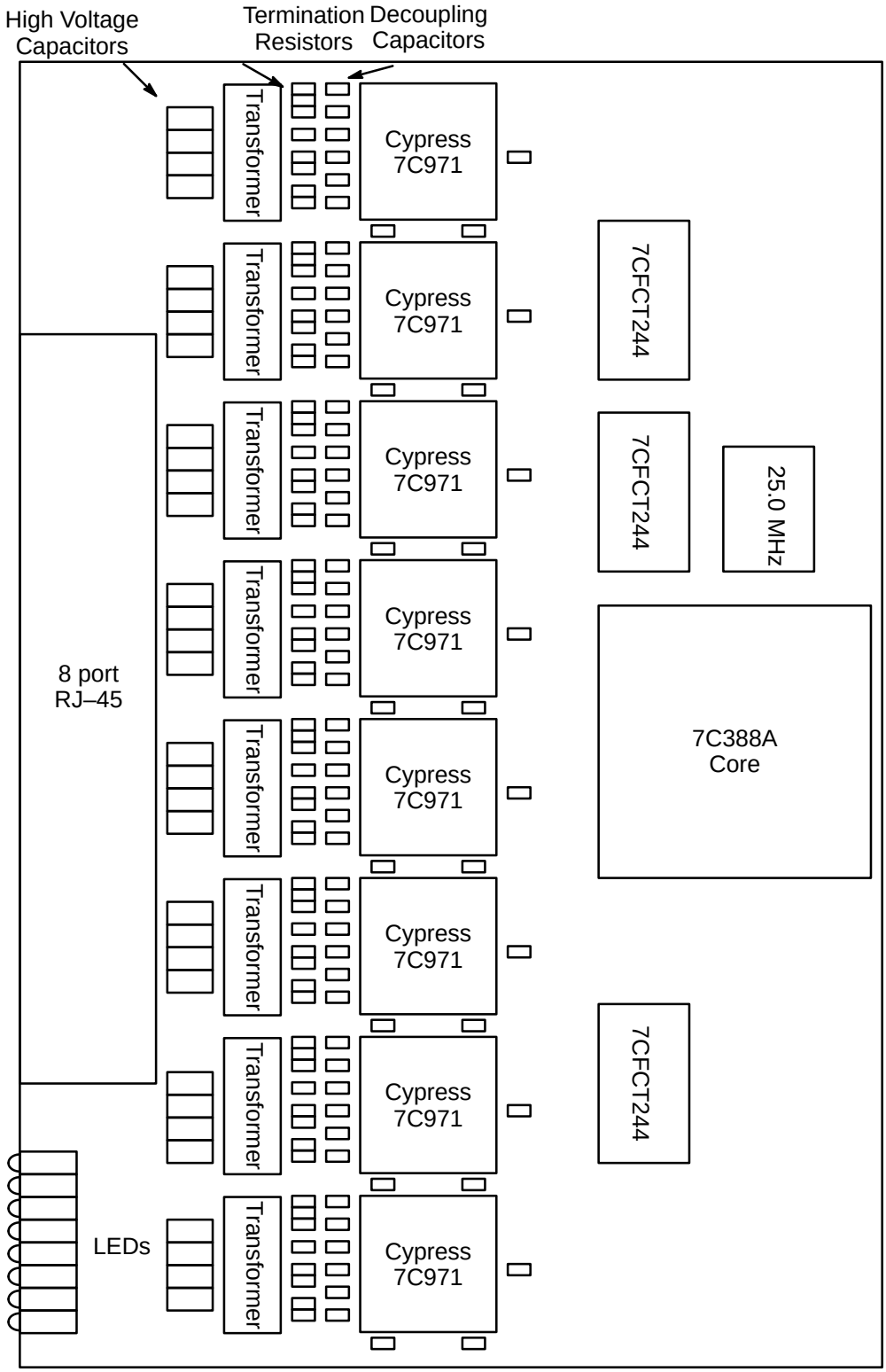

Figure 8. Component Placement

pins are placed in such a way to minimize the use of vias and simplify board layout.

Core Logic

Figure 9 shows a block diagram of the repeater core logic. The blocks perform functions as follows:

- **Port N.** Synchronizes signals and provides control signals to each port, along with detecting jabber and partition conditions.
- **Selection and Clock MUX.** Selects the receive clock from the incoming port and provides a common receive clock for use in retiming the incoming data.
- **RX FIFO.** Used for temporary storage and to retime the incoming data to TX_CLK.
- **Bad Symbol, Jam, Idle, Preamble Generator.** Provides the special characters that are transmitted during different conditions.
- **Output Register.** Provides temporary storage of outgoing data along with retiming to the TX_CLK.
- **Repeater State Machines and Logic.** Controls port selection during data reception. Also, provides collision detection and handling. Included in this block is the control of two expansion ports for use in the design of a stackable repeater.

The core logic is written in Verilog and fills 7K gates of a Cypress CY7C388P 8K pASIC.

Conclusion

This application note covers the major issues for a 8-port 100BASE-T4 Repeater design using the CY7C971 100BASE-T4/10BASE-T Transceiver and CY7C388P 8K FPGA. The high degree of integration in the CY7C971 keeps the number of external components to a minimum, helping to reduce system cost and design effort.

The complete repeater schematics and a bill of materials are available from Cypress Semiconductor. More information on the CY7C971 can be found in the data sheet. For more information on 100BASE-T4, MII, and Auto-Negotiation standards, consult the IEEE 802.3u document: “MAC Parameters, Physical Layer, Medium Attachment Units and Repeater for 100Mb/s Operation.”

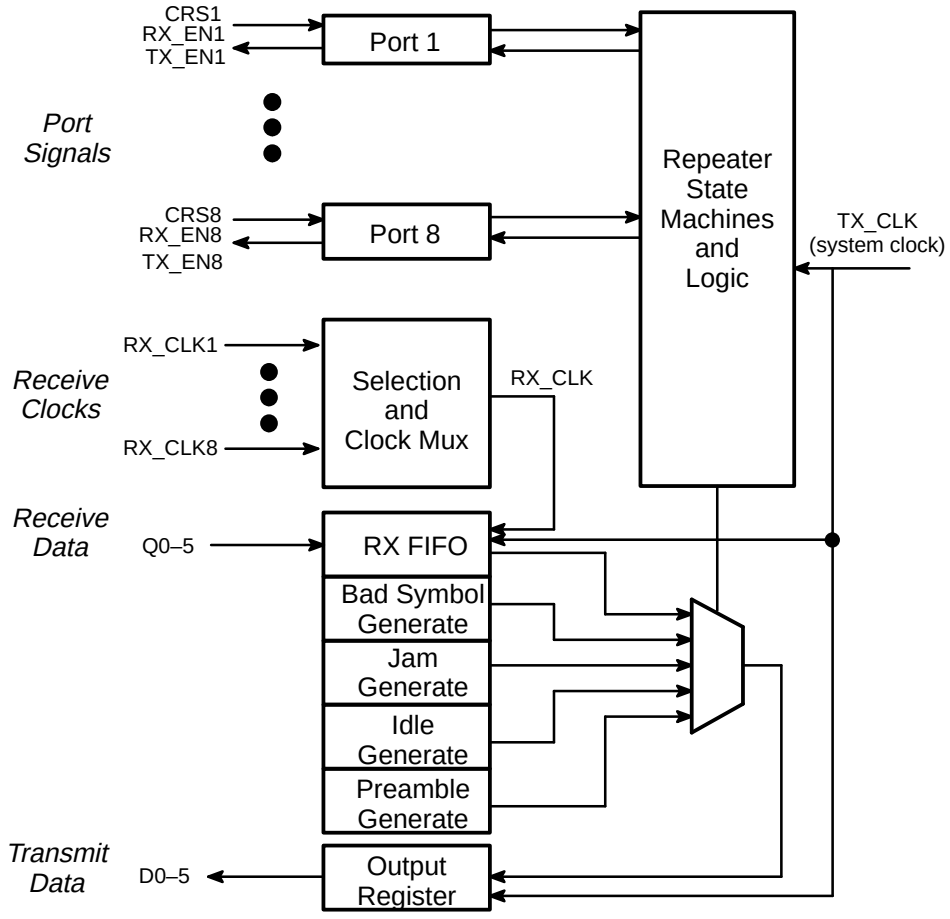

Figure 9. Core Logic