Spice Models for HOTLink

InputBuff Operation Guide

Overview

This memo responds to customer requests for a SPICE model for the HOTLink™ TTL and ECL input buffers. The requested uses of the output model include:

- modelling transmission line effect
- edge rate variations
- simulations at all temperatures between the military extremes (−55°C to 125°C)

This model satisfies those conditions. Package impedance is included in the model, but since it is a single pin model, potential cross talk between different pins is not modeled. This model only models the input impedance of the input structure and only those circuits that affect input impedance are modeled. Specifically, no circuit function is modeled or implied by these models, merely its load to external world.

There are two model files described by this guide, ECL input and TTL input. Both circuit models have the same pad and protection diode, they differ only in bias resistance.

How to Use InputBuff

Pin VPWR should be connected to the system positive supply and be between 4.5 and 5.5 volts with respect to ground. Pin VGND should be connected to system ground.

Pin A is the modeled input pin. The TTLinput buffer is valid for all of the TTL inputs on the CY7B923/933. The ECL input buffer is valid for each pin of the differential ECL input structure used in the CY7B933. Please note that to model an ECL differential pair input, two subcircuit calls to the ECLinput buffer are required.

The temperature specified during simulation is junction temperature. Please not that the junction temperature of the CY7B923/933 is approximately 25°C hotter than the ambient.

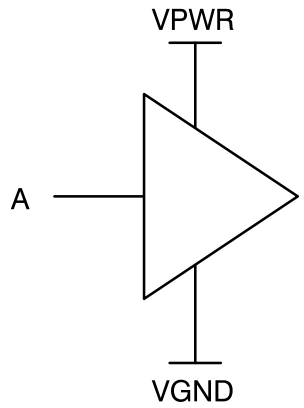

Figure 1. InputBuff Symbol

```
*#############################################################*
*           HOTLink  (7B923/7B933) Input models               *
*             HSPICE MODEL           rev 1.0                  *
*                                                             *
***************************************************************
********>> COPYRIGHT 1994 – CYPRESS SEMICONDUCTOR <<********
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*                                                             *
*        ###  THIS HEADER MUST NOT BE DETACHED  ###           *
*        ###      FROM THE FOLLOWING MODEL      ###           *
*        ###             IN ANY FORM            ###           *
*                                                             *
* This Simulation Model is intended for analytical example    *
*  purposes only and should not be construed as a device      *
*                    specification                            *
*                                                             *
*  Some variation between model simulations and actual        *
*  silicon should be expected due to model simplification     *
*  and normal process variations                              *
*                                                             *
* The ”Ckt Definition Section” may be removed from this       *
* data file and a separate call of either ”ttlinput” or       *
* ”eclinput” may be placed into a larger simulation circuit   *
*  – input signal ”A” should be connected to the trace        *
*   -------------- SIMULATION RESTRICTIONS --------------     *
* –– This model correlates to bench information at three      *
* temperatures –60, 25, and 125 degrees C at 5.0V VCC for     *
* nominal silicon.  However these parameters may be           *
* adjusted over the following ranges with acceptable          *
* results:                                                    *
*               –55’C < TEMP < 155’C                          *
* (where ”TEMP” is the device junction Temperature)           *
*                4.5V < VCC < 5.5V                            *
*   ------------------------------------------------------    *
*#############################################################*

* ------------------- Begin Ckt Section ------------------ *
***************************************************************
*                   Ckt Definition  Section                   *
***************************************************************

* input model simulation

vcc vcc 0 dc 5
vss vss 0 dc 0
***************************************************************
*                        AC STIMULUS                          *
***************************************************************
vttl ttlin 0 ac
vecl eclin 0 ac

.ac dec 10 300k 1000meg
.plot  PAR(’1/i(vecl)’) PAR(’1/i(vttl)’) $ plot impedance
***************************************************************
```

```
*                        DC STIMULUS                              *
*****************************************************************
*vttl ttlin 0 dc xin
*vecl eclin 0 dc xin
*.dc  xin –1 6 .2
*.print i(vecl) i(vttl)
*.plot  i(vecl) i(vttl)

.options post co=132

* ---------------- Subcircuit Calls ------------------------*
xecl vcc vss eclin eclinput
xttl vcc vss ttlin ttlinput
* ----------------- End Subcircuit calls --------------------*

*****************************************************************
* --------------------- End Ckt Section ------------------- *

* ------------------ Begin SubCkt Section ----------------- *
*****************************************************************
*                  SubCkt Definition  Section                   *
*****************************************************************
* –()–pkg. mod.    VPWR    ---|                                  *
* ----direct con.           |---+---\                           *
*                           |        \                          *
*   The Input       A --()–|         |                          *
*                           |        /                          *
*                           |--+----/                           *
*                   VGND   ---|                                  *
*****************************************************************

.SUBCKT ECLinput vpwr vgnd A

*********************************************************************
*                            Resistor elements                      *
*********************************************************************

ri11          r0_i11      r1_i11      0.2000
ri14          r0_i14      vgnd       8.3000k
ri18          vpwr       r0_i14      10.3000k
ri3           r0_i3       r0_i14      1.0000k
ri31          r0_i31      vgnd       10.0000
ri54          r0_i11      r0_i3       400.0000

*********************************************************************
*                           Capacitor elements                      *
*********************************************************************

ci53          r0_i11      r0_i31      0.3600p
ci6_0         r0_i11      vgnd       55.0000f
ci7_0         A        vgnd       0.1400p

*********************************************************************
*                            Inductor elements                      *
*********************************************************************
```

```
li17         r1_i11     A       5.0000n

*********************************************************************
*                            Diode elements                         *
*********************************************************************

di26_d       vgnd       r0_i11     pdiode     area=800.0000 pj=216.0000
di27         vgnd       r0_i11     nwdiode    area=2.4000k pj=180.0000
di32_d       r0_i11      vpwr      pdiode     area=800.0000 pj=216.0000
di39_d       vgnd       r0_i3      pdiode     area=80.0000 pj=36.0000
di40         vgnd       r0_i3      nwdiode    area=500.0000 pj=90.0000
di44_d       r0_i3       vpwr      pdiode     area=80.0000 pj=36.0000

* End of circuit definition

.ends
.SUBCKT TTLinput vpwr vgnd A

*********************************************************************
*                           Resistor elements                       *
*********************************************************************

ri11         r0_i11     r1_i11     0.2000
ri3          r0_i3      vpwr     39.0000k
ri31         r0_i31     vgnd      10.0000
ri54         r0_i11     r0_i3      400.0000

*********************************************************************
*                          Capacitor elements                       *
*********************************************************************

ci53         r0_i11     r0_i31     0.3600p
ci6_0        r0_i11     vgnd      55.0000f
ci7_0        A       vgnd      0.1400p

*********************************************************************
*                           Inductor elements                       *
*********************************************************************

li17         r1_i11     A       5.0000n

*********************************************************************
*                            Diode elements                         *
*********************************************************************

di26_d       vgnd       r0_i11     pdiode     area=800.0000 pj=216.0000
di27         vgnd       r0_i11     nwdiode    area=2.4000k pj=180.0000
di32_d       r0_i11      vpwr      pdiode     area=800.0000 pj=216.0000
di39_d       vgnd       r0_i3      pdiode     area=80.0000 pj=36.0000
di40         vgnd       r0_i3      nwdiode    area=500.0000 pj=90.0000
di44_d       r0_i3       vpwr      pdiode     area=80.0000 pj=36.0000

* End of circuit definition
```

```
.ends
* ------------------ End SubCkt Section ------------------ *

* -------- Begin Device Models Definition Section -------- *
************************************************************
*                 DEVICE MODELS SECTION                    *
************************************************************

************************************************************
*              Diode Models                                *
************************************************************
* diodes
.PARAM JSP=7.6E-19
+ PFOX=5090      MFOXP=15200            MFOXN=10700
+ PCJ0=3.8E-16   PCJP=3.0E-16
+ NCJ0=4.15E-16  NCJP=4.25E-16
+ NWCJ0=0.6E-16  NWCJP=1.4E-16

.MODEL PDIODE
+ D             LEVEL=1        CJO=PCJ0      M=0.55
+ PB=0.9        CJP=PCJP       EXP=0.21      PHP=0.9
+ N=0.95        JS=JSP         RS=1000       EG=1.1
+ XOI=PFOX      XOM=MFOXP
*
.PARAM JSN=1.1E-17
.MODEL NDIODE
+ D             LEVEL=1        CJO=NCJ0      M=0.65
+ PB=0.8        CJP=NCJP       EXP=0.22      PHP=0.9
+ N=1.12        JS=JSN         RS=1000       EG=1.1
+ XOI=PFOX      XOM=MFOXN
*
.MODEL  NWDIODE      D      LEVEL=1
+ CJO=NWCJ0       M=0.4           PB=0.75
+ CJP=NWCJP       EXP=0.4         PHP=0.75
+ N=1.125         JS=4.1E-17      RS=7E6         EG=1.1

.end
************************************************************
******************END*END*END*END*END*END*******************
```

TTLBuff Operation Guide

Overview

This memo responds to customer requests for a SPICE model for the HOTLink TTL output buffers. The requested uses of the output model include:

- modelling transmission line effects
- variations in output due to terminations
- edge rate variations
- simulations at all temperatures between the military extremes (−55°C to 125°C)

This model satisfies those conditions. Package impedance is included in the model, but since it is a single output model, potential cross talk between different outputs is not modeled. Only those circuits that affect the DC or AC function of RP bar are modeled.

The TTLBuff model contains two parameter statements M1 and M2 that select the output modelled. If M1 is selected (not commented out) TTLBuff models $\overline{RP}$-pin 8 (7B923). $\overline{RDY}$-pin 7 (7B933), and CKR-pin 22 (7B933) and if M2 is selected, TTLBuff models RVS, Q7−Q0, and CDL-pins 10−19 (7B933).

How to Use TTLBuff

Pin VPWR1 and pin VPLUS should connected to the system positive supply and be between 4.5 and 5.5 Volts with respect to ground. Pin VGND and VMINUS should be connected to system ground.

Pin A is an imaginary point inside the HOTLink. Just drive it between V_{SS} and V_{CC} (with respect to VGND) in 1 ns and VOUT will behave correctly.

Pin VOUT is the TTL output pin. The datasheet (4 mA) TTL load is a thevenin 330 Ohm resistor connected to a voltage 1.8 volts above ground. A 2 mA load would use a 660 Ohm resistor. The model will perform accurately with no-load, a 2 mA load, or a 4-mA load and with 0 pF to 60 pF on the output pin to ground.

The temperature specified during simulation is junction temperature. Please note that the junction temperature of the 7B923/7B933 is approximately 25°C hotter than ambient.

Note: Exactly one parameter statement M1 or M2 should be commented out during each simulation.

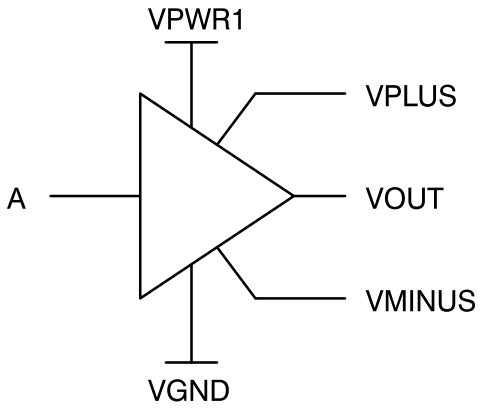

Figure 2. TTLBuff Symbol

```
*#############################################################*
*           HOTLink  (7B923) TTL RP Bar output                *
*             HSPICE MODEL           rev 1.0                  *
*                    –mkm  April 26, 1994                     *
***************************************************************
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*                                                           *
*        ###  THIS HEADER MUST NOT BE DETACHED  ###         *
*        ###      FROM THE FOLLOWING MODEL      ###         *
*        ###             IN ANY FORM            ###         *
*                                                           *
* This Simulation Model is intended for analytical example *
*  purposes only and should not be construed as a device    *
*                    specification                          *
*                                                           *
*  Some variation between model simulations and actual      *
*  silicon should be expected due to model simplification   *
*  and normal process variations                            *
*                                                           *
* The ”Ckt Definition Section” may be removed from this     *
* data file and a separate call of the ”TTLBuff” subckt     *
* may be placed into a larger simulation circuit – input    *
* signal  ”A”       should have characteristics similar     *
* to those given in the ”pulse” statement below.            *
*   ––––––––––––––– SIMULATION RESTRICTIONS ––––––––––––––  *
* –– This model correlates to bench information at three    *
* temperatures –60, 25, and 125 degrees C at 5.0V VCC for   *
* nominal silicon.  However these parameters may be         *
* adjusted over the following ranges with acceptable        *
* results:                                                  *
*               –55’C < TEMP < 155’C                        *
* (where ”TEMP” is the device junction Temperature)         *
*                4.5V < VCC < 5.5V                          *
*   ––––––––––––––––––––––––––––––––––––––––––––––––––––––  *
*#############################################################*

* ––––––––––––––––––– Begin Ckt Section ––––––––––––––––––– *
***************************************************************
*                    Ckt Definition  Section                  *
***************************************************************

* pick any temperature between –55C and 155C
.temp 50

.param vss=0 vccr=5

vpwr1 vpwr1 0  dc  vccr

* input – emulate the pulse stream from the HOTLink Tx
.param rt=1ns
.param per=30ns                   $ data sheet maximum speed
.param pw=’0.4*per–rt’  $ create a 40%–60% RP bar pulse stream
va a 0 pulse (vss vccr 0n rt rt pw per)
```

```
vplus vplus 0 dc vccr
vminus vminus 0 dc vss

vplusm vplusm 0 dc vccr
vminusm vminusm 0 dc vss

.OPTIONS CO=132 POST NOMOD
+ DCSTEP=1 DCCAP=1
+ converge=1

.TRAN 10ps 60ns
*************************************************************
*    MODEL CHOICE M1 or M2                                  *
*    M1: (HOTLink Tx) RP bar, (HOTLink Rx) CKR & RDY Bar    *
*    M2: (HOTLink Rx) Qa–Qj                                 *
*************************************************************
* Choose one of the param statements below
.param                                  $ M1
+pu=750   put1=–0.0022   put2=–1.9e–6  $ M1
+pd=1000  pdt1=–0.0023   pdt2= 7.8e–6  $ M1

*.param                                  $ M2
*+pu=1200  put1=–0.0025   put2=  17e–6  $ M2
*+pd=2400  pdt1=–0.0010   pdt2=–6.4e–6  $ M2

* ———————— subckt reference ———————————————              *
xtop  a vgnd vminus vout vplus vpwr1 TTLBuff
* ———————————————————————————————————————              *

* ———————— may cut here to retain CMOS Load Below ———————— *
*************************************************************
*   TTL LOAD –  DATASHEET SPECIFICATION STANDARD LOAD       *
*************************************************************
cload vout 0 15pf
* standard 4ma TTL Load
rup vout vplus 910
rdn vout 0     510

*************************************************************
* ———————————————— End Ckt Section ———————————————— *

* ———————————————— Begin SubCkt Section ———————————————— *
*************************************************************
*                SubCkt Definition  Section                 *
*************************************************************
* –()–pkg. mod.    VPWR1 ———| |–()– VPLUS                   *
* ————direct con.        |———+–+–\                         *
*                        |         \                       *
*   The Input      A —— |          |——()—— VOUT TTL OUTPUT  *
*   VIH: vcc            |         /                       *
*   VIL: vss            |——+——+–/                         *
*    ~5v/ns         VGND ———|  |–()– VMINUS                *
*************************************************************

.SUBCKT TTLBuff a  VGND VMINUS VOUT VPLUS VPWR1

xsplit rn sn a pm
```

```
*********************************************************************
*                            MOSFET elements                        *
*********************************************************************

mi2910_0     d_i2910    c0_i2999   vgnd       vgnd       nshort
+            l=0.8000   w=6.0000   ad=0       as=0       pd=0
+            ps=0       m=4
mi2914       d_i2914    d_i2918    s_i2914    vgnd       nshort
+            l=1.0000   w=47.6000  ad=0       as=0       pd=0
+            ps=0       m=12        $ ring
mi2914__c    s_i2914    d_i2918    s_i2914    vgnd       nshort
+            l=0.8000   w=1.3000   ad=0       as=0       pd=0
+            ps=0       m=12
mi2918_0     d_i2918    c0_i2996   s_i2918    vpwr1      pshort
+            l=1.0000   w=12.0000  ad=0       as=0       pd=0
+            ps=0       m=4
mi2928_0     d_i2918    c0_i2996   vgnd       vgnd       nshort
+            l=0.8000   w=6.0000   ad=0       as=0       pd=0
+            ps=0       m=4
mi2930       s_i2914    d_i2910    s_i2930    vgnd       nshort
+            l=1.0000   w=47.6000  ad=0       as=0       pd=0
+            ps=0       m=6         $ ring
mi2930__c    s_i2930    d_i2910    s_i2930    vgnd       nshort
+            l=0.8000   w=1.3000   ad=0       as=0       pd=0
+            ps=0       m=6
mi2931_0     d_i2910    c0_i2999   s_i2931    vpwr1      pshort
+            l=1.0000   w=12.0000  ad=0       as=0       pd=0
+            ps=0       m=4
mi3034_0     c0_i2996   rn         vgnd       vgnd       nshort
+            l=0.8000   w=6.0000   ad=0       as=0       pd=0
+            ps=0       m=2
mi3036_0     c0_i2996   rn         vpwr1      vpwr1      pshort
+            l=1.0000   w=6.0000   ad=0       as=0       pd=0
+            ps=0       m=4
mi3038_0     c0_i2999   sn         vgnd       vgnd       nshort
+            l=0.8000   w=6.0000   ad=0       as=0       pd=0
+            ps=0       m=2
mi3040_0     c0_i2999   sn         vpwr1      vpwr1      pshort
+            l=1.0000   w=6.0000   ad=0       as=0       pd=0
+            ps=0       m=4

*********************************************************************
*                            Resistor elements                      *
*********************************************************************

rconv_0      s_i2914    s_i2930    0.1000g     $ conv. res. for fet (/i2930)
rconv_1      d_i2914    s_i2914    0.1000g     $ conv. res. for fet (/i2914)
rconv_2      d_i2918    vgnd       0.1000g     $ conv. res. for fet (/i2928/0)
rconv_3      d_i2910    vgnd       0.1000g     $ conv. res. for fet (/i2910/0)
rconv_4      d_i2910    s_i2931    0.1000g     $ conv. res. for fet (/i2931/0)
rconv_5      d_i2918    s_i2918    0.1000g     $ conv. res. for fet (/i2918/0)
ri3004       vpwr1      s_i2918    pu put1 put2
ri3005       vpwr1      s_i2931    pd pdt1 pdt2
ri3006       r0_i3006   d_i2914    76.0000
ri3012       s_i2914    plus_i3011 0.2000
```

```
ri3016       r0_i3006   r1_i3016   0.2000
ri3025       s_i2930    plus_i3019 0.2000

*********************************************************************
*                          Capacitor elements                       *
*********************************************************************

ci2995       s_i2918    vgnd      64.0000f
ci2996       c0_i2996   vgnd      44.0000f
ci2997       d_i2918    vgnd      0.1870p
ci2998       s_i2931    vgnd      59.0000f
ci2999       c0_i2999   vgnd      43.0000f
ci3000       d_i2914    vgnd      0.2580p
ci3003       d_i2910    vgnd      0.1230p
ci3014_0     r0_i3006   vgnd      55.0000f
ci3015_0     vout       vgnd      0.1400p
ci3017_0     s_i2930    vgnd      55.0000f
ci3022_0     s_i2914    vgnd      55.0000f
ci3023_0     vplus      vgnd      0.1400p
ci3024_0     vminus     vgnd      0.1400p
ci3030       s_i2914    vgnd       0.3600p

*********************************************************************
*                          Inductor elements                        *
*********************************************************************

li3011       plus_i3011 vout       5.0000n
li3019       plus_i3019 vminus     5.0000n
li3021       r1_i3016   vplus      5.0000n

*********************************************************************
*                           Diode elements                          *
*********************************************************************

di2910_0__d  vgnd       d_i2910    ndiode     area=39.6000
+            pj=19.2000
di2914__d    vgnd       d_i2914    ndiode     area=688.8000
+            pj=0
di2918_0__d  d_i2918    vpwr1      pdiode     area=79.2000
+            pj=25.2000
di2918_0__s  s_i2918    vpwr1      pdiode     area=79.2000
+            pj=25.2000
di2928_0__d  vgnd       d_i2918    ndiode     area=39.6000
+            pj=19.2000
di2930__d    vgnd       s_i2914    ndiode     area=1.5640k
+            pj=229.0000
di2930__s    vgnd       s_i2930    ndiode     area=637.0800
+            pj=143.8000
di2931_0__d  d_i2910    vpwr1      pdiode     area=79.2000
+            pj=25.2000
di2931_0__s  s_i2931    vpwr1      pdiode     area=79.2000
+            pj=25.2000
di3026_d     s_i2930    s_i2914    pdiode     area=800.0000
+            pj=216.0000
```

```
di3027       vgnd       s_i2914    nwdiode    area=2.4000k
+            pj=180.0000
di3034_0__d  vgnd       c0_i2996   ndiode     area=22.8000
+            pj=13.6000
di3036_0__d  c0_i2996   vpwr1      pdiode     area=39.6000
+            pj=19.2000
di3038_0__d  vgnd       c0_i2999   ndiode     area=22.8000
+            pj=13.6000
di3040_0__d  c0_i2999   vpwr1      pdiode     area=39.6000
+            pj=19.2000

* End of circuit definition

.ends

.subckt pm rn sn a
ern rn 0 VOL='v(a)'
esn sn 0 VOL='vccr-v(a)'
.ends

* ------------------ End SubCkt Section ------------------ *

* -------- Begin Device Models Definition Section -------- *
*********************************************************
*                DEVICE MODELS SECTION                  *
*********************************************************

*********************************************************
*              Diode Models                             *
*********************************************************
* diodes
.PARAM JSP=7.6E-19
+ PFOX=5090      MFOXP=15200            MFOXN=10700
+ PCJ0=3.8E-16   PCJP=3.0E-16
+ NCJ0=4.15E-16  NCJP=4.25E-16
+ NWCJ0=0.6E-16  NWCJP=1.4E-16

.MODEL PDIODE
+ D             LEVEL=1        CJO=PCJ0      M=0.55
+ PB=0.9        CJP=PCJP       EXP=0.21      PHP=0.9
+ N=0.95        JS=JSP         RS=1000       EG=1.1
+ XOI=PFOX      XOM=MFOXP
*
.PARAM JSN=1.1E-17
.MODEL NDIODE
+ D             LEVEL=1        CJO=NCJ0      M=0.65
+ PB=0.8        CJP=NCJP       EXP=0.22      PHP=0.9
+ N=1.12        JS=JSN         RS=1000       EG=1.1
+ XOI=PFOX      XOM=MFOXN
*
.MODEL  NWDIODE      D      LEVEL=1
+ CJO=NWCJ0       M=0.4           PB=0.75
+ CJP=NWCJP       EXP=0.4         PHP=0.75
+ N=1.125         JS=4.1E-17      RS=7E6         EG=1.1
```

```
************************************************************
*                BiCMOS StarM23 CMOS Model                 *
************************************************************
.PARAM HALFDIF=1.2
.PARAM WICP=0 WICN=0
+ GOX=195
+ VTHP=-0.90      VTHN=0.85
+ PGAMMA=0.40     NGAMMA=0.67
+ LCDP=0.0        LCDN=0.0
+ WCDP=0.0        WCDN=0.0
+ COLP=3.08E-16     COLN=3.42E-16
*
.PARAM
+ WCDRDN=0
+ WCDRDP=0
+ WCDRP1=0.16

.OPTIONS
+ SCALE=1.0E-6 SCALM=1E-6      GMINDC=1.0E-9

*
.MODEL PSHORT
+ PMOS          LEVEL=7         ACM=2          HDIF=HALFDIF
+ LDIF=0.175    RSH=0           RS=5.248K      RD=5.248K
+ CJ=PCJ0       MJ=0.55         PB=0.9         JS=7.6E-19
+ CJSW=PCJP     MJSW=0.21       PHP=0.9        BULK=99
+ LD=0.075      WD=0.0          XL=LCDP        XW=WCDP
+ VTO=VTHP      GAMMA=PGAMMA    LGAMMA=1.0     VBO=0
+ XJ=0.50       VSH=0.45        NWM=0.0        FDS=0.34
+ NWE=0.07      SCM=3.0         TLEV=1         TCV=-1.8E-3
+ WIC=WICP      NFS=4.5E11      MOB=5          UO=265
+ F1=1.8E6      ECRIT=2.0E5     F3=2.0E5       UEXP=0.0
+ NU=0.0        BEX=-1.1        CLM=3          LAMBDA=1.0E-5
+ KL=0          TOX=GOX         CGSO=COLP      CGDO=COLP
+ CGBO=6.2E-16 CAPOP=2         FEX=1.7        IS=0
*
.MODEL NSHORT
+ NMOS          LEVEL=7         ACM=2          LDIF=0.175
+ HDIF=HALFDIF  RS=4.0K         RD=4.0K        CJ=NCJ0
+ MJ=0.65       PB=0.8          JS=1.1E-17     CJSW=NCJP
+ MJSW=0.22     PHP=0.9         BULK=98        LD=0.075
+ WD=0.125      XL=LCDN         XW=WCDN        VTO=VTHN
+ GAMMA=NGAMMA LGAMMA=2.0      VBO=0.0        XJ=0.6
+ VSH=0.65      NWM=0.07        FDS=0.61       NWE=0.04
+ SCM=8.0       TLEV=1          TCV=+1.4E-3    WIC=WICN
+ NFS=2.5E11    MOB=5           UO=553         F1=8.0E6
+ ECRIT=2.52E4 F3=2.52E4       UEXP=0.0       NU=0.0
+ BEX=-1.55     CLM=3           LAMBDA=7.5E-6 KL=0
+ TOX=GOX       CGSO=COLN       CGDO=COLN      CGBO=6.2E-16
+ CAPOP=2       FEX=1.1         IS=0           UPDATE=1
+ PHI=0.85      KCL=0.0
.end
************************************************************
******************END*END*END*END*END*END*****************
```

ECLBuff Operation Guide

Overview

This memo responds to customer requests for a SPICE model for the HOTLink ECL (7B923) output buffer. The requested uses of the output model include:

- modelling transmission line effects
- variations in output due to terminations
- edge rate variations
- simulations at all temperatures between the military extremes (−55°C to 125°C)

This model satisfies those conditions. Package impedance is included in the model, but since it is a single output model, potential cross talk between different outputs is not modeled.

The 7B923 (HOTLink Transmitter) and the 7B951 (SST) share the same ECL output circuitry, so this memo describes the ECL output buffer used in the 7B951 also.

How to Use ECLBuff

Pin VPWR (pin 22-V_{CCQ}) and pin VPLUS (pin 4-V_{CCN}) should be connected to the system positive supply and be between 4.5 and 5.5 Volts with respect to ground. Pin VGND (pin 20-GND) should be connected to system ground.

Pin A is an imaginary point inside the 7B923. Just drive it between 0 and 1 Volt (with respect to VGND) in 400 ps and the ECL outputs will behave correctly.

Pins VOUTX (pin A+, B+, or C+) and VOUT (pin A−, B−, or C−) are the ECL output pins. Unless the pin under test is loaded it will just float up near the voltage of VPLUS. The datasheet ECL load is a 50 Ohm resistor connected to a voltage 2 volts below the voltage of VPLUS. A resistor directly to ground may be used if sized appropriately.

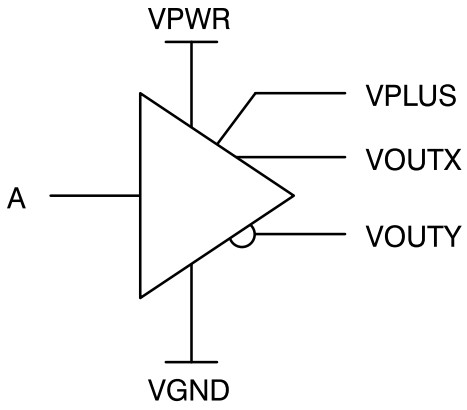

Figure 3. ECLBuff Symbol

```
*#############################################################*
*            HOTLink  (7B923  ECL  O/P Buffer Pair            *
*              HSPICE BIPOLAR MODEL   rev 1.0                 *
*                      –mkm  April 21, 1994                   *
***************************************************************
********>> COPYRIGHT 1994 – CYPRESS SEMICONDUCTOR <<********
*       >>  Do NOT Reproduce without permission   <<         *
*       >>       of CYPRESS SEMICONDUCTOR         <<         *
*                                                             *
*        ###  THIS HEADER MUST NOT BE DETACHED  ###          *
*        ###      FROM THE FOLLOWING MODEL      ###          *
*        ###             IN ANY FORM            ###          *
*                                                             *
* This Simulation Model is intended for analytical example    *
*  purposes only and should not be construed as a device      *
*                     specification                           *
*                                                             *
*  Some variation between model simulations and actual        *
*  silicon should be expected due to model simplification     *
*  and normal process variations                              *
*                                                             *
* The ”Ckt Definition Section” may be removed from this       *
* data file and a separate call of the ”ECLBuff” subckt       *
* may be placed into a larger simulation circuit              *
* input signal ”A” should have characteristics similar        *
* to those given in the ”pulse” statement below.              *
*   ––––––––––––– SIMULATION RESTRICTIONS –––––––––––––       *
* –– This model correlates to bench information at three      *
* temperatures –60, 25, and 125 degrees C at 5.0V VCC for     *
* nominal silicon.  However these parameters may be           *
* adjusted over the following ranges with acceptable          *
* results:                                                    *
*               –55’C < TEMP < 155’C                          *
* (where ”TEMP” is the device junction Temperature)           *
*                4.5V < VCC < 5.5V                            *
*   ––––––––––––––––––––––––––––––––––––––––––––––––––––      *
*#############################################################*

* –––––––––––––––––– Begin Ckt Section ––––––––––––––––––– *
*************************************************************
*                   Ckt Definition  Section                 *
*************************************************************
* eclmodel test simulation
.param vccr=5  $ system VCC voltage value
vvcc vcc 0 dc vccr

.param rt=0.4ns
.param per=6ns $ 6ns corresponds to the fastest HOTLink Data Rate
.param pw='(per–2*rt)/2'

va                      a  0 pulse( 0 1 0ns rt rt pw per )

.options post
.tran 10p 12ns

.print v(a) v(y)
```

```
* ----------- subckt reference --------------                *
xECLBuff a 0 y yn vcc vcc ECLBuff
* ------------------------------------------                *

* -------- may cut here to retain CMOS Load Below -------- *
************************************************************
*  ECL LOAD  –  DATASHEET SPECIFICATION STANDARD LOAD      *
************************************************************
vload vl 0  dc 'vccr–2'
rloady y vl 50
cloady y 0 5pf
rloadyn yn vl 50
cloadyn yn 0 5pf
************************************************************
* -------------------- End Ckt Section ------------------- *

* ----------------- Begin SubCkt Section ----------------- *
************************************************************
*                SubCkt Definition  Section                *
************************************************************
* –()–pkg. mod.    VPWR ----| |–()– VPLUS                   *
* ----direct con.       |---+–+–\                          *
*                       |        \––()–– VOUTX             *
*   The Input      A –– |          |        ECL OUTPUT PAIR *
*   VIH: 1              |        /O–()–– VOUTY             *
*   VIL: 0              |---+---/                          *
*   ~400ps/1v      VGND ----|                              *
************************************************************
.SUBCKT ECLBuff                A VGND VOUTX VOUTY VPLUS VPWR

*********************************************************************
*                     Independent voltage sources                   *
*********************************************************************

vi112_b      b_i112     onthefly_1 dc=0.0
vi112_e      onthefly_2 vis        dc=0.0
vi35_b       iy         onthefly_7 dc=0.0
vi35_e       onthefly_8 e_i35      dc=0.0
ei667        VPWR          b_i112     VOL='2–0.4*v(A)'
ei668        VPWR         ib          VOL='1.6+0.4*v(a)'
*vi673        vpwr       r0_i669    dc=vshift
vi73_b       ix         onthefly_5 dc=0.0
vi73_e       onthefly_6 c0_i52     dc=0.0
vi78_b       ib         onthefly_3 dc=0.0
vi78_e       onthefly_4 vis        dc=0.0

ei673        vpwr       r0_i669    moo 0 1 TC1=24m TC2=–26u
vshift       moo       0           dc 65m

*********************************************************************
*                     Independent current sources                   *
*********************************************************************

iisource     vis        vgnd       dc=3mA
```

```
*********************************************************************
*                            BJT elements                           *
*********************************************************************

qi112        iy         onthefly_1 onthefly_2 cbc2x10
qi35         c_i35      onthefly_7 onthefly_8 ob14x6_r   m=2
qi73         c_i35      onthefly_5 onthefly_6 ob14x6_r   m=2
qi78         ix         onthefly_3 onthefly_4 cbc2x10

*********************************************************************
*                          Resistor elements                        *
*********************************************************************

ri57         e_i35      plus_i51   0.2000
ri58         c0_i52     r1_i58     0.2000
ri637        e_i35      c0_i579    400.0000
ri638        c0_i579    c0_i556    8.0000k
ri643        c0_i639    c0_i556    8.0000k
ri644        c0_i52     c0_i639    400.0000
ri654        r0_i654    vgnd       10.0000
ri658        r0_i658    vgnd       10.0000
ri66         c_i35      plus_i54   0.2000
ri669        r0_i669    iy         307 -830u 5.0u
ri670        r0_i669    ix         307 -830u 5.0u
rrout        vis        vgnd       1meg

*********************************************************************
*                         Capacitor elements                        *
*********************************************************************

ci47_0       e_i35      vgnd      55.0000f
ci52_0       c0_i52     vgnd      55.0000f
ci53_0       vplus      vgnd      0.1400p
ci547        vis        vgnd      98.0000f
ci56_0       vouty      vgnd      0.1400p
ci573        iy         vgnd      0.2330p
ci579        c0_i579    vgnd      52.0000f
ci594        ix         vgnd      0.2330p
ci61_0       c_i35      vgnd      55.0000f
ci62_0       voutx      vgnd      0.1400p
ci639        c0_i639    vgnd      52.0000f
ci642        c0_i556    vgnd      80.0000f
ci663        e_i35      r0_i654    36.0000f
ci664        c0_i52     r0_i658    36.0000f

*********************************************************************
*                          Inductor elements                        *
*********************************************************************

li51         plus_i51   vouty      5.0000n
li54         plus_i54   vplus      5.0000n
li60         r1_i58     voutx      5.0000n

*********************************************************************
*                           Diode elements                          *
*********************************************************************
```

```
di629_d      vgnd       c0_i579    pdiode     area=80.  pj=36.0
di630        vgnd       c0_i579    nwdiode    area=500. pj=90.0
di631        vgnd       vpwr       nwdiode    area=5.8k pj=540.0
di634_d      c0_i579    vpwr       pdiode     area=80.  pj=36.0
di640_d      c0_i639    vpwr       pdiode     area=80.  pj=36.0
di641        vgnd       c0_i639    nwdiode    area=500. pj=90.0
di646_d      vgnd       c0_i639    pdiode     area=80.  pj=36.0
di649_d      vgnd       e_i35      pdiode     area=800  pj=216.0
di650        vgnd       e_i35      nwdiode    area=2.4k pj=180.0
di655_d      e_i35      vpwr       pdiode     area=800  pj=216.0
di657_d      vgnd       c0_i52     pdiode     area=800  pj=216.0
di661        vgnd       c0_i52     nwdiode    area=2.4k pj=180.0
di662_d      c0_i52     vpwr       pdiode     area=800  pj=216.0

* End of circuit definition
.ends
* ------------------ End SubCkt Section ------------------ *

* -------- Begin Device Models Definition Section -------- *
************************************************************
*                 DEVICE MODELS SECTION                    *
************************************************************

************************************************************
*               Diode Models                               *
************************************************************
.PARAM JSP=7.6E-19
+ PCJ0=3.8E-16   PCJP=3.0E-16
+ PFOX=5090      MFOXP=15200
+ NWCJ0=0.6E-16  NWCJP=1.4E-16

.MODEL PDIODE
+ D            LEVEL=1        CJO=PCJ0      M=0.55
+ PB=0.9       CJP=PCJP       EXP=0.21      PHP=0.9
+ N=0.95       JS=JSP         RS=1000       EG=1.1
+ XOI=PFOX     XOM=MFOXP

.MODEL  NWDIODE      D      LEVEL=1
+ CJO=NWCJ0       M=0.4           PB=0.75
+ CJP=NWCJP       EXP=0.4         PHP=0.75
+ N=1.125         JS=4.1E-17      RS=7E6         EG=1.1

*
************************************************************
*                 BiCMOS StarM23 BIPOLAR Models            *
************************************************************
*
.MODEL CBC2X10  NPN   (        TLEV=       2 EG=      1.17 XTI=         3
+BF=     125.00 BR=          12 VAF=     16.5 VAR=         0 RBM=      3.73
+IS=   1.21E-16 NF=        1.02 IKF= 2.09E-02 IKR= 1.44E-03 RB=     129.73
+TF=   15.00P   TR=   2.50N    XTF=       3.5 VTF=       1.5 IRB=  9.19E-05
+CJE=  84.06F   MJE=        0.4 VJE=       0.9 ITF= 2.69E-02 RE=       5.13
+CJS=  121.85F  MJS=        0.4 VJS=      0.75 GAP1=        0 RC=       7.18
+CJC=  78.68F   MJC=       0.22 VJC=       0.8 XCJC=  0.3429 TITF1=-3.0E-03
```

```
+TIRB1=-0.00734 TIRB2=2.22E-05 TBF1=7.00E-03 TBR1=7.00E-03 TLEVC=       0
+TIKF1=-0.00307 TIKF2=1.45E-06 TRC= 4.57E-03 TRB= 6.00E-03 )

.MODEL OB14X6_R NPN   (         TLEV=       2 EG=      1.17 XTI=         3
+BF=     125.00 BR=          12 VAF=     16.5 VAR=         0 RBM=      2.02
+IS=   5.08E-16 NF=        1.02 IKF= 8.77E-02 IKR= 6.05E-03 RB=      32.02
+TF=   15.00P   TR=   2.50N     XTF=       3.5 VTF=       1.5 IRB=  3.86E-04
+CJE=  362.21F  MJE=        0.4 VJE=       0.9 ITF= 1.13E-01 RE=       0.74
+CJS=  464.80F  MJS=        0.4 VJS=      0.75 GAP1=        0 RC=       2.73
+CJC=  413.06F  MJC=       0.22 VJC=       0.8 XCJC=  0.2669 TITF1=-3.0E-03
+TIRB1=-0.00734 TIRB2=2.22E-05 TBF1=7.00E-03 TBR1=7.00E-03 TLEVC=       0
+TIKF1=-0.00307 TIKF2=1.45E-06 TRC= 4.57E-03 TRB= 6.00E-03 )
*
* --------- End Device Models Definition Section --------- *

.end
************************************************************
******************END*END*END*END*END*END*****************
```