



CY7C130/CY7C131 CY7C140/CY7C141

1K x 8 Dual-Port Static RAM

Features

- 0.8-micron CMOS for optimum speed/power
- Automatic power-down
- TTL compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- Master CY7C130/CY7C131 easily expands data bus width to 16 or more bits using SLAVE CY7C140/CY7C141
- \overline{BUSY} output flag on CY7C130/ CY7C131; \overline{BUSY} input on CY7C140/CY7C141
- \overline{INT} flag for port-to-port communication

- Pin compatible and functionally equivalent to IDT7130 and IDT7140

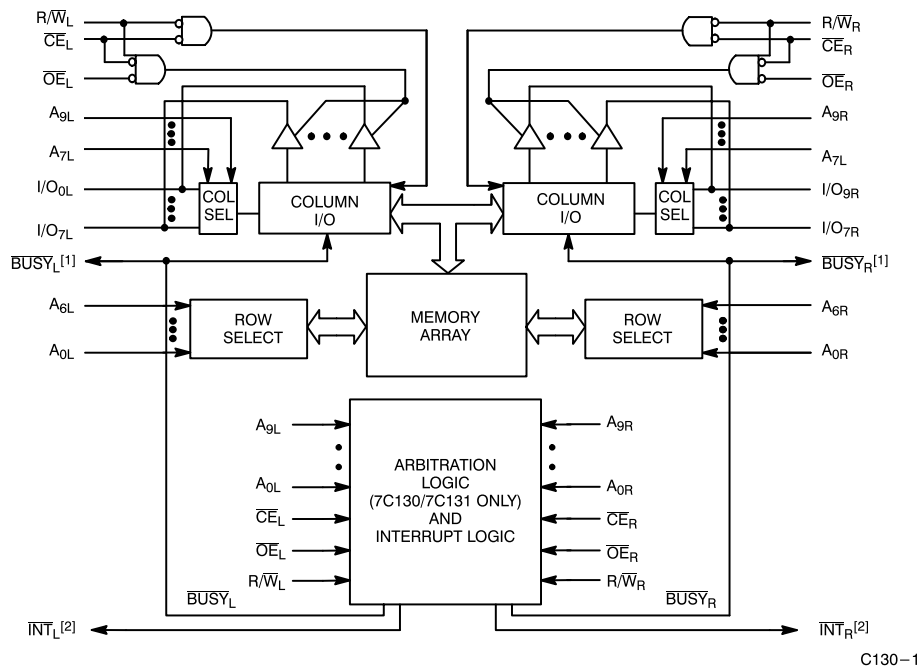
Functional Description

The CY7C130/CY7C131/CY7C140 and CY7C141 are high-speed CMOS 1K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/ CY7C131 can be utilized as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

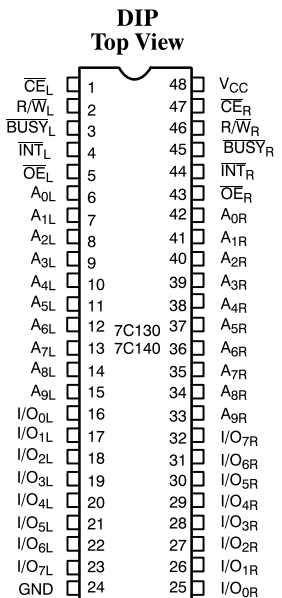
Each port has independent control pins; chip enable (\overline{CE}), write enable ($\overline{R/W}$), and output enable (\overline{OE}). Two flags are provided on each port, \overline{BUSY} and \overline{INT} . \overline{BUSY} signals that the port is trying to access the same location currently being accessed by the other port. \overline{INT} is an interrupt flag indicating that data has been placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power-down feature is controlled independently on each port by the chip enable (\overline{CE}) pins.

The CY7C130 and CY7C140 are available in both 48-pin DIP and 48-pin LCC. The CY7C131 and CY7C141 are available in 52-pin LCC, PLCC, and PQFP.

Logic Block Diagram



Pin Configurations



C130-2

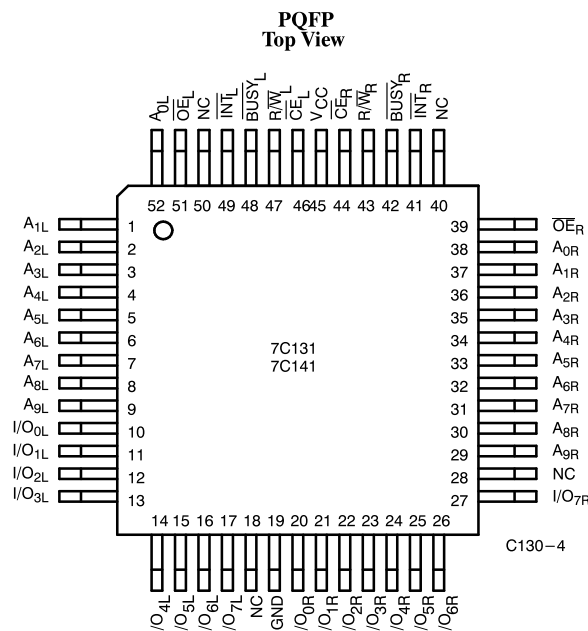
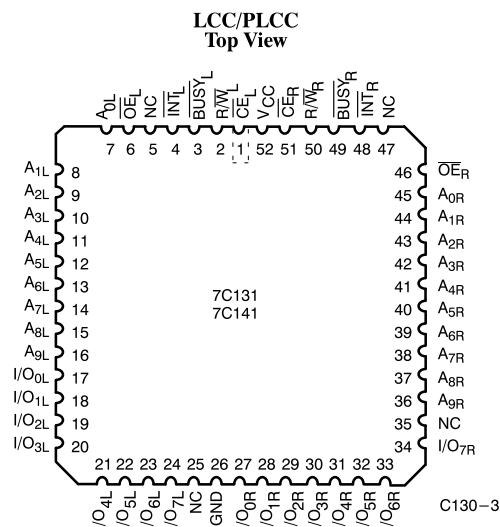
C130-1

Notes:

1. CY7C130/CY7C131 (Master): \overline{BUSY} is open drain output and requires pull-up resistor. CY7C140/CY7C141 (Slave): \overline{BUSY} is input.
2. Open drain outputs: pull-up resistor required.



Pin Configurations (continued)



Selection Guide

		7C130-25 ^[3] 7C131-25 7C140-25 7C141-25	7C130-30 7C131-30 7C140-30 7C141-30	7C130-35 7C131-35 7C140-35 7C141-35	7C130-45 7C131-45 7C140-45 7C141-45	7C130-55 7C131-55 7C140-55 7C141-55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	170	170	120	90	90
	Military			170	120	120
Maximum Standby Current (mA)	Com'l/Ind	65	65	45	35	35
	Military			65	45	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage to Ground Potential

(Pin 48 to Pin 24) -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State -0.5V to +7.0V

DC Input Voltage -3.5V to +7.0V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military ^[4]	-55°C to +125°C	5V ± 10%

Notes:

3. 25-ns version available only in PLCC/PQFP packages.

4. T_A is the “instant on” case temperature



Electrical Characteristics Over the Operating Range^[5]

Parameter	Description	Test Conditions	7C130–25, 30 ^[3] 7C131–25, 30 7C140–25, 30 7C141–25, 30		7C130–35 7C131–35 7C140–35 7C141–35		7C130–45, 55 7C131–45, 55 7C140–45, 55 7C141–45, 55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = –4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 4.0 mA		0.4		0.4		0.4	V
		I _{OL} = 16.0 mA ^[6]		0.5		0.5		0.5	
V _{IH}	Input HIGH Voltage		2.2		2.2		2.2		V
V _{IL}	Input LOW Voltage			0.8		0.8		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	–5	+5	–5	+5	–5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	–5	+5	–5	+5	–5	+5	μA
I _{OS}	Output Short Circuit Current ^[7, 8]	V _{CC} = Max., V _{OUT} = GND		–350		–350		–350	mA
I _{CC}	V _{CC} Operating Supply Current	$\overline{CE} = V_{IL}$, Outputs Open, f = f _{MAX} ^[9]	Com'l	170		120		90	mA
			Mil			170		120	
I _{SB1}	Standby Current Both Ports, TTL Inputs	\overline{CE}_L and $\overline{CE}_R \geq V_{IH}$, f = f _{MAX} ^[9]	Com'l	65		45		35	mA
			Mil			65		45	
I _{SB2}	Standby Current One Port, TTL Inputs	\overline{CE}_L or $\overline{CE}_R \geq V_{IH}$, Active Port Outputs Open, f = f _{MAX} ^[9]	Com'l	115		90		75	mA
			Mil			115		90	
I _{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} – 0.2V or V _{IN} ≤ 0.2V, f = 0	Com'l	15		15		15	mA
			Mil			15		15	
I _{SB4}	Standby Current One Port, CMOS Inputs	One Port \overline{CE}_L or $\overline{CE}_R \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} – 0.2V or V _{IN} ≤ 0.2V, Active Port Outputs Open, f = f _{MAX} ^[9]	Com'l	105		85		70	mA
			Mil			105		85	

Capacitance^[8]

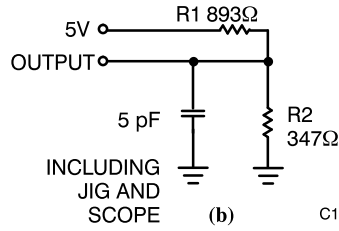
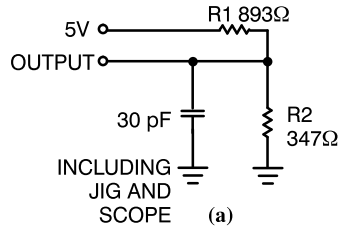
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	15	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

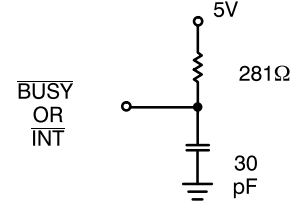
- See the last page of this specification for Group A subgroup testing information.
- \overline{BUSY} and \overline{INT} pins only.
- Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of 1/t_{RC} and using AC Test Waveforms input levels of GND to 3V.
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
- AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
- At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
- t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CS} LOW and R/ \overline{W} LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.



AC Test Loads and Waveforms

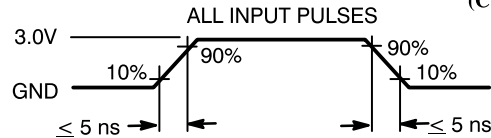


C130-5



BUSY Output Load
(CY7C130/CY7C131 ONLY)

Equivalent to: THÉVENIN EQUIVALENT
OUTPUT — 250Ω — 1.40V



C130-6

Switching Characteristics Over the Operating Range^[5, 10]

Parameter	Description	7C130–25 ^[3]		7C130–30		7C130–35		7C130–45		7C130–55		Unit
		7C131–25	7C131–30	7C131–35	7C131–45	7C131–55						
		7C140–25	7C140–30	7C140–35	7C140–45	7C140–55						
		7C141–25	7C141–30	7C141–35	7C141–45	7C141–55						
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	25		30		35		45		55		ns
t _{AA}	Address to Data Valid ^[11]		25		30		35		45		55	ns
t _{OHA}	Data Hold from Address Change	0		0		0		0		0		ns
t _{ACE}	\overline{CE} LOW to Data Valid ^[11]		25		30		35		45		55	ns
t _{DOE}	\overline{OE} LOW to Data Valid ^[11]		15		20		20		25		25	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[12, 13]	3		3		3		3		3		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[12, 13]		15		15		20		20		25	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[12, 13]	5		5		5		5		5		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[12, 13]		15		15		20		20		25	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		25		25		35		35		35	ns
WRITE CYCLE ^[14]												
t _{WC}	Write Cycle Time	25		30		35		45		55		ns
t _{SCE}	\overline{CE} LOW to Write End	20		25		30		35		40		ns
t _{AW}	Address Set-Up to Write End	20		25		30		35		40		ns
t _{HA}	Address Hold from Write End	2		2		2		2		2		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	R/ \overline{W} Pulse Width	15		25		25		30		30		ns
t _{SD}	Data Set-Up to Write End	15		15		15		20		20		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{HZWE}	R/ \overline{W} LOW to High Z ^[13]		15		15		20		20		25	ns
t _{LZWE}	R/ \overline{W} HIGH to Low Z ^[13]	0		0		0		0		0		ns



Switching Characteristics Over the Operating Range^[5, 10] (continued)

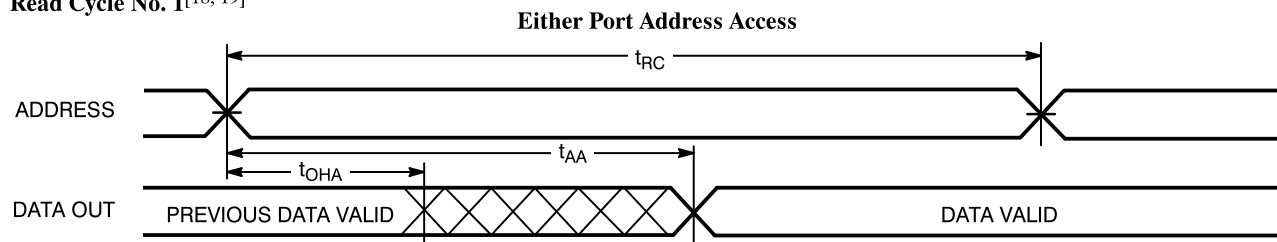
Parameter	Description	7C130–25 ^[3] 7C131–25 7C140–25 7C141–25		7C130–30 7C131–30 7C140–30 7C141–30		7C130–35 7C131–35 7C140–35 7C141–35		7C130–45 7C131–45 7C140–45 7C141–45		7C130–55 7C131–55 7C140–55 7C141–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
		BUSY/INTERRUPT TIMING										
t _{BLA}	$\overline{\text{BUSY}}$ LOW from Address Match		20		20		20		25		30	ns
t _{BHA}	$\overline{\text{BUSY}}$ HIGH from Address Mismatch ^[15]		20		20		20		25		30	ns
t _{BLC}	$\overline{\text{BUSY}}$ LOW from $\overline{\text{CE}}$ LOW		20		20		20		25		30	ns
t _{BHC}	$\overline{\text{BUSY}}$ HIGH from $\overline{\text{CE}}$ HIGH ^[15]		20		20		20		25		30	ns
t _{PS}	Port Set Up for Priority	5		5		5		5		5		ns
t _{WB} ^[16]	R/ $\overline{\text{W}}$ LOW after $\overline{\text{BUSY}}$ LOW	0		0		0		0		0		ns
t _{WH}	R/ $\overline{\text{W}}$ HIGH after $\overline{\text{BUSY}}$ HIGH	20		30		30		35		35		ns
t _{BDD}	$\overline{\text{BUSY}}$ HIGH to Valid Data		25		30		35		45		45	ns
t _{DDD}	Write Data Valid to Read Data Valid		Note 17		Note 17		Note 17		Note 17		Note 17	ns
t _{WDD}	Write Pulse to Data Delay		Note 17		Note 17		Note 17		Note 17		Note 17	ns
INTERRUPT TIMING												
t _{WINS}	R/ $\overline{\text{W}}$ to $\overline{\text{INTERRUPT}}$ Set Time		25		25		25		35		45	ns
t _{EINS}	$\overline{\text{CE}}$ to $\overline{\text{INTERRUPT}}$ Set Time		25		25		25		35		45	ns
t _{INS}	Address to $\overline{\text{INTERRUPT}}$ Set Time		25		25		25		35		45	ns
t _{OINR}	$\overline{\text{OE}}$ to $\overline{\text{INTERRUPT}}$ Reset Time ^[15]		25		25		25		35		45	ns
t _{EINR}	$\overline{\text{CE}}$ to $\overline{\text{INTERRUPT}}$ Reset Time ^[15]		25		25		25		35		45	ns
t _{INR}	Address to $\overline{\text{INTERRUPT}}$ Reset Time ^[15]		25		25		25		35		45	ns

Notes:

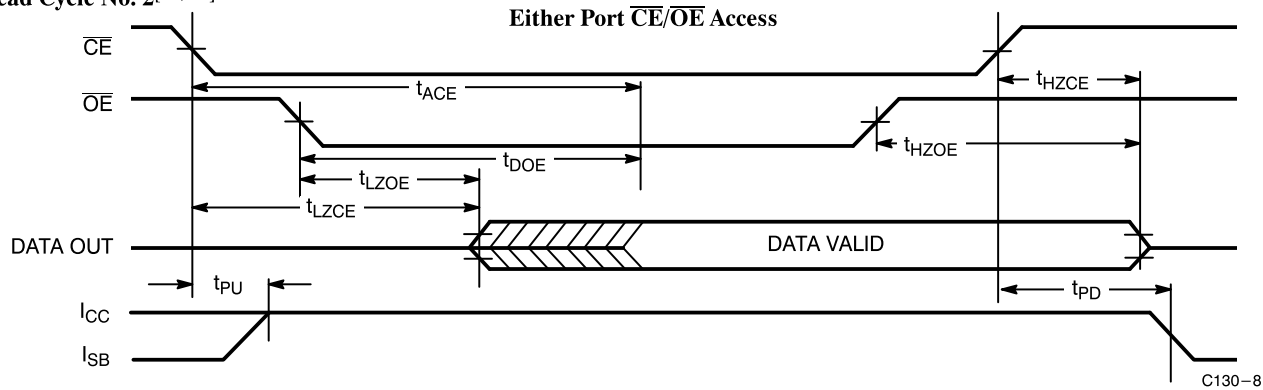
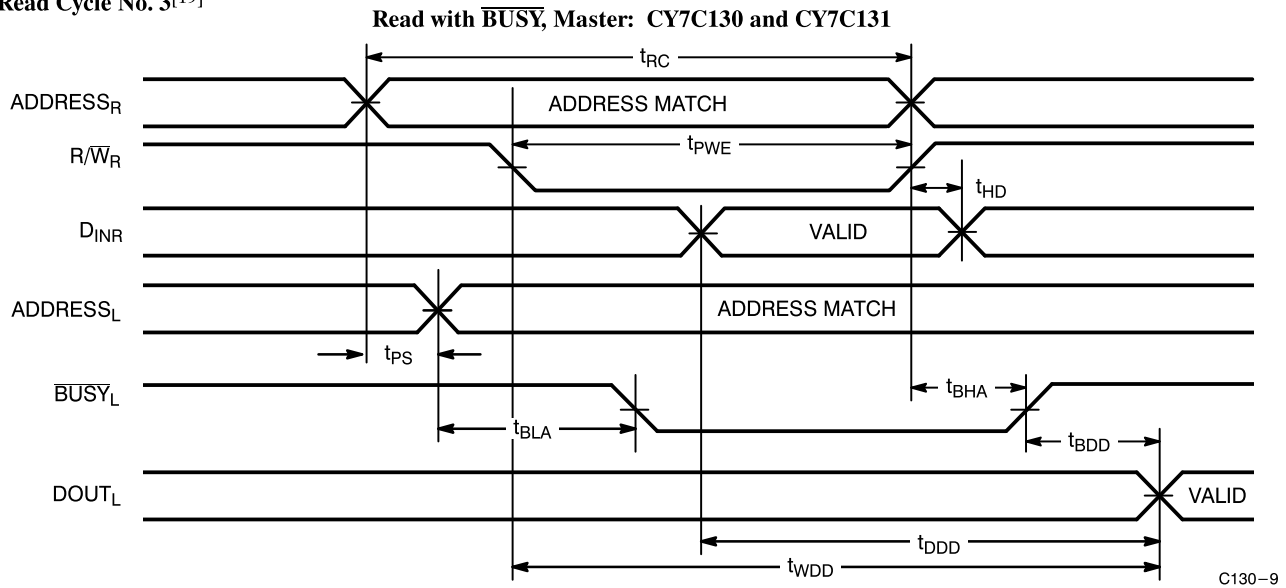
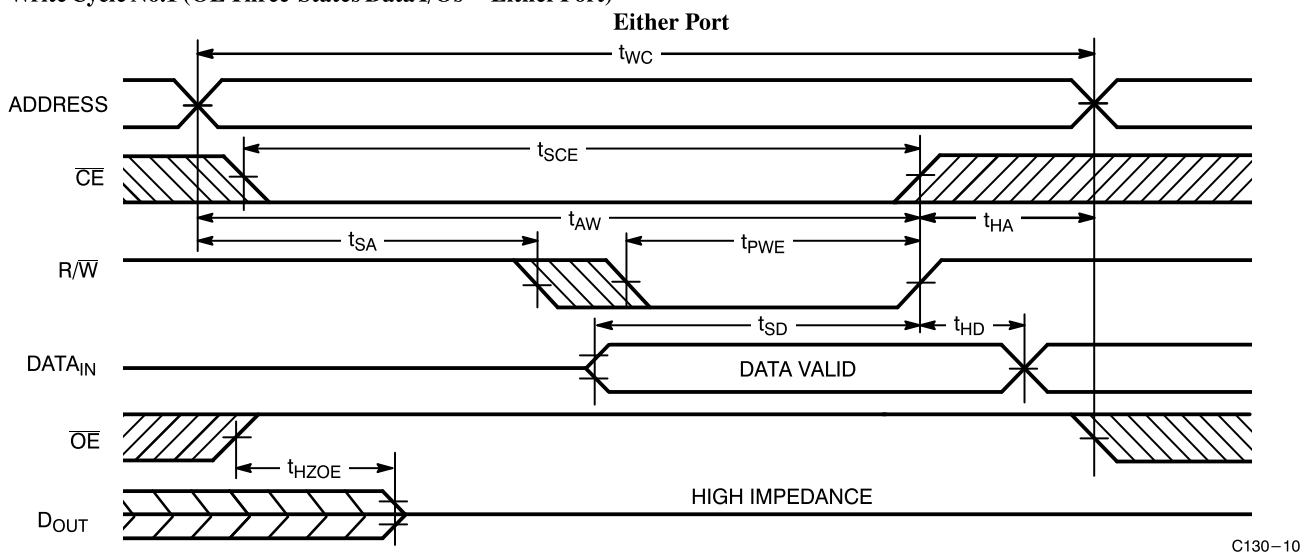
15. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
16. CY7C140/CY7C141 only.
17. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
 - A. BUSY on Port B goes HIGH.
 - B. Port B's address is toggled.
 - C. \overline{CE} for Port B is toggled.
 - D. R/ \overline{W} for Port B is toggled during valid read.
18. R/ \overline{W} is HIGH for read cycle.
19. Device is continuously selected, $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$.
20. Address valid prior to or coincident with \overline{CE} transition LOW.
21. If \overline{OE} is LOW during a R/ \overline{W} controlled write cycle, the write pulse width must be the larger of t_{PWE} or t_{HZWE} + t_{SD} to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.
22. If the \overline{CE} LOW transition occurs simultaneously with or after the R/ \overline{W} LOW transition, the outputs remain in the high-impedance state.

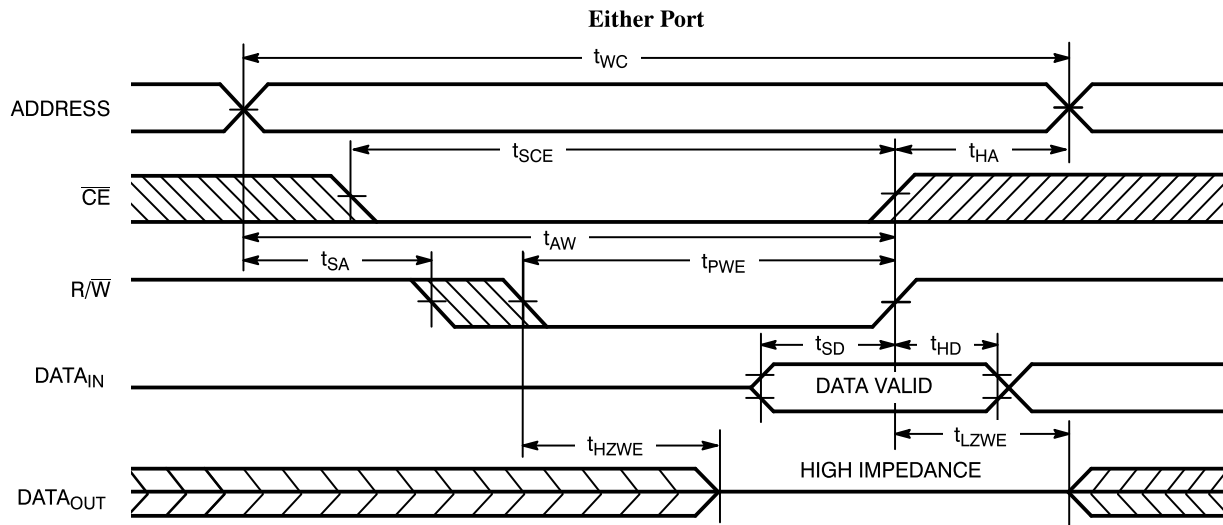
Switching Waveforms

Read Cycle No. 1^[18, 19]

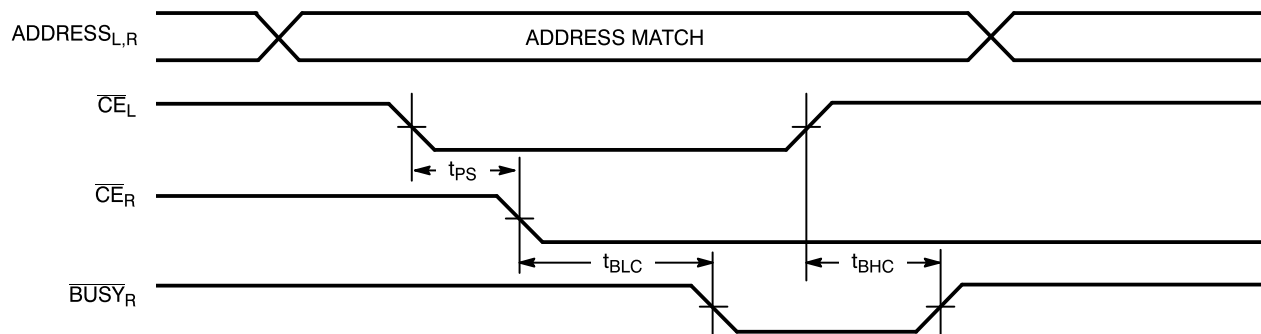


C130–7

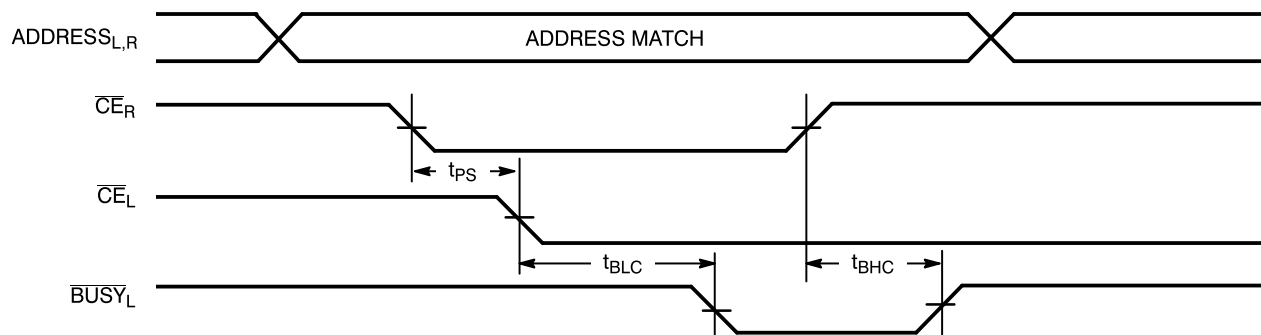
Switching Waveforms (continued)
Read Cycle No. 2^[18, 20]

Read Cycle No. 3^[19]

Write Cycle No.1 (\overline{OE} Three-States Data I/Os – Either Port)^[14, 21]


Switching Waveforms (continued)
Write Cycle No. 2 (R/ \overline{W} Three-States Data I/Os – Either Port)^[15, 22]


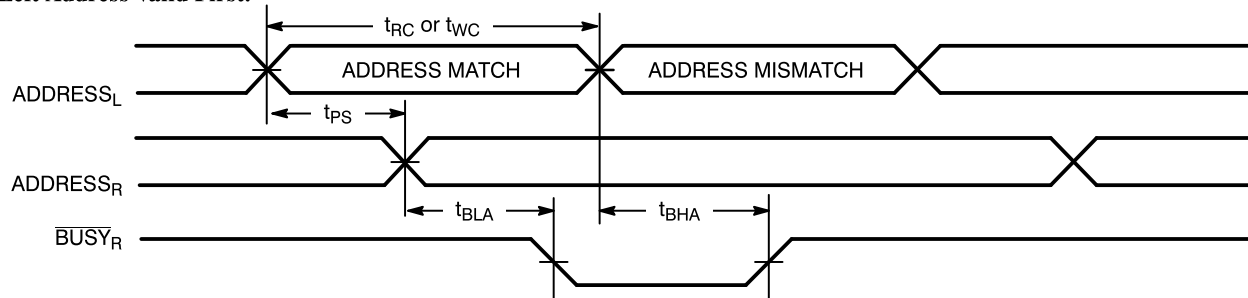
C130-11

Busy Timing Diagram No. 1 (\overline{CE} Arbitration)
 \overline{CE}_L Valid First:


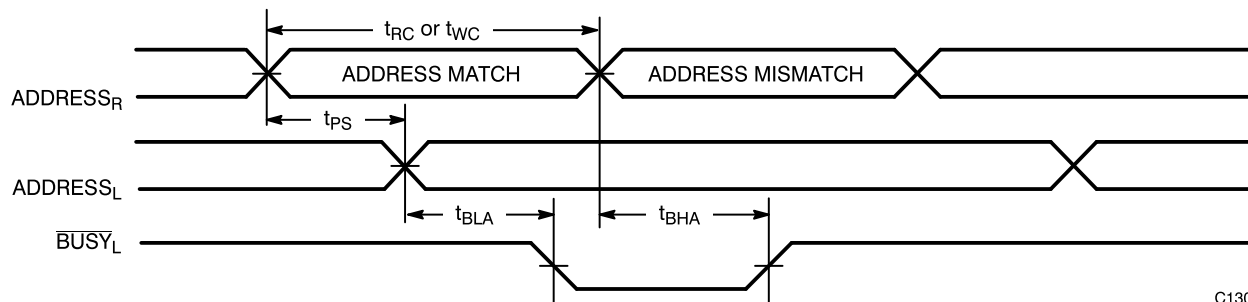
C130-12

 \overline{CE}_R Valid First:


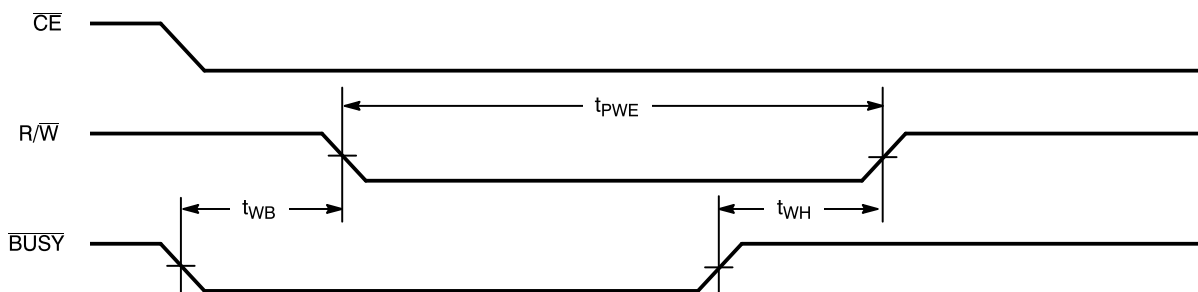
C130-13

Switching Waveforms (continued)
Busy Timing Diagram No. 2 (Address Arbitration)
Left Address Valid First:


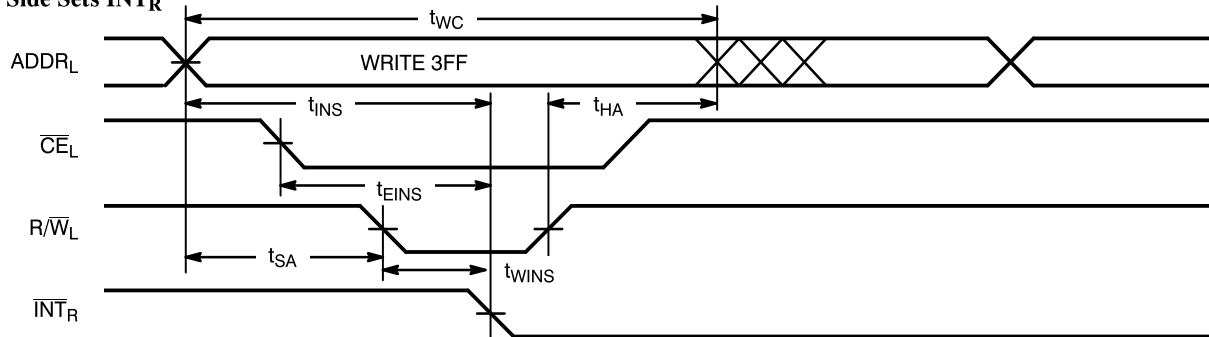
C130-14

Right Address Valid First:


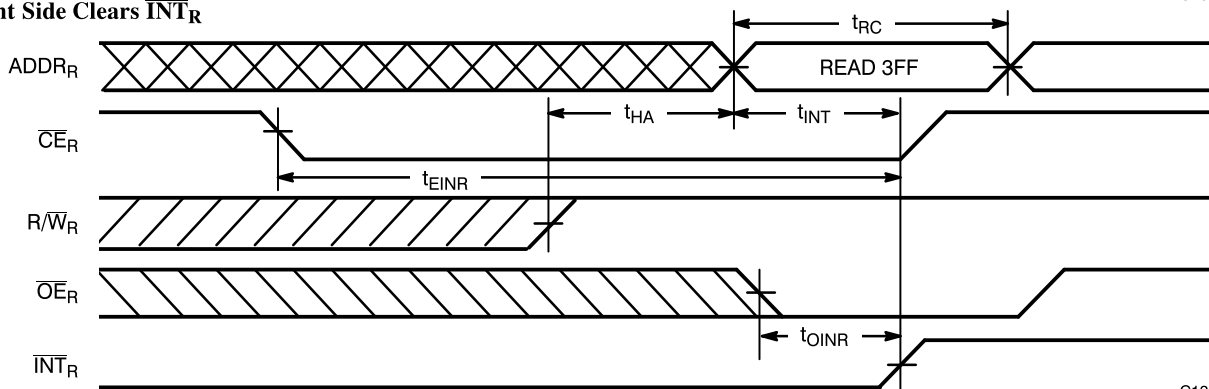
C130-15

Busy Timing Diagram No. 3
Write with $\overline{\text{BUSY}}$ (Slave: CY7C140/CY7C141)


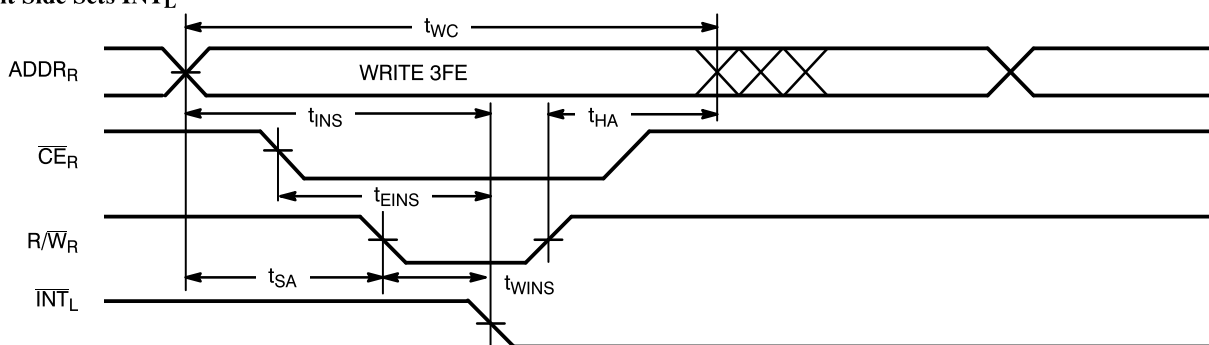
C130-16

Switching Waveforms (continued)
Interrupt Timing Diagrams
Left Side Sets $\overline{\text{INT}}_R$


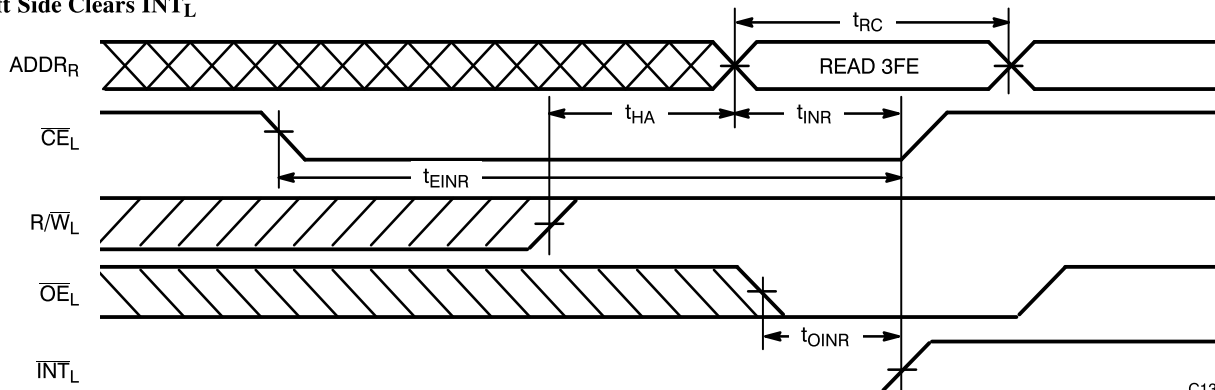
C130-17

Right Side Clears $\overline{\text{INT}}_R$


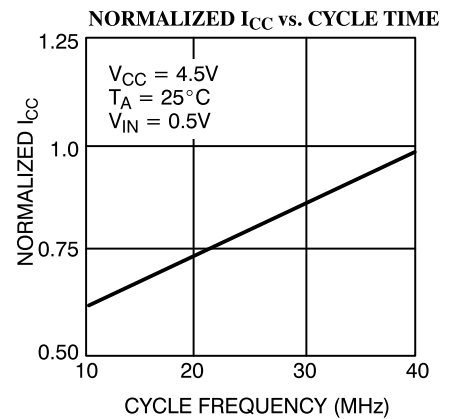
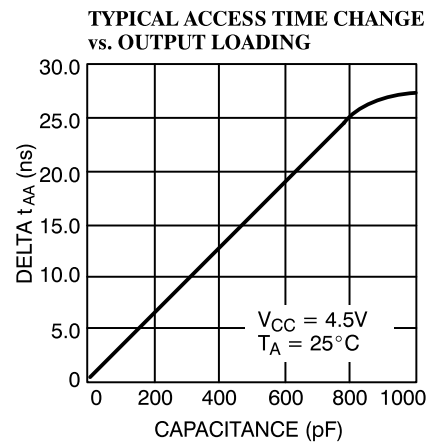
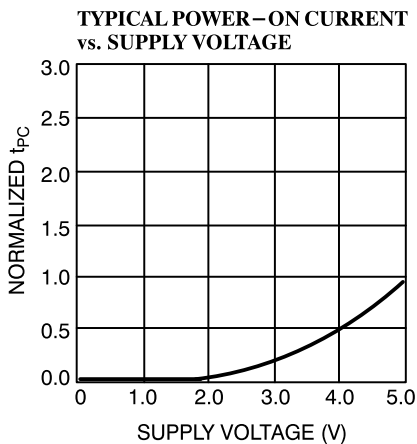
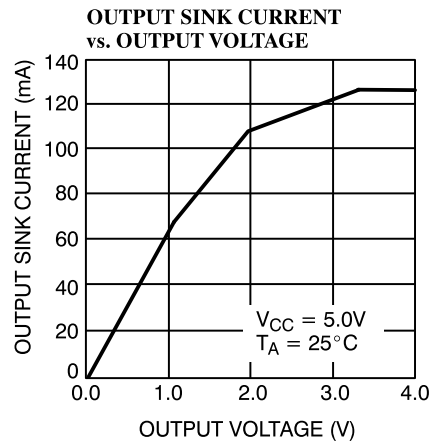
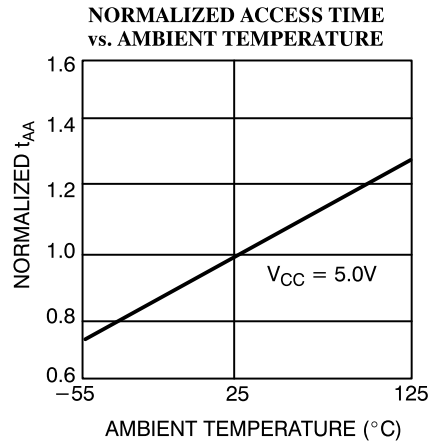
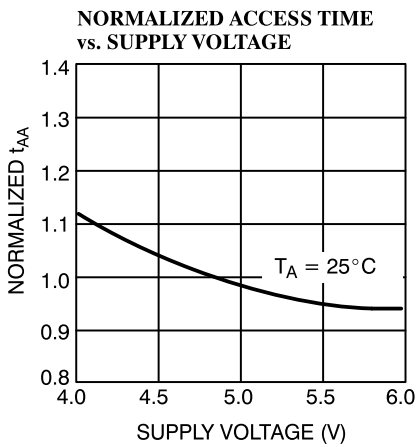
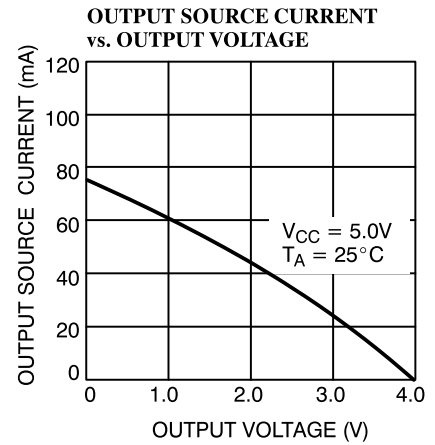
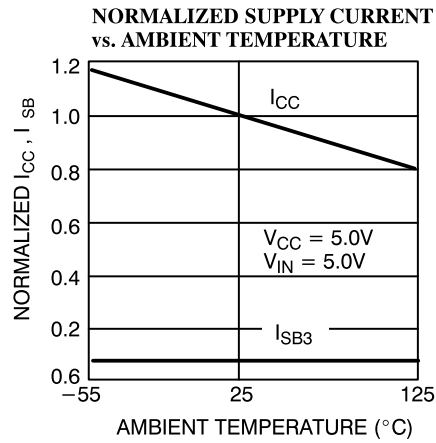
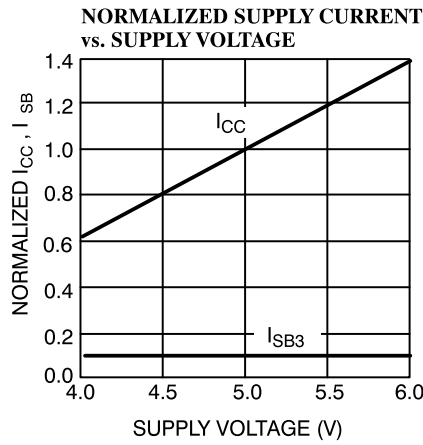
C130-18

Right Side Sets $\overline{\text{INT}}_L$


C130-19

Left Side Clears $\overline{\text{INT}}_L$


C130-20

Typical DC and AC Characteristics




Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C130–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C130–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130–35DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
45	CY7C130–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130–45DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
55	CY7C130–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130–55DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C131–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131–25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C131–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–30NC	N52	52-Pin Plastic Quad Flatpack	Industrial
	CY7C131–30JI	J69	52-Lead Plastic Leaded Chip Carrier	
35	CY7C131–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–35NC	N52	52-Pin Plastic Quad Flatpack	Industrial
	CY7C131–35JI	J69	52-Lead Plastic Leaded Chip Carrier	
	CY7C131–35NI	N52	52-Pin Plastic Quad Flatpack	Military
	CY7C131–35LMB	L69	52-Square Leadless Chip Carrier	
45	CY7C131–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–45NC	N52	52-Pin Plastic Quad Flatpack	Industrial
	CY7C131–45JI	J69	52-Lead Plastic Leaded Chip Carrier	
	CY7C131–45NI	N52	52-Pin Plastic Quad Flatpack	Military
	CY7C131–45LMB	L69	52-Square Leadless Chip Carrier	
55	CY7C131–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–55NC	N52	52-Pin Plastic Quad Flatpack	Industrial
	CY7C131–55JI	J69	52-Lead Plastic Leaded Chip Carrier	
	CY7C131–55NI	N52	52-Pin Plastic Quad Flatpack	Military
	CY7C131–55LMB	L69	52-Square Leadless Chip Carrier	



Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C140–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C140–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140–35DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
45	CY7C140–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140–45DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
55	CY7C140–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140–55DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C141–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141–25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C141–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–30NC	N52	52-Pin Plastic Quad Flatpack	Industrial
	CY7C141–30JI	J69	52-Lead Plastic Leaded Chip Carrier	
35	CY7C141–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–35NC	N52	52-Pin Plastic Quad Flatpack	Industrial
	CY7C141–35JI	J69	52-Lead Plastic Leaded Chip Carrier	
	CY7C141–35NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C141–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–45NC	N52	52-Pin Plastic Quad Flatpack	Industrial
	CY7C141–45JI	J69	52-Lead Plastic Leaded Chip Carrier	
	CY7C141–45NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C141–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–55NC	N52	52-Pin Plastic Quad Flatpack	Industrial
	CY7C141–55JI	J69	52-Lead Plastic Leaded Chip Carrier	
	CY7C141–55NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–55LMB	L69	52-Square Leadless Chip Carrier	Military



MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3
I _{SB3}	1, 2, 3
I _{SB4}	1, 2, 3

Switching Characteristics

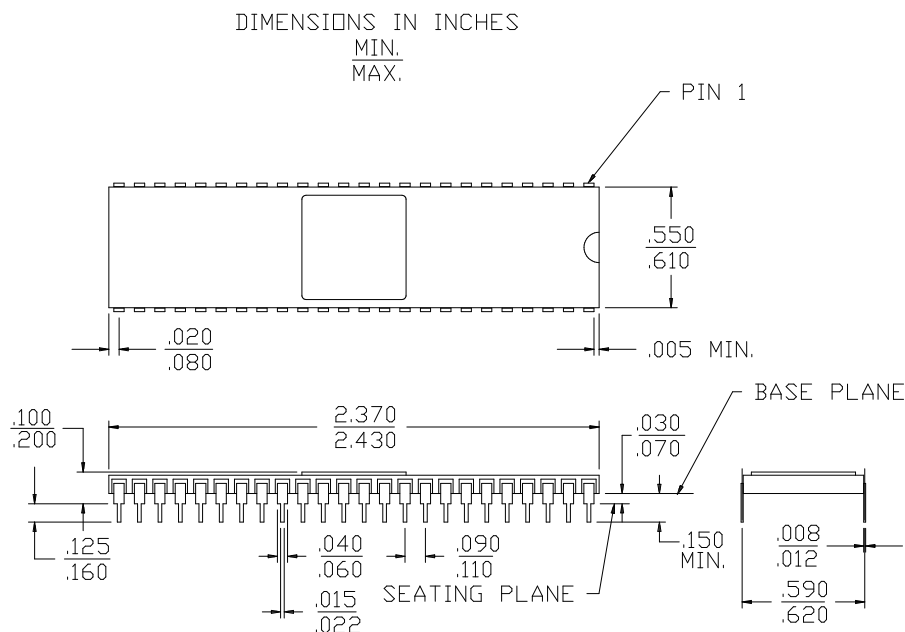
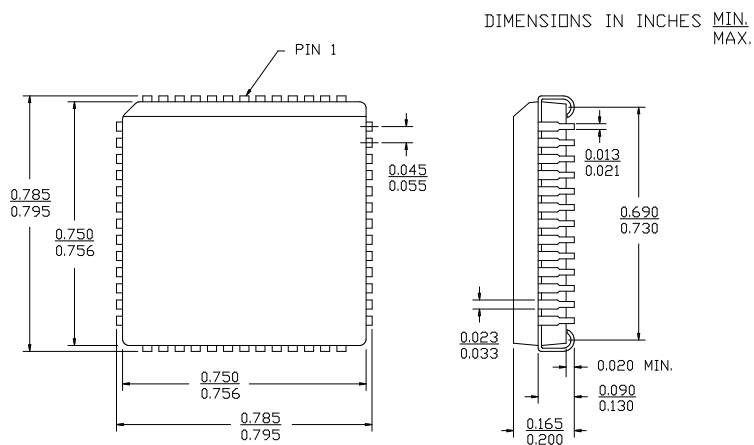
Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t _{BLA}	7, 8, 9, 10, 11
t _{BHA}	7, 8, 9, 10, 11
t _{BLC}	7, 8, 9, 10, 11
t _{BHC}	7, 8, 9, 10, 11
t _{PS}	7, 8, 9, 10, 11
t _{WINS}	7, 8, 9, 10, 11
t _{EINS}	7, 8, 9, 10, 11
t _{INS}	7, 8, 9, 10, 11
t _{OINR}	7, 8, 9, 10, 11
t _{EINR}	7, 8, 9, 10, 11
t _{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t _{WB} ^[23]	7, 8, 9, 10, 11
t _{WH}	7, 8, 9, 10, 11
t _{BDD}	7, 8, 9, 10, 11

Note:

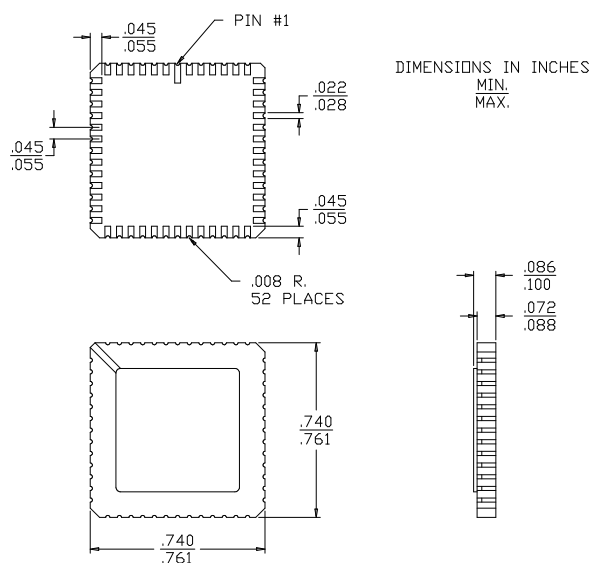
23. CY7C140/CY7C141 only.

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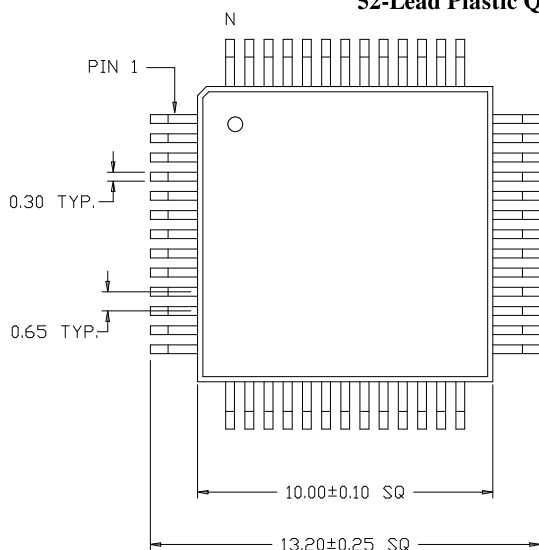
Package Diagrams
48-Lead (600-Mil) Sidebrazed DIP D26

52-Lead Plastic Leaded Chip Carrier J69


Package Diagrams (continued)

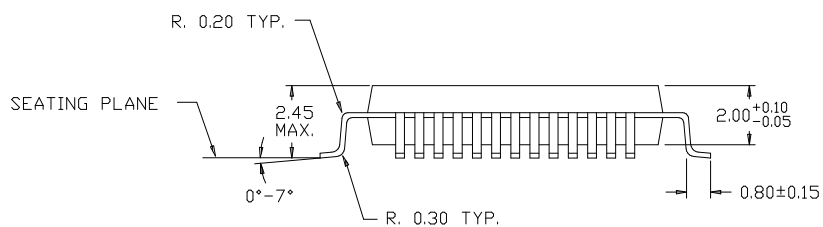
52-Square Leadless Chip Carrier L69



52-Lead Plastic Quad Flatpack N52



DIMENSIONS ARE IN MILLIMETERS
 LEAD COPLANARITY 0.102 MAX.





Package Diagrams (continued)

48-Lead (600-Mil) Molded DIP P25

