PRELIMINARY

CY7C133
CY7C143

2K x 16 Dual-Port Static RAM

Features

- **0.8-micron CMOS for optimum speed/power**
- **High speed access: 25 ns**
- **Low operating power: I_{CC} = 170 mA (typ.)**
- **Automatic power-down**
- **TTL compatible**
- **Fully asynchronous operation**
- **Master CY7C133 easily expands data bus width to 32 or more bits using slave CY7C143**
- **$\overline{BUSY}$ output flag on CY7C133; $\overline{BUSY}$ input on CY7C143**
- **Available in 68-pin PLCC**
- **Pin compatible and functionally equivalent to IDT7133 and IDT7143**

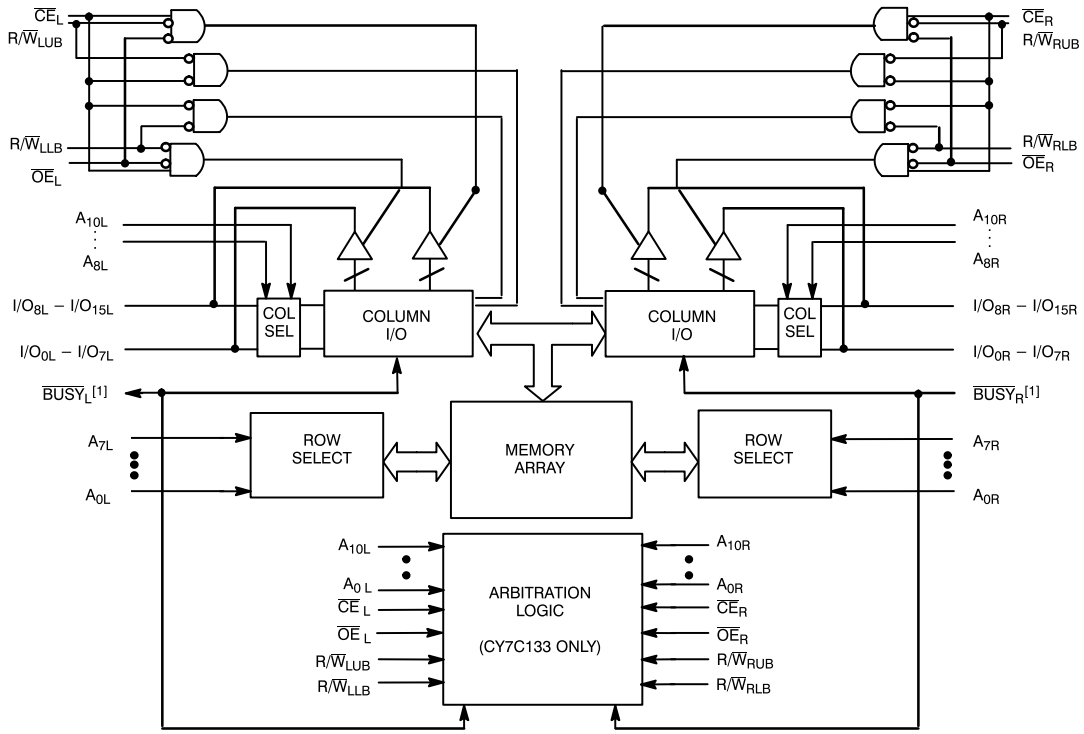
Functional Description

The CY7C133 and CY7C143 are high-speed CMOS 2K by 16 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C133 can be utilized as either a standalone 16-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C143 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable ($R/\overline{W}_{UB}$, $R/\overline{W}_{LB}$), and output enable ($\overline{OE}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C133 and CY7C143 are available in 68-pin PLCC.

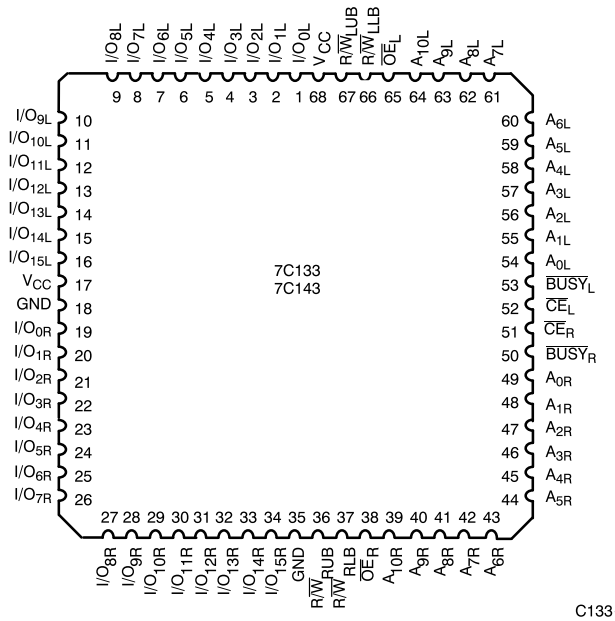
Logic Block Diagram



Notes:
1. CY7C133 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor. CY7C143 (Slave): $\overline{BUSY}$ is input.

Pin Configuration

68-Pin LCC/PLCC
Top View



C133–2

Selection Guide

	7C133–25 7C143–25	7C133–35 7C143–35	7C133–55 7C143–55
Maximum Access Time (ns)	25	35	55
Typical Operating Current I_{CC} (mA)	170	160	150
Typical Standby Current for I_{SB1} (mA)	40	30	20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

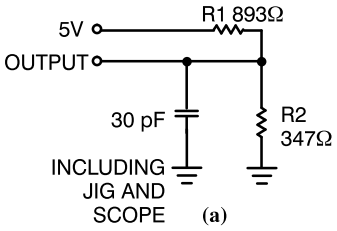
Parameter	Description	Test Conditions		7C133−25 7C143−25 Min.	Typ.	Max.	7C133−35 7C143−35 Min.	Typ.	Max.	7C133−55 7C143−55 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA				0.4			0.4			0.4	V
		I_{OL} = 16.0 mA[3]				0.5			0.5			0.5	
V_{IH}	Input HIGH Voltage			2.2			2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−5		+5	−5		+5	−5		+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5		+5	−5		+5	−5		−5	µA
I_{OS}	Output Short Circuit Current[4, 5]	V_{CC} = Max., V_{OUT} = GND				−200			−200			−200	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[6]	Com'l		170	250		160	230		150	220	mA
			Ind		170	290		160	260		150	250	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[6]	Com'l		40	60		30	50		20	40	mA
			Ind		40	75		30	65		20	55	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[6]	Com'l		100	140		85	125		75	110	mA
			Ind		100	160		85	140		75	125	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		3	15		3	15		3	15	mA
			Ind		3	15		3	15		3	15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[6]	Com'l		90	120		80	105		70	90	mA
			Ind		90	140		80	120		70	105	

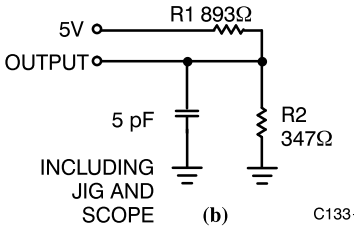
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

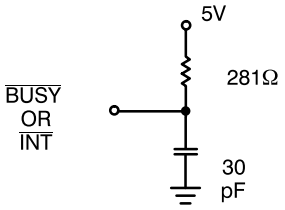
Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. $\overline{BUSY}$ pin only.
4. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.
6. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of 1/t_{RC} and using AC Test Waveforms input levels of GND to 3V.

AC Test Loads and Waveforms

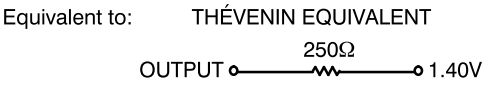


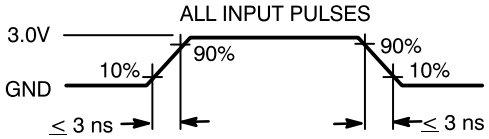


C133–3



BUSY Output Load (CY7C133 ONLY)





C133–4

Switching Characteristics Over the Operating Range[7]

Parameter	Description	7C133–25 7C143–25		7C133–35 7C143–35		7C133–55 7C143–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		55		ns
t_{AA}	Address to Data Valid[8]		25		35		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[8]		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[8]		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9, 10]	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9, 10]		15		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9, 10]	3		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		15		20		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		25		25	ns
WRITE CYCLE[11]								
t_{WC}	Write Cycle Time	25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		40		ns
t_{AW}	Address Set-Up to Write End	20		25		40		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	20		25		35		ns
t_{SD}	Data Set-Up to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z[10]		15		20		20	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z[10]	0		0		0		ns

Notes:

7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
8. AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
9. At any given temperature and voltage condition for any given device, t_{LZCE} is less than t_{HZCE} and t_{LZOE} is less than t_{HZOE}.
10. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

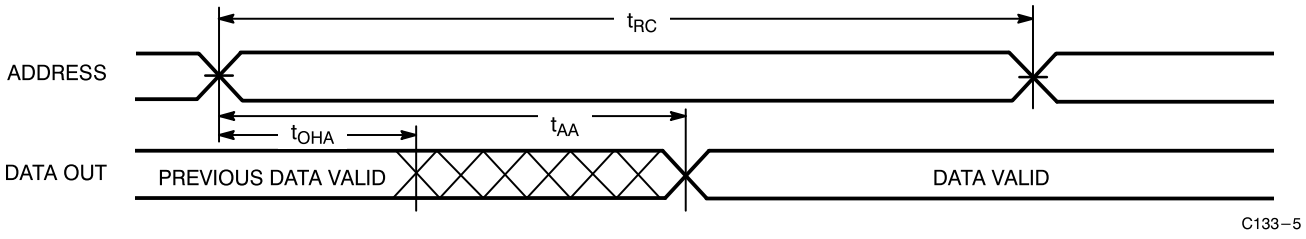
Switching Characteristics Over the Operating Range[2,7] (continued)

Parameter	Description	7C133−25 7C143−25		7C133−35 7C143−35		7C133−55 7C143−55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING (For Master CY7C133)								
t_{BLA}	$\overline{BUSY}$ Low from Address Match		25		35		50	ns
t_{BHA}	$\overline{BUSY}$ High from Address Mismatch		20		30		40	ns
t_{BLC}	$\overline{BUSY}$ Low from $\overline{CE}$ Low		20		25		35	ns
t_{BHC}	$\overline{BUSY}$ High from $\overline{CE}$ High		20		20		30	ns
t_{WDD}	Write Pulse to Data Delay[12]		50		60		80	ns
t_{DDD}	Write Data Valid to Read Data Valid[12]		35		45		55	ns
t_{BDD}	$\overline{BUSY}$ High to Valid Data[13]		Note 13		Note 13		Note 13	ns
t_{PS}	Arbitration Priority Set Up Time[14]	5		5		5		ns
BUSY TIMING (For Slave CY7C143)								
t_{WB}	Write to $\overline{BUSY}$[15]	0		0		0		ns
t_{WH}	Write Hold After $\overline{BUSY}$[16]	20		25		30		ns
t_{WDD}	Write Pulse to Data Delay[17]		50		60		80	ns
t_{DDD}	Write Data Valid to Read Data Valid[17]		35		45		55	ns

Switching Waveforms

Read Cycle No. 1[18, 19]

Either Port Address Access



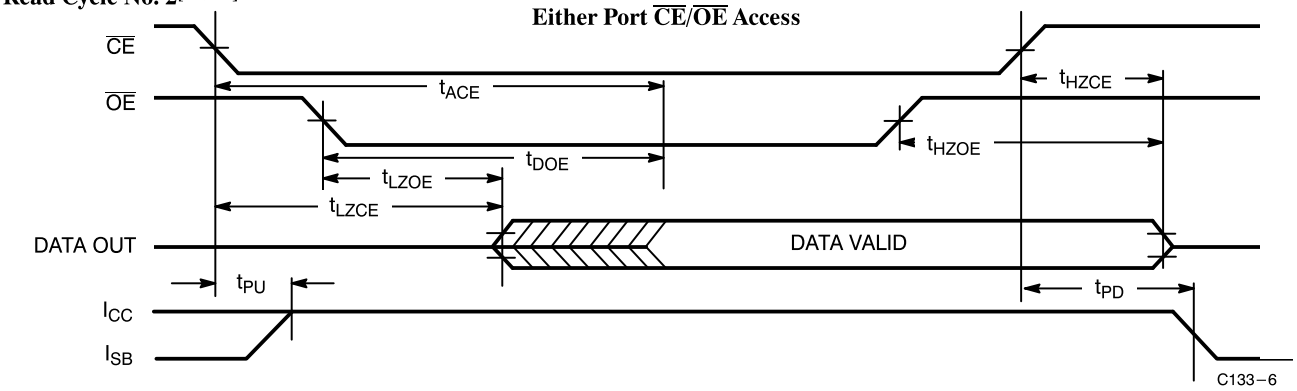
Notes:

12. Port-to-port delay through RAM cells from writing port to reading port. Refer to timing waveform of "Read with $\overline{BUSY}$, Master: CY7C133."
13. t_{BDD} is calculated parameter and is greater of 0,$t_{WDD}-$twp (actual) or $t_{DDD}-t_{DW}$ (actual).
14. To ensure that the earlier of the two ports wins.
15. To ensure that write cycle is inhibited during contention.
16. To ensure that a write cycle is completed after contention.
17. Port-to-port delay through RAM cells from writing port to reading port. Refer to timing waveform of "Read with Port-to-port Delay."
18. R/$\overline{W}$ is HIGH for read cycle
19. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.

Switching Waveforms (continued)

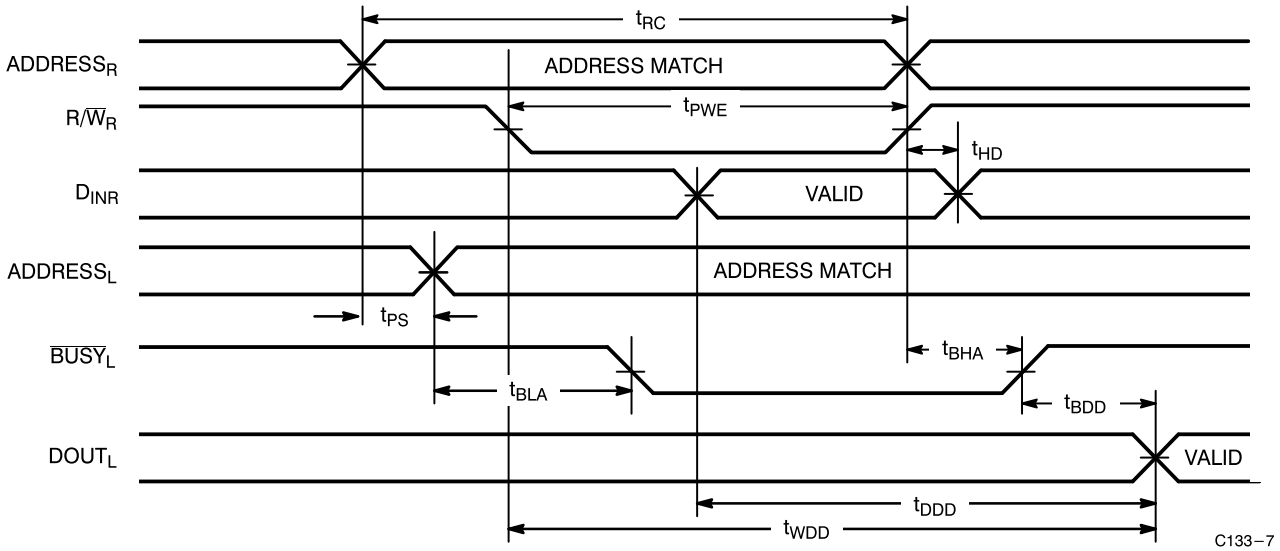
Read Cycle No. 2[18, 20]

Either Port $\overline{CE}$/$\overline{OE}$ Access



Read Cycle No. 3[19]

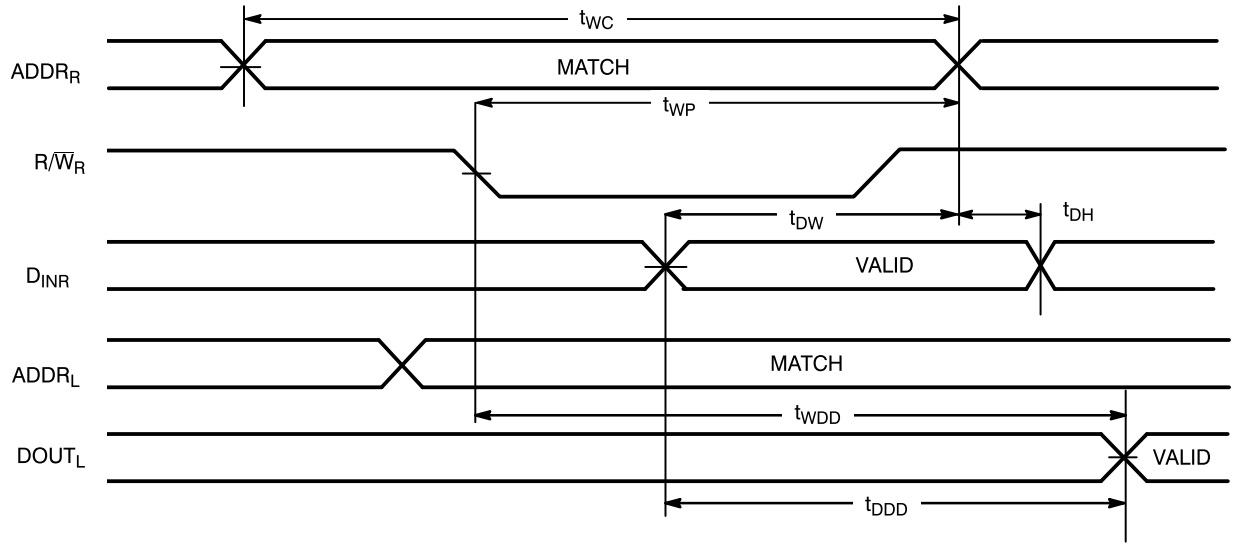
Read with $\overline{BUSY}$, Master: CY7C133



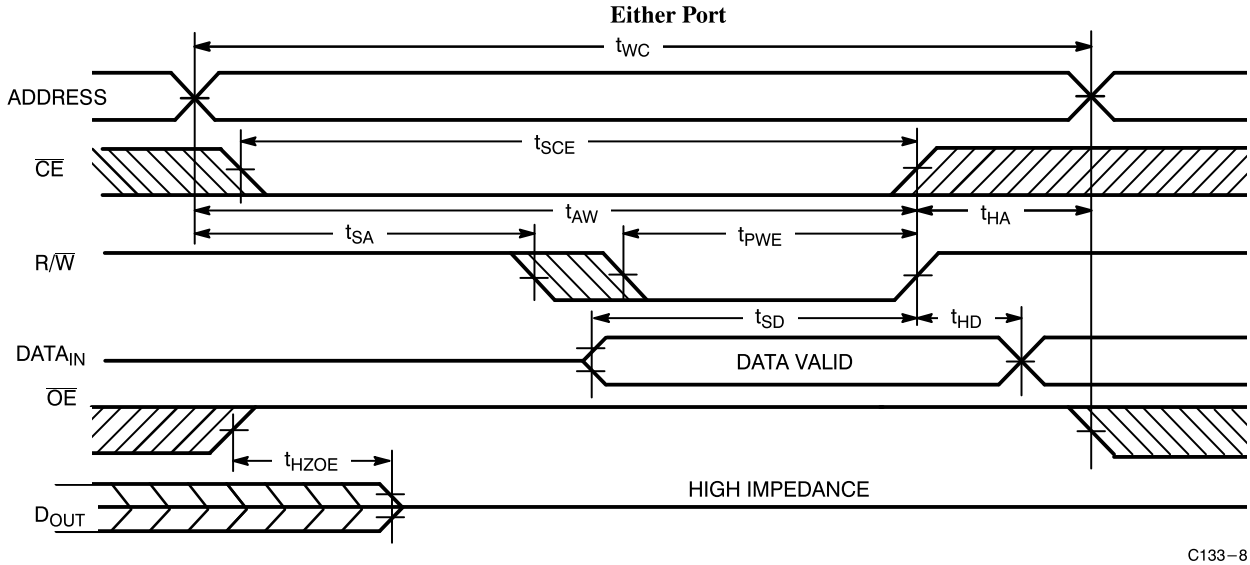
Notes:
20. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Timing Waveform of Read with Port-to-port Delay No. 4 (For Slave CY7C143)[21,22,23]



Write Cycle No.1 ($\overline{OE}$ Three-States Data I/Os − Either Port)[11, 24]

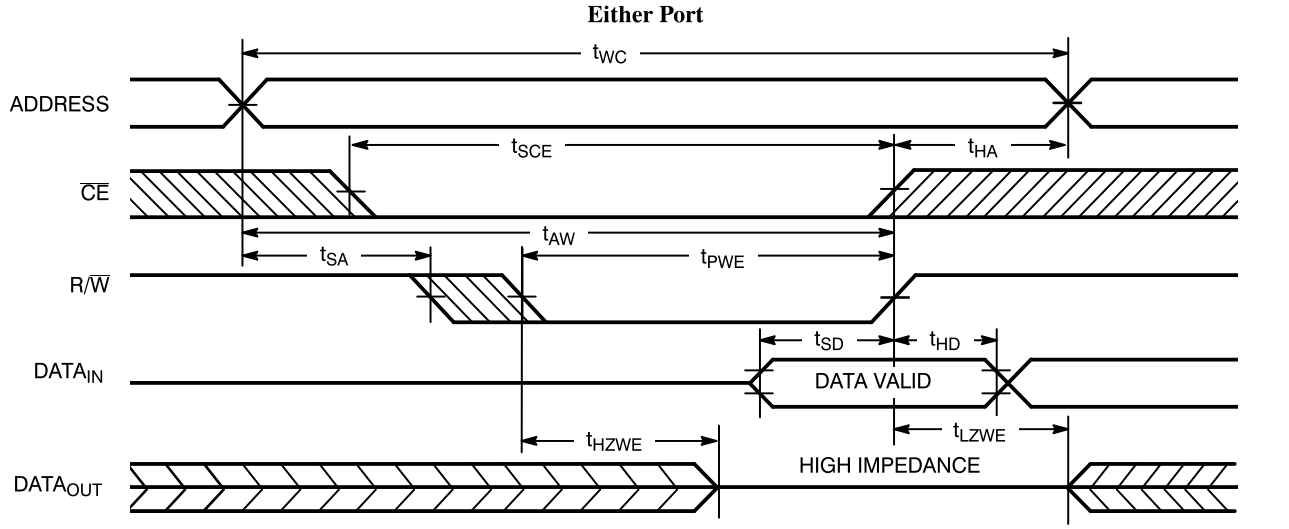


Notes:

21. Assume $\overline{BUSY}$ input at V_{IH} for the writing port and at V_{IL} for the reading port.
22. Write cycle parameters should be adhered to inorder to ensure proper writing.
23. Device is continuously enabled for both ports.
24. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.

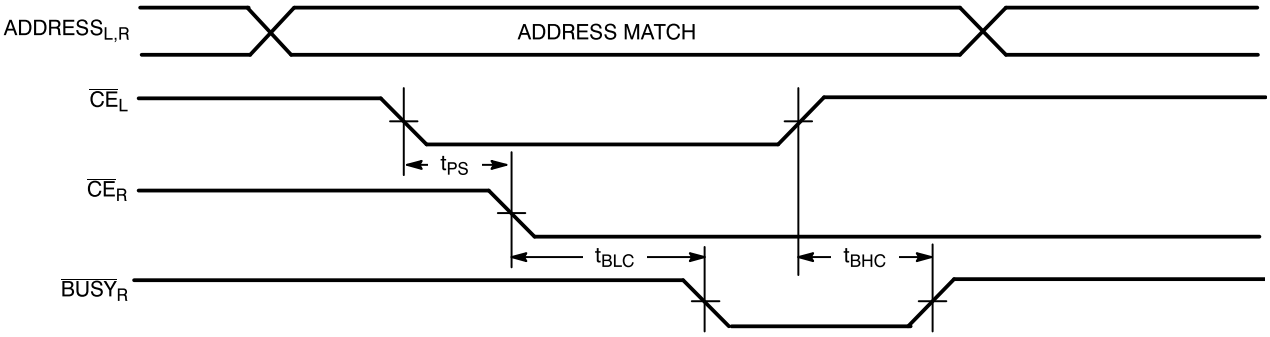
Switching Waveforms (continued)

Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os − Either Port)[20,25]

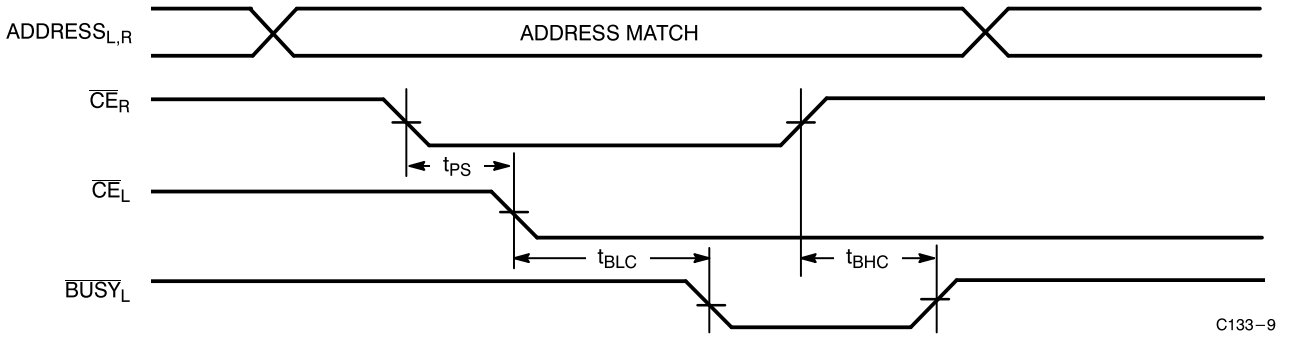


Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



$\overline{CE}_R$ Valid First:



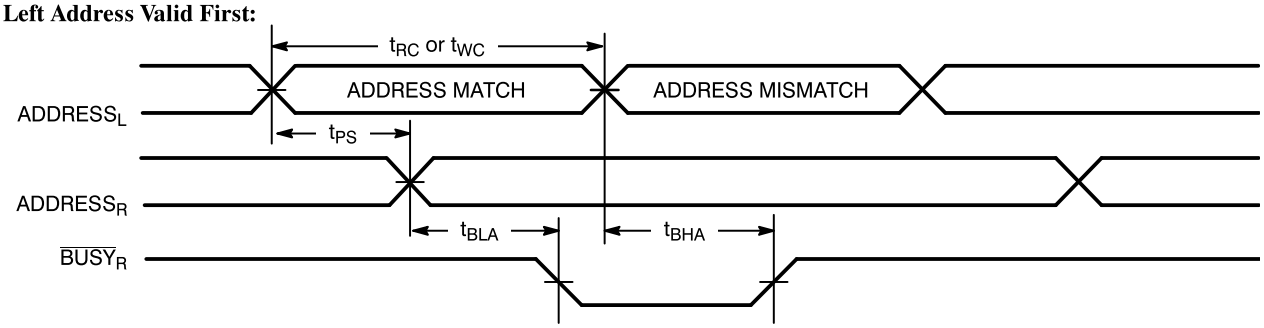
Note:

25. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

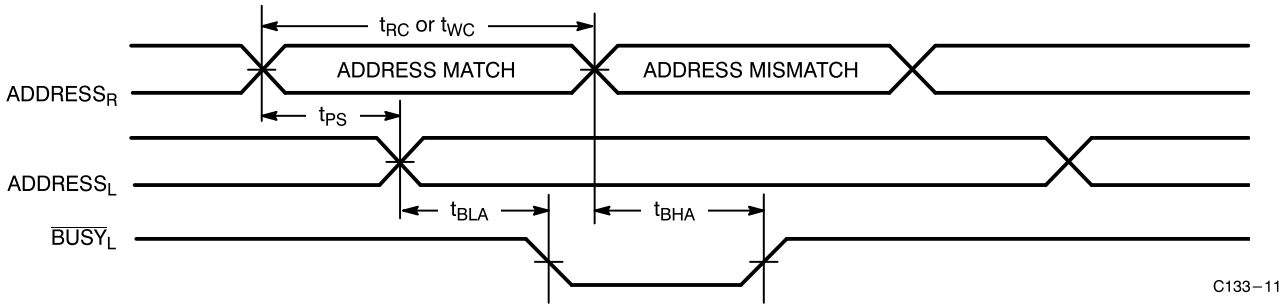
Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:

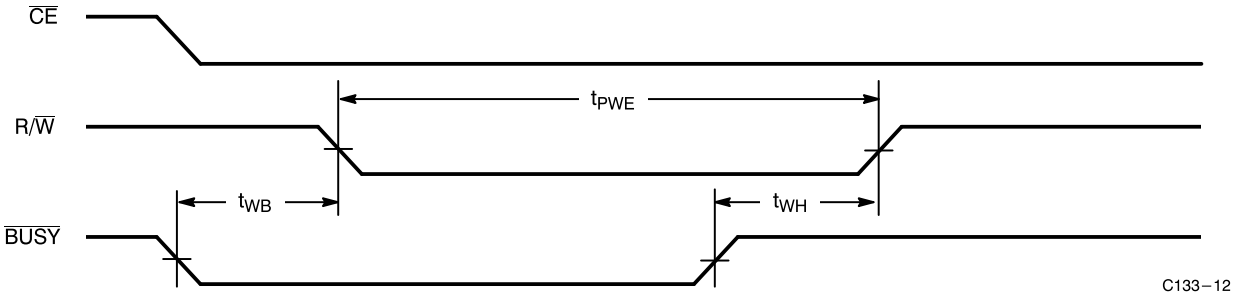


Right Address Valid First:

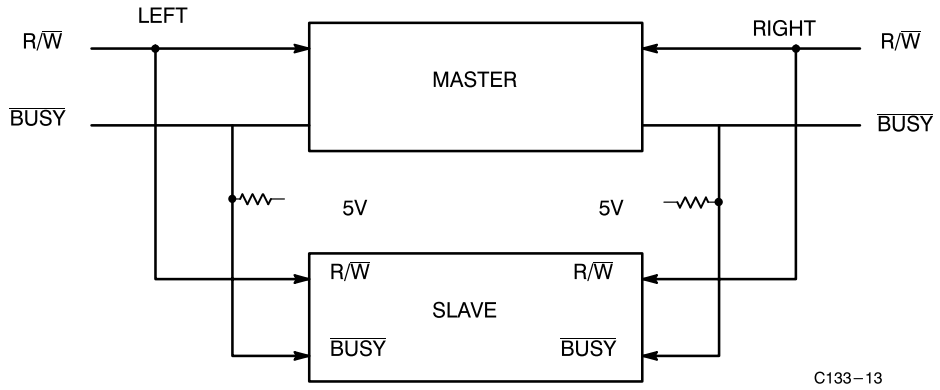


Busy Timing Diagram No. 3

Write with $\overline{\text{BUSY}}$ (Slave: CY7C143)



32-Bit Master/Slave Dual-Port Memory Systems



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C133–25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C133–25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C133–35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C133–35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
55	CY7C133–55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C133–55JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C143–25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143–25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C143–35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143–35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
55	CY7C143–55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143–55JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[26]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

Note:
26. CY7C143 only.

Document #: 38−00414

Package Diagrams

68-Lead Plastic Leaded Chip Carrier J81