CY29FCT52T

8-Bit Registered Transceiver

Features

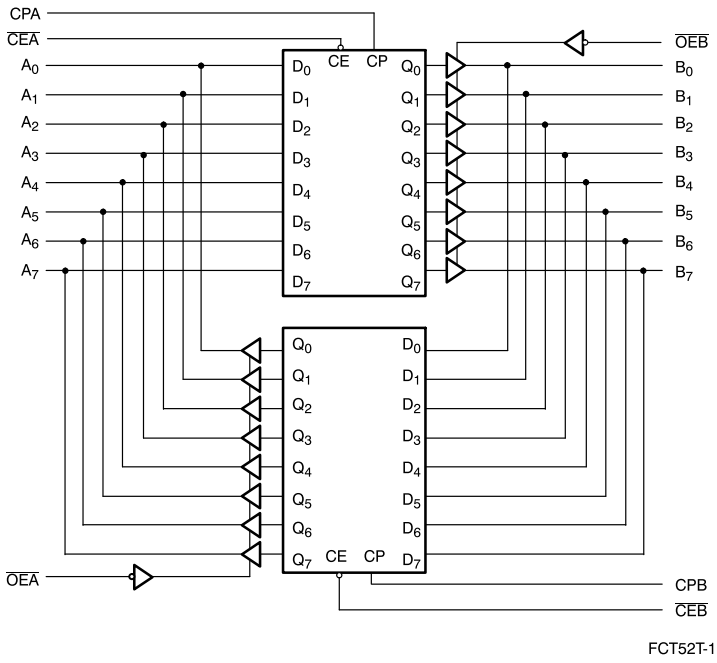
- **Function, pinout, and drive compatible with FCT, F Logic and AM2952**
- **FCT-C speed at 6.3 ns max. (Com'l) FCT-B speed at 7.5 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **ESD > 2000V**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink Current 64 mA (Com'l), 48 mA (Mil)**
- **Source Current 32 mA (Com'l), 12 mA (Mil)**

Functional Description

The CY29FCT52T has two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Separate clock, clock enable, and three-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64 mA.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram



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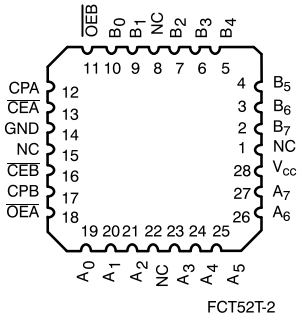
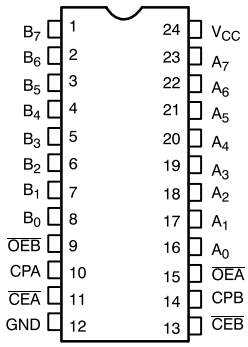
Pin Configurations

LCC
Top View



FCT52T-2

DIP/SOIC/QSOP
Top View



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Function Table[1]

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	⌐	L	L	Load Data
H	⌐	L	H	

Output Control

$\overline{OE}$	Internal Q	Y-Outputs	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

Note:
1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

Pin Description

Name	Description
A	A register inputs or B register outputs.
B	B register inputs or A register outputs.
CPA	Clock for the A register. When $\overline{CEA}$ is LOW, data is entered into the A register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	Clock Enable for the A register. When $\overline{CEA}$ is LOW, data is entered into the A register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A register holds its contents regardless of CPA signal transitions.
$\overline{OEA}$	Output Enable for the A register. When $\overline{OEA}$ is LOW, the A register outputs are enabled onto the B lines. When $\overline{OEA}$ is HIGH, the B outputs are in the high impedance state.
CPB	Clock for the B register. When $\overline{CEB}$ is LOW, data is entered into the B register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	Clock Enable for the B register. When $\overline{CEB}$ is LOW, data is entered into the B register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B register holds its contents regardless of CPA signal transitions.
$\overline{OEB}$	Output Enable for the B register. When $\overline{OEB}$ is LOW, the B register outputs are enabled onto the A lines. When $\overline{OEB}$ is HIGH, the A outputs are in the high impedance state.

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	AT, BT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the “instant on” case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=48mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTLinputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OEA}$ or $\overline{OEB}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{OEA}$ or $\overline{OEB}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{OEA}$ or $\overline{OEB}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OEA}$ or $\overline{OEB}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.6	3.2[11]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OEA}$ or $\overline{OEB}$=GND, V_{IN}=3.4V or V_{IN}=GND	3.9	12.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	29FCT52AT				29FCT52BT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to A, B	2.0	11.0	2.0	10.0	2.0	8.0	2.0	7.5	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A or B	1.5	13.0	1.5	10.5	1.5	8.5	1.5	8.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A or B	1.5	10.0	1.5	10.0	1.5	8.0	1.5	7.5	ns	1, 7, 8
t_S	Set-Up Time HIGH or LOW, A, B to CPA, CPB	2.5		2.5		2.5		2.5		ns	4
t_H	Hold Time HIGH or LOW, A, B to CPA, CPB	2.0		2.0		1.5		1.5		ns	4
t_S	Set-Up Time HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	3.0		3.0		3.0		3.0		ns	4
t_H	Hold Time HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	2.0		2.0		2.0		2.0		ns	4
t_W	Pulse Width,[6] HIGH or LOW, CPA or CPB	3.0		3.0		3.0		3.0		ns	5

Parameter	Description	29FCT52CT				Unit	Fig. No.[13]
		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to A, B	2.0	7.3	2.0	6.3	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time, $\overline{OEA}$ or $\overline{OEB}$ to A or B	1.5	8.0	1.5	7.0	ns	1, 7, 8
t_{PHZ} t_{PHZ}	Output Disable Time, $\overline{OEA}$ or $\overline{OEB}$ to A or B	1.5	7.5	1.5	6.5	ns	1, 7, 8
t_S	Set-Up Time HIGH or LOW, A, B to CPA, CPB	2.5		2.5		ns	4
t_H	Hold Time HIGH or LOW, A, B to CPA, CPB	1.5		1.5		ns	4
t_S	Set-Up Time HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	3.0		3.0		ns	4
t_H	Hold Time HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	2.0		2.0		ns	4
t_W	Pulse Width,[6] HIGH or LOW, CPA or CPB	3.0		3.0		ns	5

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY29FCT52CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT52CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT52CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.3	CY29FCT52CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT52CTLMB	L64	28-Square Leadless Chip Carrier	
7.5	CY29FCT52BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT52BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT52BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
8.0	CY29FCT52BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT52BTLMB	L64	28-Square Leadless Chip Carrier	
10.0	CY29FCT52ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT52ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY29FCT52ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY29FCT52ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY29FCT52ATLMB	L64	28-Square Leadless Chip Carrier	

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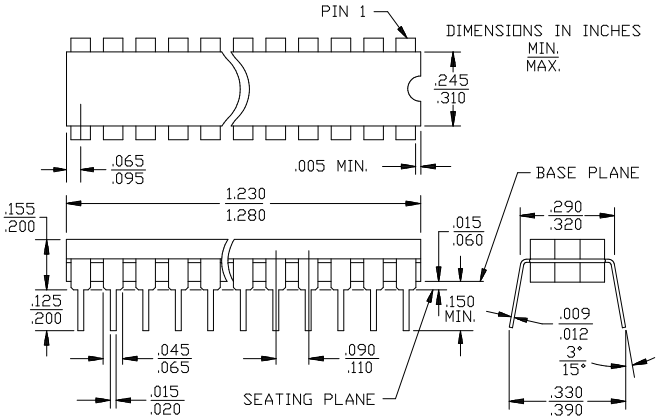
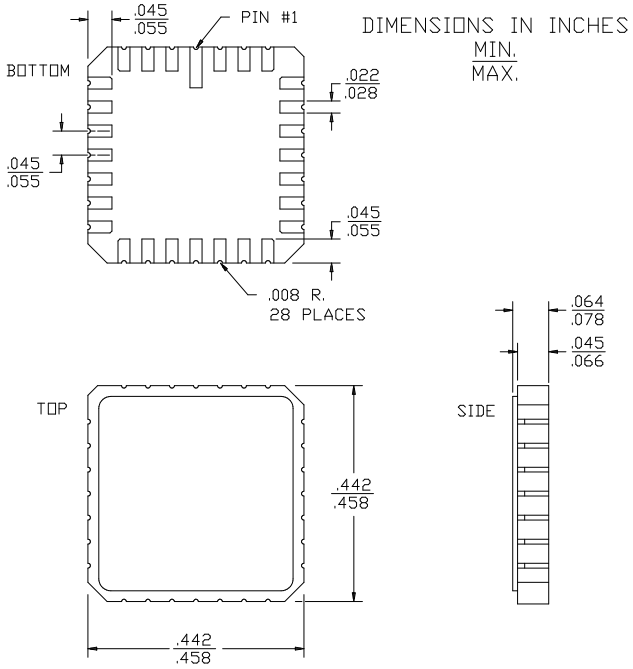
Package Diagrams

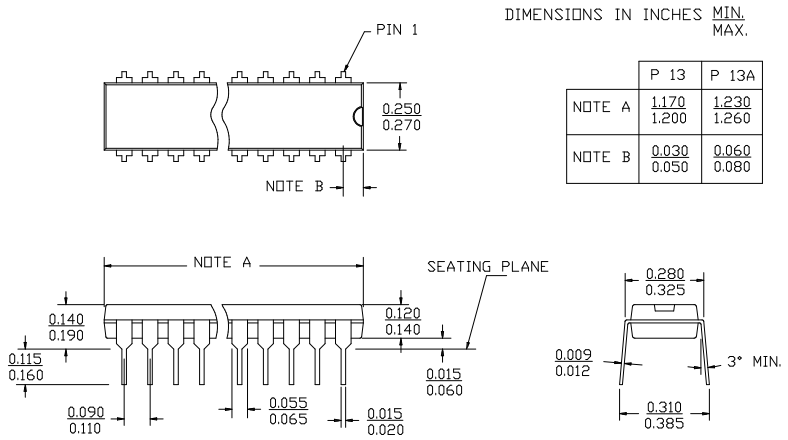
24-Lead (300-Mil) CerDIP D14
MIL−STD−1835 D−9 Config. A



28-Square Leadless Chip Carrier L64
MIL−STD−1835 C−4



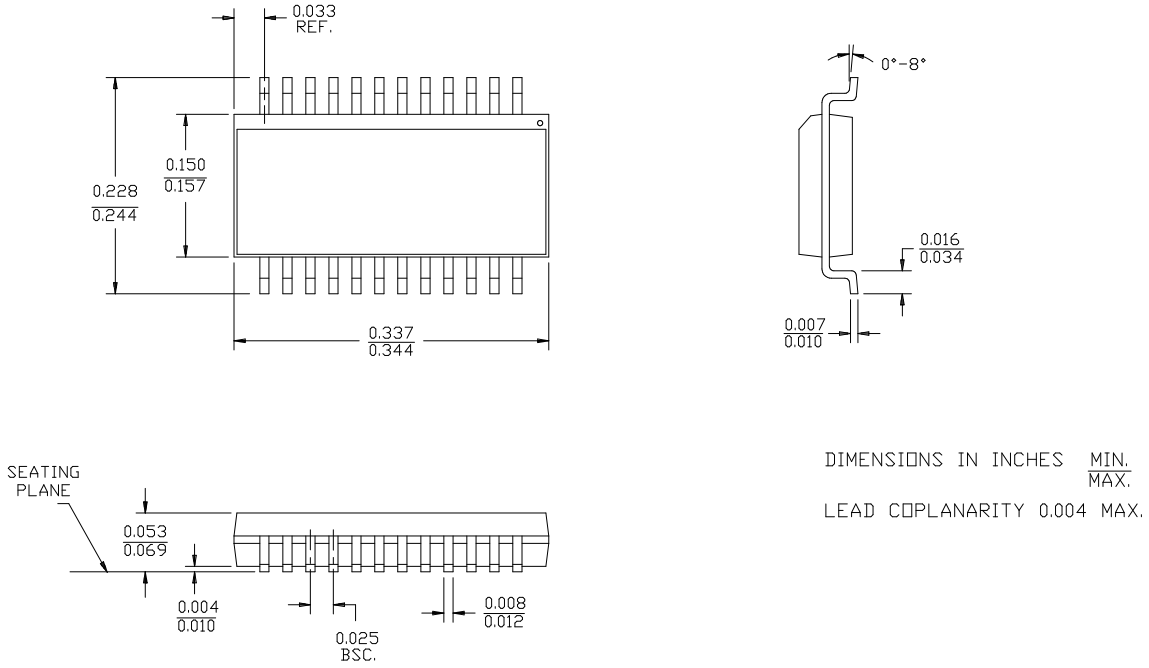
24-Lead (300-Mil) Molded DIP P13/P13A



	P 13	P 13A
NOTE A	1.170 1.200	1.230 1.260
NOTE B	0.030 0.050	0.060 0.080

Package Diagrams (continued)

24-Lead Quarter Size Outline Q13



24-Lead (300-Mil) Molded SOIC S13