CY54/74FCT163T

4-Bit Binary Counter

Features

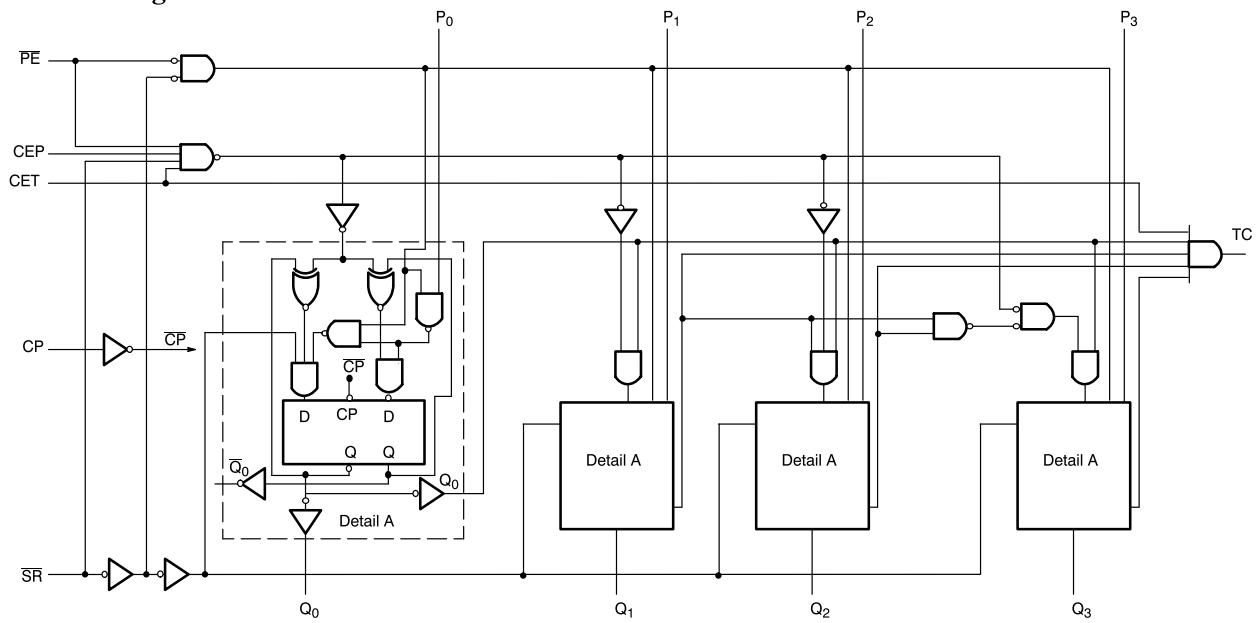
- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 5.8 ns max. (Com'l), FCT-A speed at 7.2 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
- **Source current 32 mA (Com'l), 12 mA (Mil)**

Functional Description

The FCT163T is a high-speed synchronous modulo-16 binary counter. It is synchronously presettable for application in programmable dividers and has two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-staged counters. The FCT163T has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

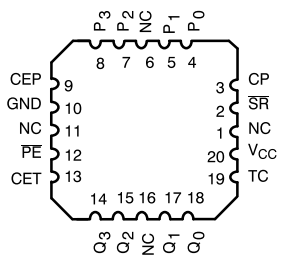
Logic Block Diagram



FCT163T-1

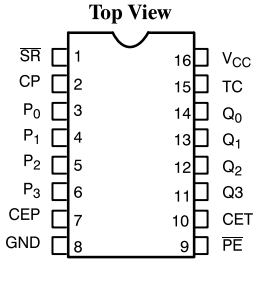
Pin Configurations

LCC
Top View



FCT163T-2

DIP/SOIC/QSOP
Top View



FCT163T-3

Function Table[1]

Inputs				Action on the Rising Clock Edge(s)
$\overline{SR}$	$\overline{PE}$	CET	CEP	
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Incremental)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

Pin Description

Name	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{SR}$	Synchronous Reset Input (Active LOW)
P	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q	Flip-Flop Outputs
TC	Terminal Count Output

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.2	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Bit Toggling, Load Mode, 50% Duty Cycle, Outputs Open, $\overline{CEP}$=CET=$\overline{PE}$=GND, $\overline{SR}$=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_0=10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{CEP}$=CET=$\overline{PE}$=GND, $\overline{SR}$=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, CEP=CET=$\overline{PE}$=GND, $\overline{SR}$=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=5 MHz, $\overline{CEP}$=CET=$\overline{PE}$=GND, $\overline{SR}$=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.6	3.2[11]	mA
		V_{CC}=Max., f_0=10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=5 MHz, CEP=CET=$\overline{PE}$=GND, $\overline{SR}$=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	2.9	8.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT163T				FCT163AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Q ($\overline{PE}$ Input HIGH)	2.0	11.5	1.5	11.0	2.0	7.5	1.5	7.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$ ($\overline{PE}$ Input LOW)	2.0	10.0	1.5	9.5	2.0	6.5	1.5	6.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	2.0	16.5	1.5	15.0	2.0	10.8	1.5	9.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CET to $\overline{TC}$	1.5	9.0	1.5	8.5	1.5	5.9	1.5	5.5	ns	1, 5
t_S	Set-Up Time, HIGH or LOW P to CP	5.5		4.0		4.5		4.0		ns	4
t_H	Hold Time, HIGH or LOW P to CP	2.0		1.5		2.0		1.5		ns	4
t_{SU}	Set-Up Time HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	13.5		9.5		11.5		9.5		ns	4
t_H	Hold Time HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	1.5		1.5		1.5		1.5		ns	4
t_{SU}	Set-Up Time HIGH or LOW CEP or CET to CP	13.0		9.5		11.0		9.5		ns	4
t_H	Hold Time HIGH or LOW CEP or CET to CP	0		0		0		0		ns	4
t_W	Clock Pulse Width (Load) HIGH or LOW	5.0		4.0		4.0		4.0		ns	5
t_W	Clock Pulse Width(Count) HIGH or LOW	8.0		6.0		7.0		6.0		ns	5

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.

Switching Characteristics Over the Operating Range (continued)

Parameter	Description	FCT163CT				Unit	Fig. No.[13]
		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Q ($\overline{PE}$ Input HIGH)	1.5	6.1	1.5	5.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to TC ($\overline{PE}$ Input LOW)	1.5	5.5	1.5	5.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to TC	1.5	8.7	1.5	7.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CET to TC	1.5	4.8	1.5	4.4	ns	1, 5
t_S	Set-Up Time, HIGH or LOW P to CP	3.9		3.5		ns	4
t_H	Hold Time, HIGH or LOW P to CP	2.0		1.5		ns	4
t_{SU}	Set-Up Time, HIGH or LOW$\overline{PE}$ or $\overline{SR}$ to CP	9.0		7.6		ns	4
t_H	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	1.5		1.0		ns	4
t_{SU}	Set-Up Time, HIGH or LOW CEP or CET to CP	8.8		7.6		ns	4
t_H	Hold Time, HIGH or LOW CEP or CET to CP	0		0		ns	4
t_W	Clock Pulse Width (Load) HIGH or LOW	4.0		4.0		ns	5
t_W	Clock Pulse Width (Count) HIGH or LOW	6.0		5.0		ns	5

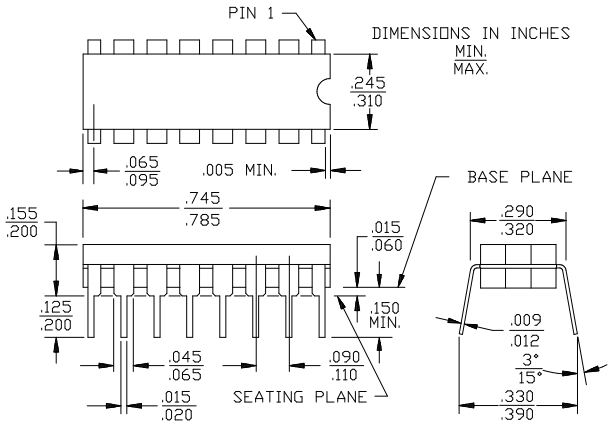
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.8	CY74FCT163CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT163CTQC	Q1	16-Lead (150-Mil) Quarter Size Outline	
	CY74FCT163CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
6.1	CY54FCT163CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT163CTLMB	L61	20-Square Leadless Chip Carrier	
7.2	CY74FCT163ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT163ATQC	Q1	16-Lead (150-Mil) Quarter Size Outline	
	CY74FCT163ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
7.5	CY54FCT163ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT163ATLMB	L61	20-Square Leadless Chip Carrier	
11.0	CY74FCT163TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT163TQC	Q1	16-Lead (150-Mil) Quarter Size Outline	
	CY74FCT163TSOC	S1	16-Lead (300-Mil) Molded SOIC	
11.5	CY54FCT163TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT163TLMB	L61	20-Square Leadless Chip Carrier	

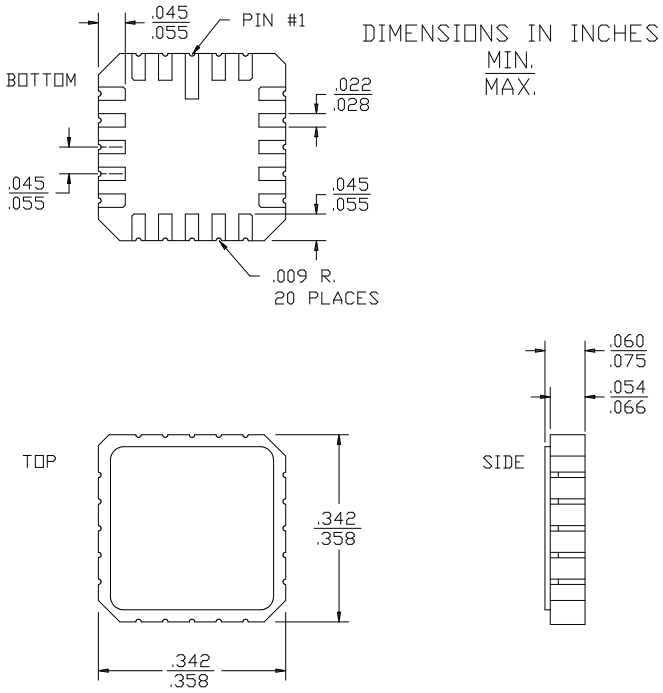
Document #: 38−00285−A

Package Diagrams

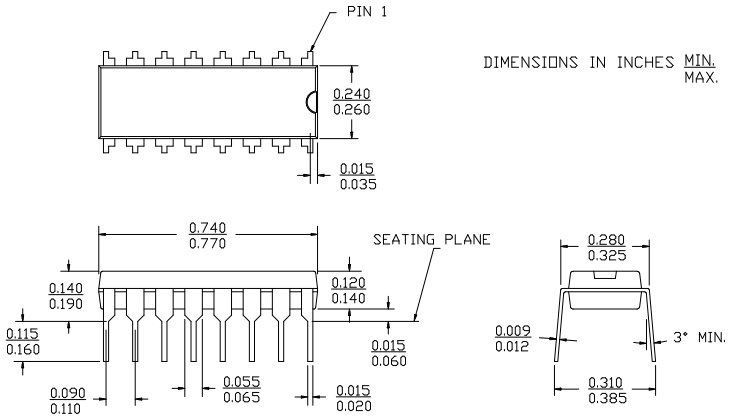
16-Lead (300-Mil) CerDIP D2
MIL−STD−1835 D−2 Config. A



20-Pin Square Leadless Chip Carrier L61
MIL−STD−1835 C−2A

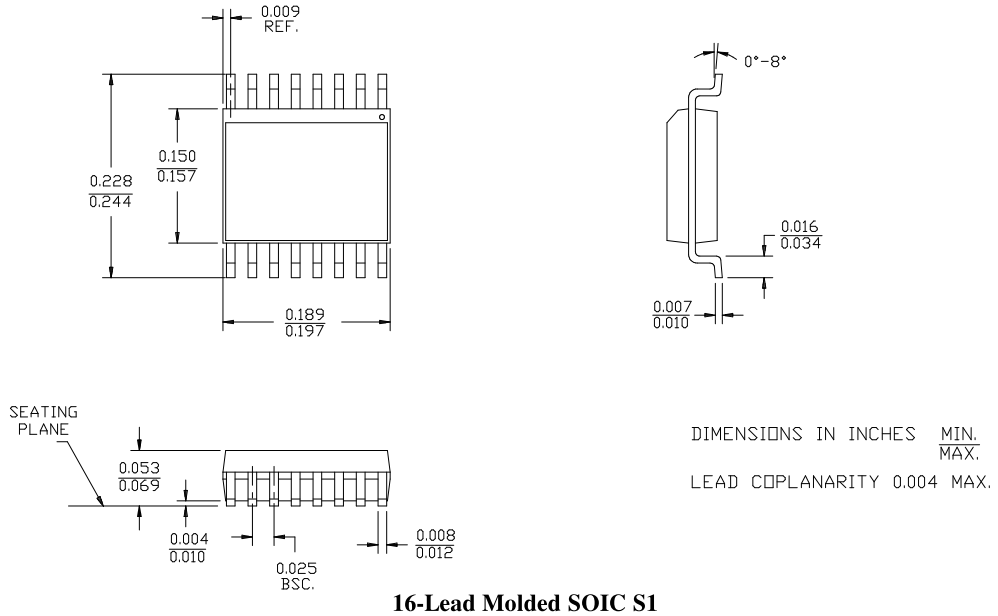


16-Lead (300-Mil) Molded DIP P1



Package Diagrams(continued)

16-Lead Quarter Size Outline Q1



16-Lead Molded SOIC S1