CY74FCT16841T
CY74FCT162841T

20-Bit Latch

Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-C speed at 5.5 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40˚C to +85˚C**
- **V_{CC} = 5V ± 10%**

CY74FCT16841T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25˚C**

CY74FCT162841T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25˚C**

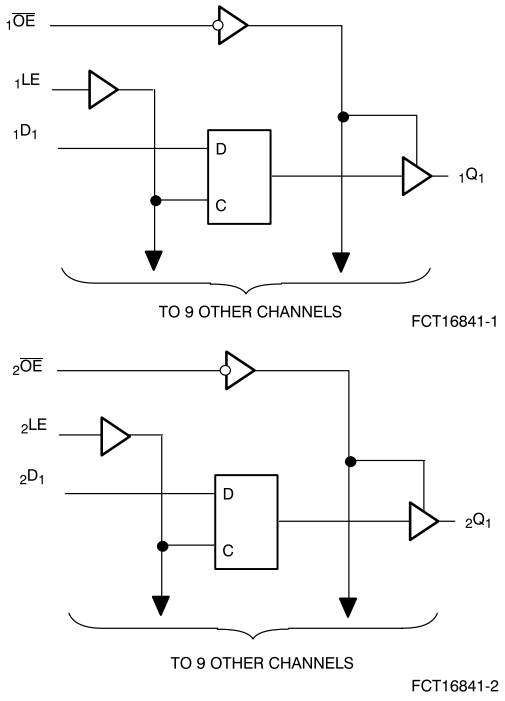
Functional Description

The CY74FCT16841T and CY74FCT162841T are 20-bit D-type latches deisgned for use in bus applications requiring high speed and low power. These devices can be used as two independent 10-bit latches, or as a single 10-bit latch, or as a single 20-bit latch by connecting the Output Enable ($\overline{OE}$) and Latch (LE) inputs. Flow-through pinout and small shrink packaging aid in simplifying board layout. The output buffers are designed with a power-off disable feature to allow live insertion of boards.

The CY74FCT16841T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162841T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162841T is ideal for driving transmission lines.

Logic Block Diagrams

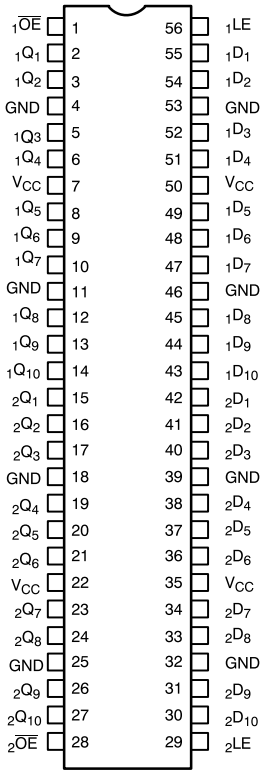


FCT16841-1

FCT16841-2

Pin Configuration

SSOP/TSSOP
Top View



FCT16841-3

Pin Description

Name	Description
D	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O	Three-State Outputs

Function Table[1]

Inputs			Outputs
D	LE	$\overline{OE}$	Q
H	H	L	H
L	H	L	L
X	L	L	Q[2]
X	X	H	Z

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
V_H	Input Hysteresis[6]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[7]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V			±1	µA

Notes:

1. H = HIGH Voltage Level.
   L = LOW Voltage Level.
   X = Don't Care.
   Z = HIGH Impedance.
2. Output level before LE HIGH-to-LOW Transition.
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Output Drive Characteristics for CY74FCT16841T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162841T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
I_{ODL}	Output LOW Current[7]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[7]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[6] (T_A = +25°C, f = 1.0 MHz)

Symbol	Description	Conditions	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	V_{IN}≤0.2V V_{IN}≥V_{CC}−0.2V	—	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.,	V_{IN}=3.4V[8]	—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND LE = V_{CC}	V_{IN}=V_{CC} or V_{IN}=GND	—	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	—	0.9	2.3	
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Twenty Bits Toggling, $\overline{OE}$=GND LE = V_{CC}	V_{IN}=V_{CC} or V_{IN}=GND	—	3.0	5.5[11]	
			V_{IN}=3.4V or V_{IN}=GND	—	8.0	20.5[11]	

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = I_{CC}+$\Delta I_{CC} D_H N_T$+$I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range[12]

Parameter	Description	Condition[13]	74FCT16841AT 74FCT162841AT		74FCT16841BT 74FCT162841BT		74FCT16841CT 74FCT162841CT		Unit	Fig. No.[14]
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Q (LE=HIGH)	C_L=50 pF R_L=500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns	1, 5
		C_L=300 pF[15] R_L=500Ω	1.5	13.0	1.5	13.0	1.5	13.0		
t_{PLH} t_{PHL}	Propagation Delay LE to Q	C_L=50 pF R_L=500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns	1, 5
		C_L=300 pF[15] R_L=500Ω	1.5	16.0	1.5	15.5	1.5	15.0		
t_{PHZ} t_{PZL}	Output Enable Time $\overline{OE}$ to Q	C_L=50 pF R_L=500Ω	1.5	11.5	1.5	8.0	1.5	6.5	ns	1, 7, 8
		C_L=300 pF[15] R_L=500Ω	1.5	23.0	1.5	14.0	1.5	12.0		
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Q	C_L=5 pF[15] R_L=500Ω	1.5	7.0	1.5	6.0	1.5	5.7	ns	1, 7, 8
		C_L=50 pF R_L=500Ω	1.5	8.0	1.5	7.0	1.5	6.0		
t_{SU}	Set-Up Time HIGH or LOW, D to LE	C_L=50 pF R_L=500Ω	2.5	—	2.5	—	2.0	—	ns	9
t_H	Hold Time HIGH or LOW, D to LE		2.5	—	2.5	—	1.5	—	ns	9
t_W	LE Pulse Width HIGH		4.0[16]	—	4.0[16]	—	4.0[16]	—	ns	5
$t_{SK(O)}$	Output Skew[17]		—	0.5	—	0.5	—	0.5	ns	—

Notes:
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See test circuit and waveform.
14. See "Parameter Measurement Information" in the General Information section.
15. These conditions are guaranteed but not tested.
16. These limits are guaranteed but not tested.
17. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Ordering Information for CY74FCT16841T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.5	CY74FCT16841CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16841CTPVC	O56	56-Lead (300-Mil) SSOP	
6.5	CY74FCT16841ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16841ATPVC	O56	56-Lead (300-Mil) SSOP	
9.0	CY74FCT16841TPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16841TPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162841T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.5	CY74FCT162841CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162841CTPVC	O56	56-Lead (300-Mil) SSOP	
6.5	CY74FCT162841ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162841ATPVC	O56	56-Lead (300-Mil) SSOP	
9.0	CY74FCT162841TPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162841TPVC	O56	56-Lead (300-Mil) SSOP	

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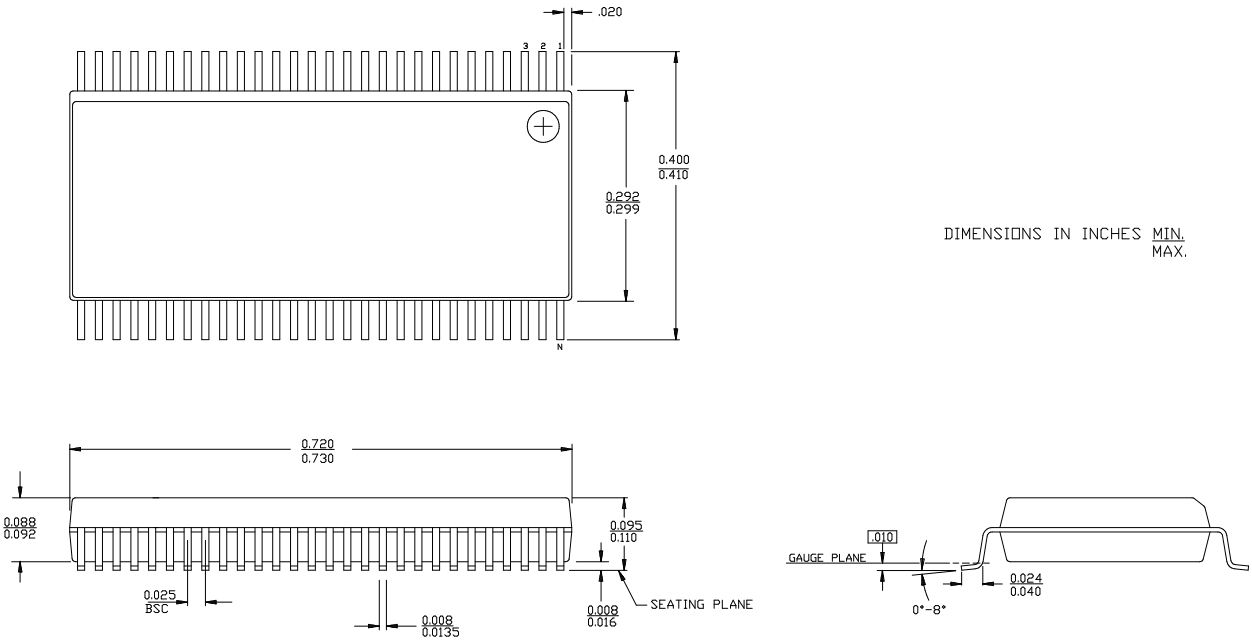
Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56