CY74FCT16952T
CY74FCT162952T
CY74FCT162H952T

16-Bit Registered Transceiver

Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-C speed at 6.3 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40˚C to +85˚C**
- **V_{CC} = 5V ± 10%**

CY74FCT16952T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25˚C**

CY74FCT162952T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25˚C**

CY74FCT162H952T Features:

- **Bus hold retains last active state**
- **Eliminates the need for external pull-up or pull-down resistors**

Functional Description

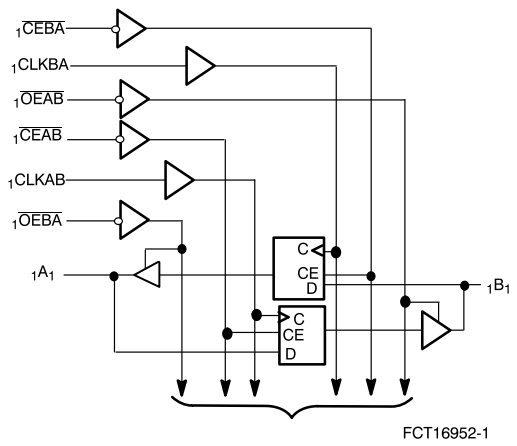
These 16-bit registered transceivers are high-speed, low-power devices. 16-bit operation is achieved by connecting the control lines of the two 8-bit registered transceivers together. For data flow from bus A-to-B, $\overline{CEAB}$ must be LOW to allow data to be stored when CLKAB transitions from LOW-to-HIGH. The stored data will be present on the output when $\overline{OEAB}$ is LOW. Control of data from B-to-A is similar and is controlled by using the $\overline{CEBA}$, CLKBA, and $\overline{OEBA}$ inputs. The output buffers are designed with a power-off disable feature to allow for live insertion of boards.

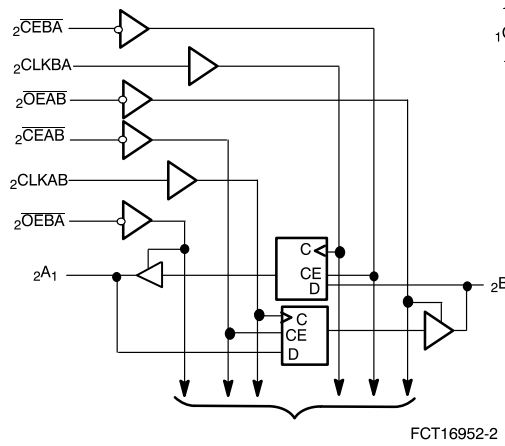
The CY74FCT16952T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162952T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162952T is ideal for driving transmission lines.

The CY74FCT162H952T is a 24-mA balanced output part that has "bus hold" on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

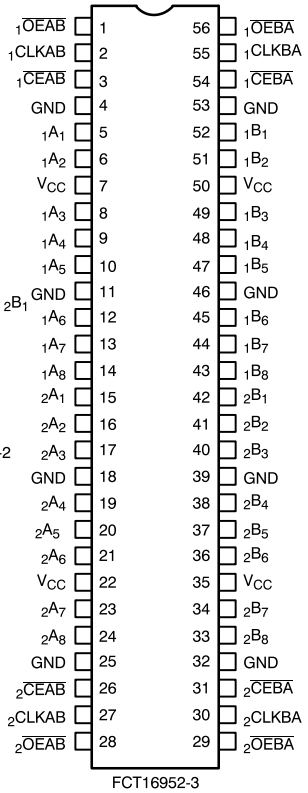
Logic Block Diagrams





Pin Configuration

SSOP/TSSOP
Top View



Pin Description

Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Clock Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Clock Enable Input (Active LOW)
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A	A-to-B Data Inputs or B-to-A Three-State Outputs[1]
B	B-to-A Data Inputs or A-to-B Three-State Outputs[1]

Function Table[2, 3]

For A-to-B (Symmetric with B-to-A)

Inputs				Outputs
$\overline{CEAB}$	CLKAB	$\overline{OEAB}$	A	B
H	X	L	X	B[4]
X	L	L	X	B[4]
L	⌐	L	L	L
L	⌐	L	H	H
X	X	H	X	Z

Maximum Ratings[5, 6]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l −55°C to +125°C

Ambient Temperature with Power Applied ..... Com'l −55°C to +125°C

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... −60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

Notes:

1. On the CY74FCT162H952T these pins have bus hold.
2. A-to-B data flow is shown: B-to-A data flow is similar but uses, $\overline{CEBA}$, CLKBA, and $\overline{OEBA}$.
3. H = HIGH Voltage Level.
   L = LOW Voltage Level.
   X = Don't Care.
   ⌐ = LOW-to-HIGH Transition.
   Z = HIGH Impedance.
4. Level of B before the indicated steady-state input conditions were established.
5. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
6. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Electrical Characteristics Over the Operating Range

Parameter	Description		Test Conditions		Min.	Typ.[7]	Max.	Unit
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_H	Input Hysteresis[8]					100		mV
V_{IK}	Input Clamp Diode Voltage		V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_{IH}	Input HIGH Current	Standard	V_{CC}=Max., V_I=V_{CC}				±1	µA
		Bus Hold					±100	
I_{IL}	Input LOW Current	Standard	V_{CC}=Max., V_I=GND				±1	µA
		Bus Hold					±100	µA
I_{BBH} I_{BBL}	Bus Hold Sustain Current on Bus Hold Input[9]		V_{CC}=Min.	V_I=2.0V	−50			µA
				V_I=0.8V	+50			
I_{BHHO} I_{BHLO}	Bus Hold Overdrive Current on Bus Hold Input[9]		V_{CC}=Max., V_I=1.5V				TBD	mA
I_{OZH}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=2.7V				±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=0.5V				±1	µA
I_{OS}	Short Circuit Current[10]		V_{CC}=Max., V_{OUT}=GND		−80	−140	−200	mA
I_O	Output Drive Current[10]		V_{CC}=Max., V_{OUT}=2.5V		−50		−180	mA
I_{OFF}	Power-Off Disable		V_{CC}=0V, V_{OUT}≤4.5V				±1	µA

Output Drive Characteristics for CY74FCT16952T

Parameter	Description	Test Conditions	Min.	Typ.[7]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162952T, CY74FCT162H952T

Parameter	Description	Test Conditions	Min.	Typ.[7]	Max.	Unit
I_{ODL}	Output LOW Current[10]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[10]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[8] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[7]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Notes:

7. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
8. This parameter is guaranteed but not tested.
9. Pins with bus hold are described in the Pin Description.
10. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions[11]		Typ.[7]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \le 0.2V$ $V_{IN} \ge V_{CC}-0.2V$	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[12]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[13]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OEAB}$ or $\overline{OEBA}$=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	75	120	µA/ MHz
I_C	Total Power Supply Current[14]	V_{CC}=Max., F_1=5 MHz, F_0 = 10 MHz (CLKAB) $\overline{OEAB}$ = $\overline{CEAB}$ = GND $\overline{OEBA}$ = V_{CC} 50% Duty Cycle, Outputs Open, One Bit Toggling	$V_{IN}=V_{CC}$ or V_{IN}=GND	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	1.3	3.2	
		V_{CC}=Max., f_0=10 MHz (CLKAB) f_1=2.5 MHz, $\overline{OEAB}$ = $\overline{CEAB}$ = GND $\overline{OEBA}$ = V_{CC} 50% Duty Cycle, Outputs Open, Sixteen Bit Toggling	$V_{IN}=V_{CC}$ or V_{IN}=GND	3.8	6.5[15]	
			V_{IN}=3.4V or V_{IN}=GND	8.3	20.0[15]	

Notes:

11. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
12. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
13. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
14. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
15. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range[16]

Parameter	Description	Conditions[17]	74FCT16952AT 74FCT162952AT 74FCT162H952AT		74FCT16952BT 74FCT162952BT 74FCT162H952BT		74FCT16952CT 74FCT162952CT 74FCT162H952CT		Unit	Fig. No.[18]
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay CLKAB, CLKBA to B, A	C_L=50 pF R_L=500Ω	2.0	10.0	2.0	7.5	2.0	6.3	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$, $\overline{OEAB}$ to A, B		1.5	10.5	1.5	8.0	1.5	7.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$, $\overline{OEAB}$ to A, B		1.5	10.0	1.5	7.5	1.5	6.5	ns	1, 7, 8
t_{SU}	Set-Up Time, HIGH or LOW A, B to CLKAB, CLKBA		2.5	—	2.5	—	2.5	—	ns	4
t_H	Hold Time, HIGH or LOW A, B to CLKAB, CLKBA		2.0	—	1.5	—	1.5	—	ns	4
t_{SU}	Set-Up Time, HIGH or LOW $\overline{CEAB}$, $\overline{CEBA}$ to CLKAB, CLKBA		3.0	—	3.0	—	3.0	—	ns	4
t_H	Hold Time, HIGH or LOW $\overline{CEAB}$, $\overline{CEBA}$ to CLKAB, CLKBA		2.0	—	2.0	—	2.0	—	ns	4
t_W	Pulse Width HIGH or LOW CLKAB or CLKBA[19]		3.0	—	3.0	—	3.0	—	ns	5
$t_{SK(O)}$	Output Skew[20]		—	0.5	—	0.5	—	0.5	ns	—

Notes:
16. Minimum limits are guaranteed but not tested on Propagation Delays.
17 See test circuits and waveforms.
18. See “Parameter Measurement Information” in the General Information section.
19. This parameter is guaranteed but not tested.
20. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Ordering Information CY74FCT16952

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT16952CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16952CTPVC	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT16952BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16952BTPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT16952ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16952ATPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162952

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT162952CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162952CTPVC	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT162952BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162952BTPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT162952ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162952ATPVC	O56	56-Lead (300-Mil) SSOP	

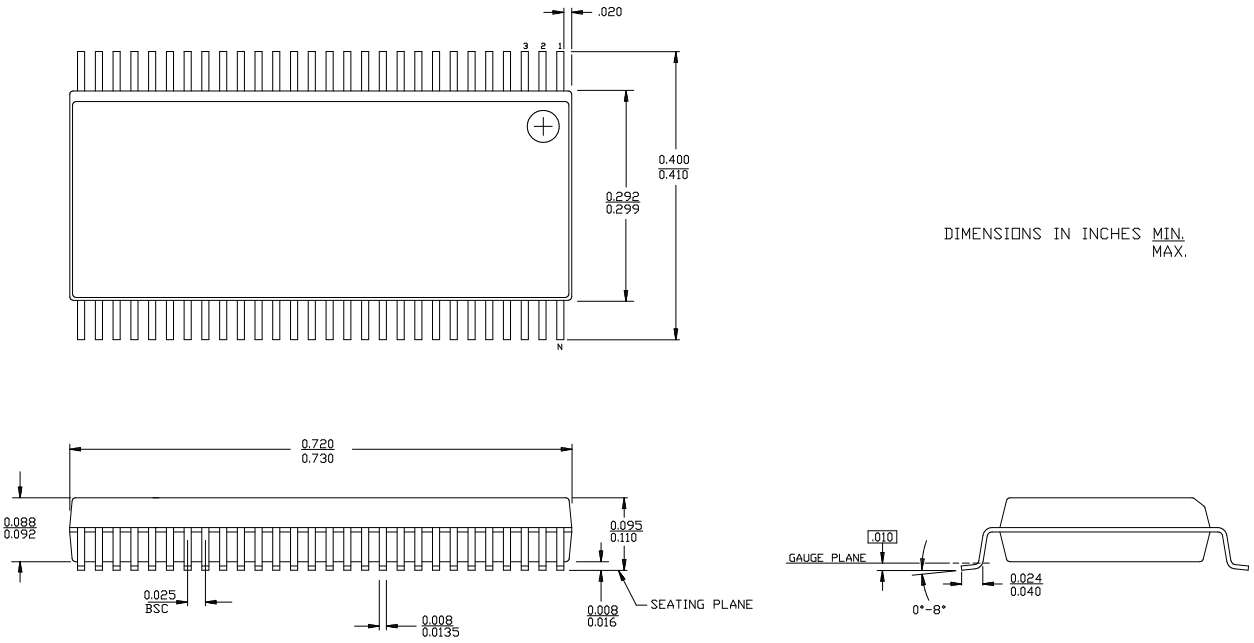
Ordering Information CY74FCT162H952

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT162H952CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H952CTPVC	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT162H952BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H952BTPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT162H952ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H952ATPVC	O56	56-Lead (300-Mil) SSOP	

Document #: 38−00392

Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56