



CY54/74FCT374T CY54/74FCT574T

8-Bit Registers

Features

- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 5.2 ns max. (Com'l)
FCT-A speed at 6.5 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V

- Sink Current 64 mA (Com'l),
32 mA (Mil)
- Source Current 32 mA (Com'l),
12 mA (Mil)

- Edge-triggered D-type inputs
- 250 MHz typical toggle rate

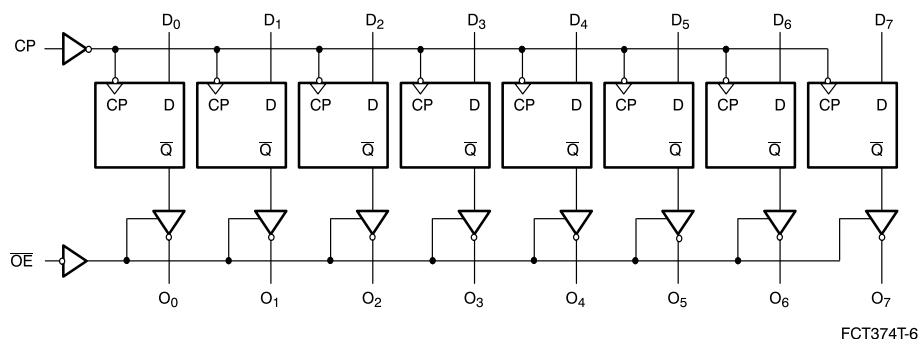
Functional Description

The FCT374T and FCT574T are high-speed low-power octal D-type flip-flops featuring separate D-type inputs for each flip-flop. Both devices have three-state outputs for bus oriented applications. A buffered clock (CP) and output enable (\overline{OE}) are common to all flip-flops. The FCT574T is identical to FCT374T except

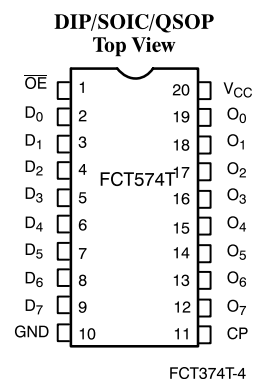
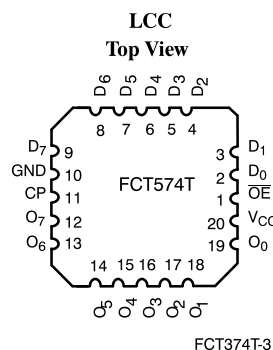
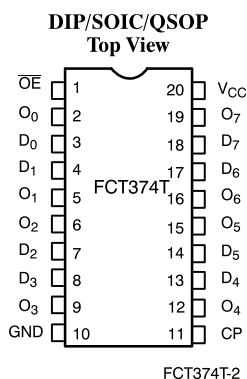
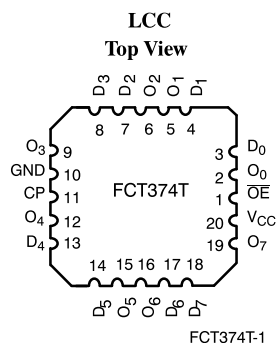
for flow-through pinout to simplify board design. The eight flip-flops contained in the FCT374T and FCT574T will store the state of their individual D inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. When \overline{OE} is LOW, the contents of the eight flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs will be in the high-impedence state. The state of output enable does not affect the state of the flip-flops.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

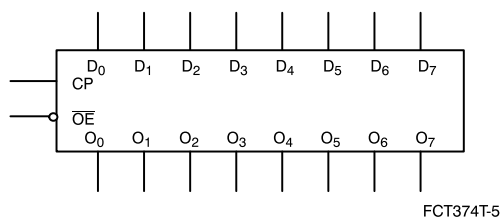
Logic Block Diagram



Pin Configurations



Logic Symbol



Function Table^[1]

Inputs			Outputs
D	CP	\overline{OE}	O
H	\downarrow	L	H
L	\downarrow	L	L
X	X	H	Z

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Ambient Temperature with
 Power Applied -65°C to $+135^{\circ}\text{C}$
 Supply Voltage to Ground Potential -0.5V to $+7.0\text{V}$
 DC Input Voltage -0.5V to $+7.0\text{V}$
 DC Output Voltage -0.5V to $+7.0\text{V}$
 DC Output Current (Maximum Sink Current/Pin) 120 mA
 Power Dissipation 0.5W

Static Discharge Voltage $>2001\text{V}$
 (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 5\%$
Commercial	T, AT	-40°C to $+85^{\circ}\text{C}$	$5\text{V} \pm 5\%$
Military ^[4]	All	-55°C to $+125^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC}=\text{Min.}, I_{OH}=-32\text{ mA}$	Com'l	2.0			V
		$V_{CC}=\text{Min.}, I_{OH}=-15\text{ mA}$	Com'l	2.4	3.3		V
		$V_{CC}=\text{Min.}, I_{OH}=-12\text{ mA}$	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	$V_{CC}=\text{Min.}, I_{OL}=64\text{ mA}$	Com'l		0.3	0.55	V
		$V_{CC}=\text{Min.}, I_{OL}=32\text{ mA}$	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis ^[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	$V_{CC}=\text{Min.}, I_{IN}=-18\text{ mA}$			-0.7	-1.2	V
I_I	Input HIGH Current	$V_{CC}=\text{Max.}, V_{IN}=V_{CC}$				5	μA
I_{IH}	Input HIGH Current	$V_{CC}=\text{Max.}, V_{IN}=2.7\text{V}$				± 1	μA
I_{IL}	Input LOW Current	$V_{CC}=\text{Max.}, V_{IN}=0.5\text{V}$				± 1	μA
I_{OZH}	Off State HIGH-Level Output Current	$V_{CC} = \text{Max.}, V_{OUT} = 2.7\text{V}$				10	μA
I_{OZL}	Off State LOW-Level Output Current	$V_{CC} = \text{Max.}, V_{OUT} = 0.5\text{V}$				-10	μA
I_{OS}	Output Short Circuit Current ^[7]	$V_{CC}=\text{Max.}, V_{OUT}=0.0\text{V}$		-60	-120	-225	mA
I_{OFF}	Power-Off Disable	$V_{CC}=0\text{V}, V_{OUT}=4.5\text{V}$				± 1	μA

Notes:

- H = HIGH Voltage Level.
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance
 \downarrow = LOW-to-HIGH clock transition
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at $V_{CC}=5.0\text{V}$, $T_A=+25^{\circ}\text{C}$ ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameters tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max., V _{IN} =3.4V, ^[8] f ₁ =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Bit Toggling, 50% Duty Cycle, Outputs Open, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.06	0.12	mA/ MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =5 MHz, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =5 MHz, OE=GND, V _{IN} =3.4V or V _{IN} =GND	1.2	3.4	mA
		V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, OE=GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	1.6	3.2 ^[11]	mA
		V _{CC} =Max., f ₀ =10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, OE=GND, V _{IN} =3.4V or V _{IN} =GND	3.9	12.2 ^[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.

9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)

f₀ = Clock frequency for registered devices, otherwise zero

f₁ = Input signal frequency

N₁ = Number of inputs changing at f₁

- All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics^[12] Over the Operating Range

Parameter	Description	FCT374T/FCT574T				FCT374AT/FCT574AT				Unit	Fig. No. ^[14]
		Military		Commercial		Military		Commercial			
		Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Clock to Output	2.0	11.0	2.0	10.0	2.0	7.2	2.0	6.5	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	14.0	1.5	12.5	1.5	7.5	1.5	6.5	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	8.0	1.5	8.0	1.5	6.5	1.5	5.5	ns	1, 7, 8
t _S	Set-Up Time HIGH or LOW D to CP	2.0		2.0		2.0		2.0		ns	4
t _H	Hold Time HIGH or LOW D to CP	1.5		1.5		1.5		1.5		ns	4
t _W	Clock Pulse Width ^[15] HIGH or LOW	7.0		7.0		6.0		5.0		ns	5

Parameter	Description	FCT374CT/FCT574CT				FCT374DT/ FCT574DT		Unit	Fig. No. ^[14]
		Military		Commercial		Commercial			
		Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Clock to Output	2.0	6.2	2.0	5.2	2.0	4.2	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	6.2	1.5	5.5	1.5	4.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.7	1.5	5.0	1.5	4.0	ns	1, 7, 8
t _S	Set-Up Time, HIGH or LOW D to CP	2.0		2.0		2.0		ns	4
t _H	Hold Time, HIGH or LOW D to CP	1.5		1.5		1.5		ns	4
t _W	Clock Pulse Width ^[15] HIGH or LOW	6.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

12. AC Characteristics guaranteed with C_L = 50 pF as shown in Figure 1 of the "Parameter Measurement Information" in the General Information section.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. See "Parameter Measurement Information" in the General Information section.
15. With one data channel toggling, t_W(L) = t_W(H) = 4.0 ns and t_r = t_f = 1.0 ns.



Ordering Information—FCT374T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT374DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT374DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.2	CY74FCT374CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT374CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT374CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
6.2	CY54FCT374CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT374CTLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT374ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT374ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT374ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.2	CY54FCT374ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT374ATLMB	L61	20-Pin Square Leadless Chip Carrier	
10.0	CY74FCT374TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT374TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT374TSOC	S5	20-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT374TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT374TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information—FCT574T

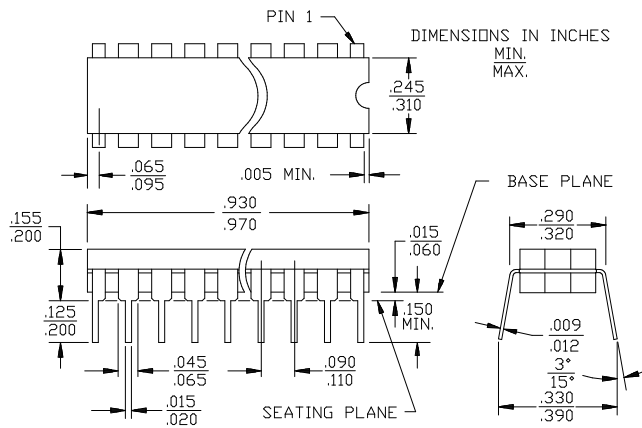
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT574DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT574DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.2	CY74FCT574CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT574CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT574CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
6.2	CY54FCT574CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT574CTLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT574ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT574ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT574ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.2	CY54FCT574ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT574ATLMB	L61	20-Pin Square Leadless Chip Carrier	
10.0	CY74FCT574TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT574TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT574TSOC	S5	20-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT574TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT574TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

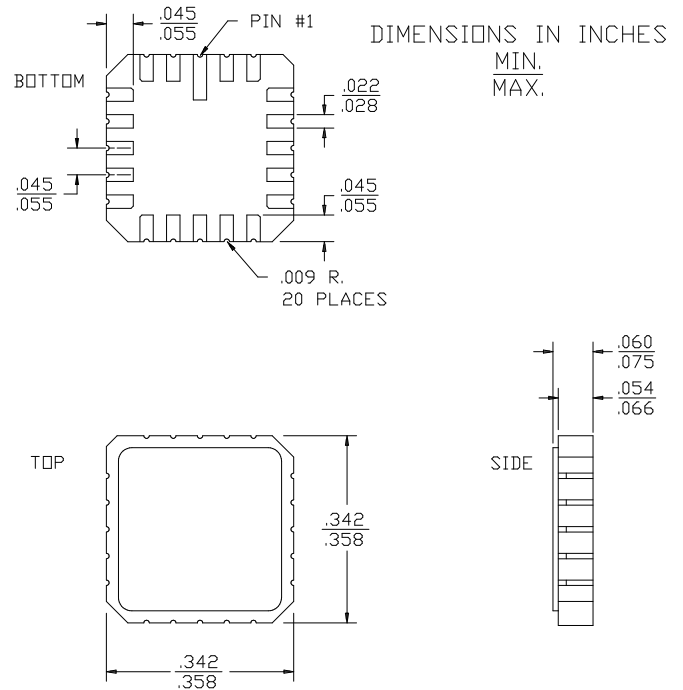
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Package Diagrams

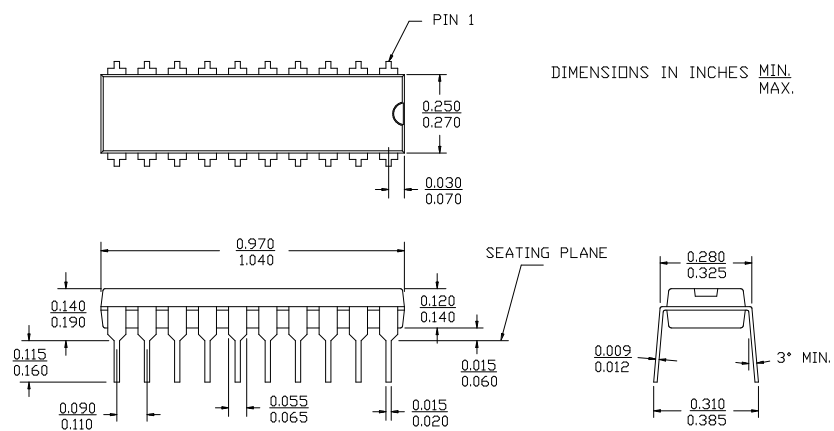
20-Lead (300-Mil) CerDIP D6
MIL-STD-1835 D-8 Config. A

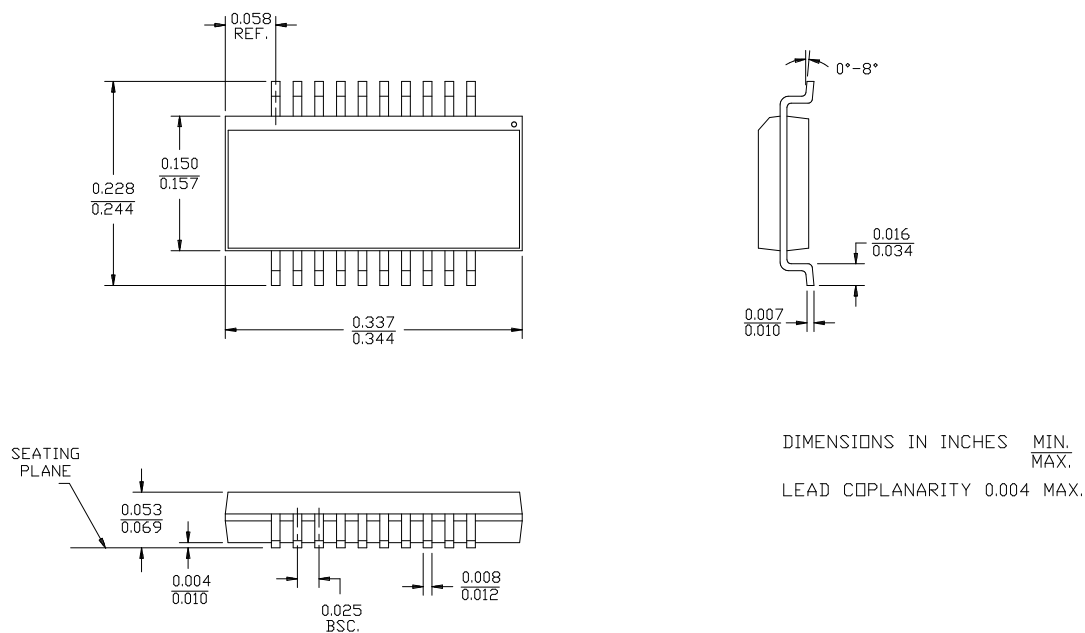


20-Pin Square Leadless Chip Carrier L61
MIL-STD-1835 C-2A



20-Lead (300-Mil) Molded DIP P5



Package Diagrams (continued)
20-Lead Quarter Size Outline Q5

20-Lead (300-Mil) Molded SOIC S5
