CY54/74FCT540T
CY54/74FCT541T

8-Bit Buffers/Line Drivers

Features

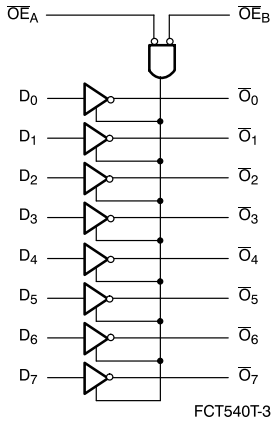
- **Function, pinout and drive compatible with FCT and F logic**
- **FCT-C speed at 4.1 ns max. (Com'l) FCT-A speed at 4.8 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink current 64 mA (Com'l), 48 mA (Mil)**
  Source current 32 mA (Com'l), 12 mA (Mil)
- **Three-state outputs**

Functional Description

The FCT540T inverting buffer/line driver and the FCT541T non-inverting buffer/line driver are designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. The devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

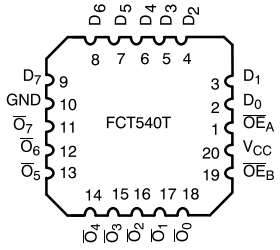
Logic Block Diagram—FCT540T



FCT540T-3

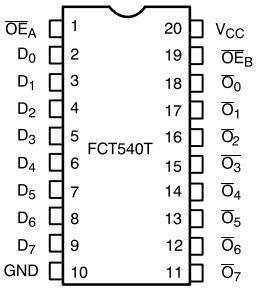
Pin Configurations

LCC
Top View



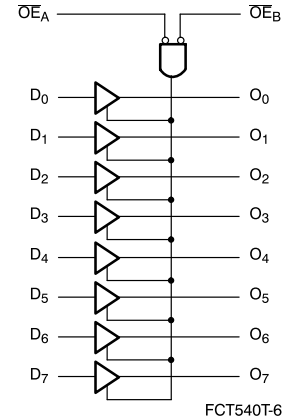
FCT540T-1

DIP/SOIC/QSOP
Top View



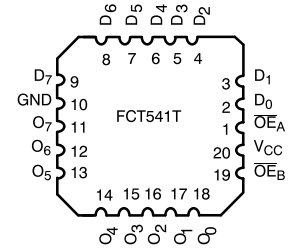
FCT540T-2

Logic Block Diagram—FCT541T



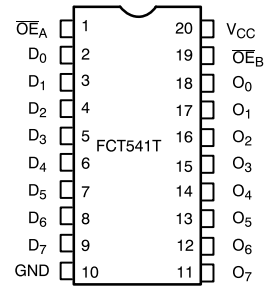
FCT540T-6

LCC
Top View



FCT540T-4

DIP/SOIC/QSOP
Top View



FCT540T-5

Function Table FCT540T[1]

Inputs			Output
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	H
L	L	H	L
H	H	X	Z

Function Table FCT541T[1]

Inputs			Output
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	L
L	L	H	H
H	H	X	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[4]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=48 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC}=Max., V_{OUT}=2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC}= Max., V_{OUT}=0.5V				−10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max,. V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Notes:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedence
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parametric tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Test Conditions	Typ. [5]	Max.	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10 MHz, $\overline{OE}_A$=$\overline{OE}_B$=GND, or $\overline{OE}_A$=GND, OE_B=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_A$=$\overline{OE}_B$=GND, or $\overline{OE}_A$=GND, OE_B=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=10 MHz, $\overline{OE}_A$=$\overline{OE}_B$=GND, or $\overline{OE}_A$=GND, OE_B=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}_A$=$\overline{OE}_B$=GND, or $\overline{OE}_A$=GND, OE_B=V_{CC}, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	1.3	2.6[11]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}_A$=$\overline{OE}_B$=GND, or $\overline{OE}_A$=GND, OE_B=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	3.3	10.6[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT540T/FCT541T				FCT540AT/FCT541AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output (FCT540)	1.5	9.5	1.5	8.5	1.5	5.1	1.5	4.8	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output (FCT541)	1.5	9.0	1.5	8.0	1.5	5.1	1.5	4.8	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.5	1.5	10.0	1.5	6.5	1.5	6.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	10.0	1.5	9.5	1.5	5.9	1.5	5.6	ns	1, 7, 8

Parameter	Description	FCT540CT/FCT541CT				FCT540DT/ FCT541DT		Unit	Fig. No.[13]
		Military		Commercial		Commercial			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output (FCT540)	1.5	4.7	1.5	4.1	1.5	3.8	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output (FCT541)	1.5	4.6	1.5	4.1	1.5	3.8	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.5	1.5	5.8	1.5	5.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.7	1.5	5.2	1.5	5.0	ns	1, 7, 8

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See “Parameter Measurement Information” in the General Information section.

Ordering Information—FCT540T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT540DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT540DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.1	CY74FCT540CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT540CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT540CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.7	CY54FCT540CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT540CTLMB	L61	20-Pin Square Leadless Chip Carrier	
4.8	CY74FCT540ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT540ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT540ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT540ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT540ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.5	CY74FCT540TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT540TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT540TSOC	S5	20-Lead (300-Mil) Molded SOIC	
9.5	CY54FCT540TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT540TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information—FCT541T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT541DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT541DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.1	CY74FCT541CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT541CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT541CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.6	CY54FCT541CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT541CTLMB	L61	20-Pin Square Leadless Chip Carrier	
4.8	CY74FCT541ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT541ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT541ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT541ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT541ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT541TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT541TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT541TSOC	S5	20-Lead (300-Mil) Molded SOIC	
9.0	CY54FCT541TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT541TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

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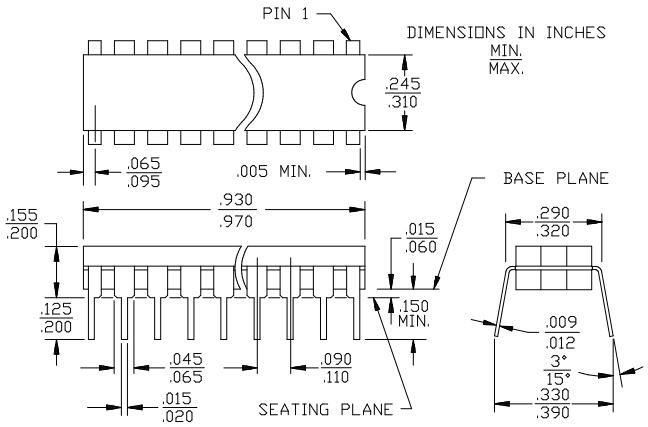
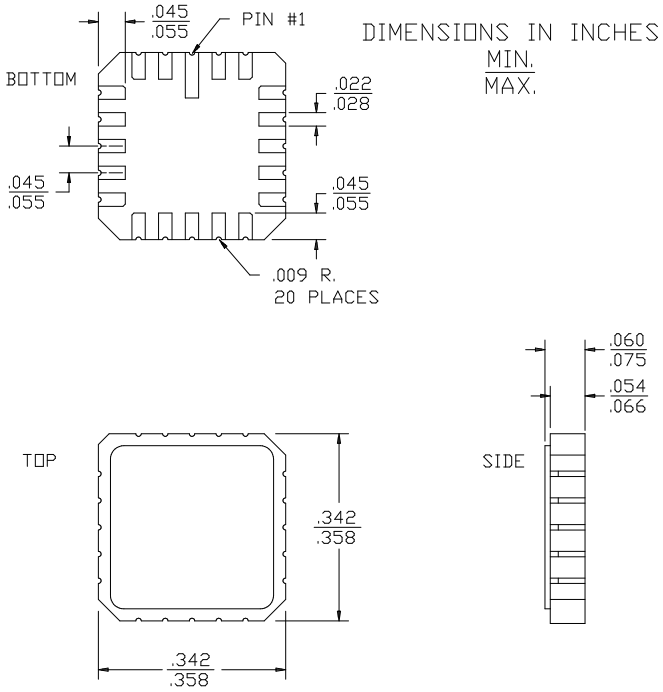
Package Diagrams

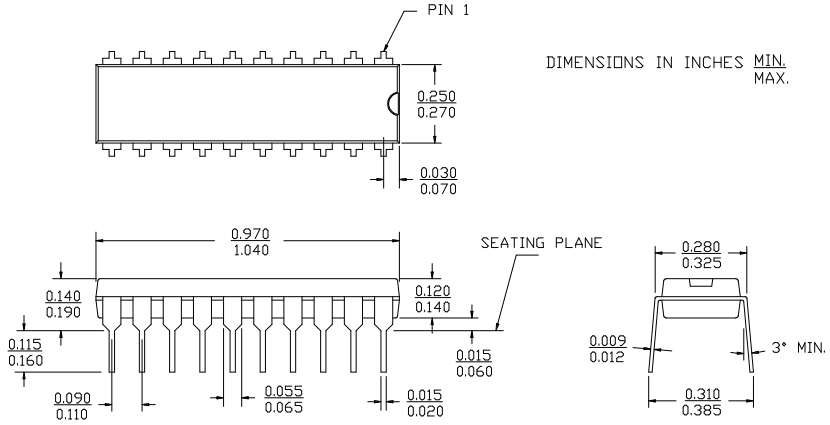
20-Lead (300-Mil) CerDIP D6
MIL−STD−1835 D−8 Config. A



20-Pin Square Leadless Chip Carrier L61
MIL−STD−1835 C−2A

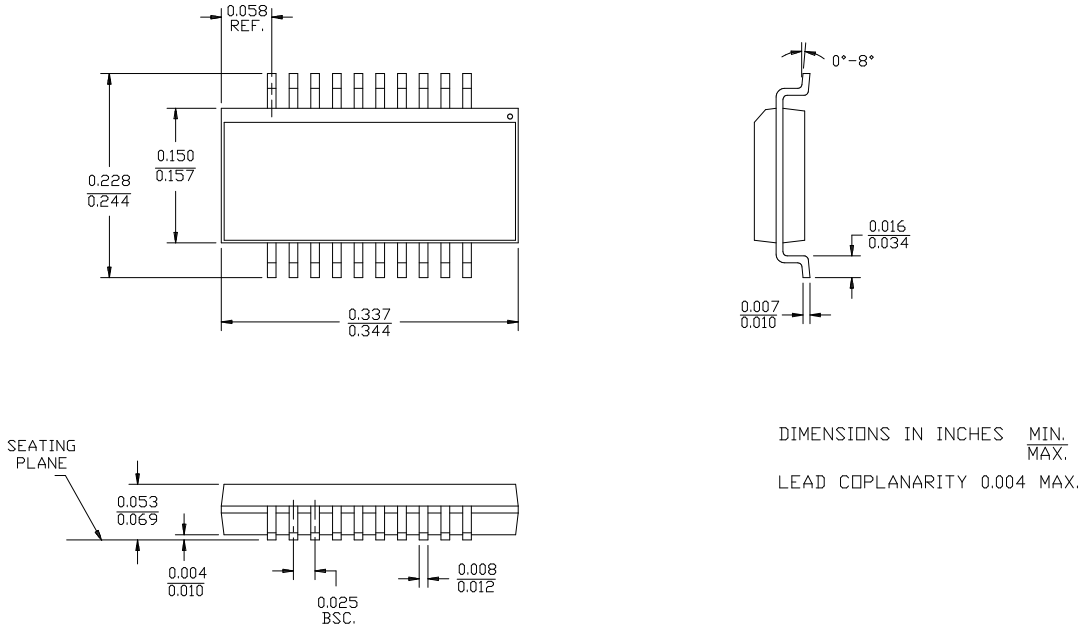


20-Lead (300-Mil) Molded DIP P5



Package Diagrams (continued)

20-Lead Quarter Size Outline Q5



20-Lead (300-Mil) Molded SOIC S5