# CY54/74FCT646T
# CY54/74FCT648T

## 8-Bit Registered Transceivers

### Features

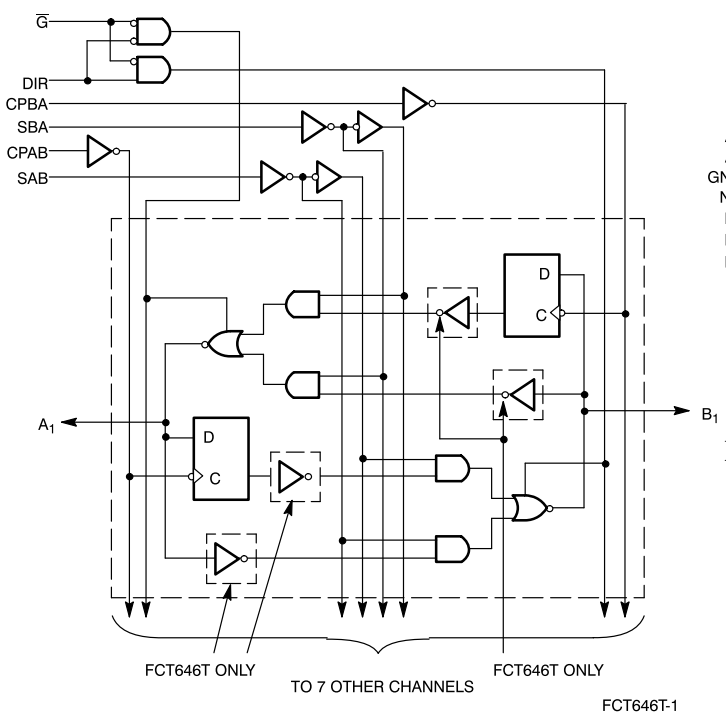
- **Function, pinout and drive compatible with FCT and F logic**
- **FCT-C speed at 5.4 ns max. (Com'l) FCT-A speed at 6.3 ns max. (Com'l)**
- **Reduced $V_{OH}$ (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Sink current 64 mA (Com'l), 48 mA (Mil)**
  **Source current 32 mA (Com'l), 12 mA (Mil)**
- **Independent register for A and B buses**
- **Three-state output**

### Functional Description

The FCT646T and FCT648T consist of a bus transceiver circuit with three-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Enable Control $\overline{G}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (enable Control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

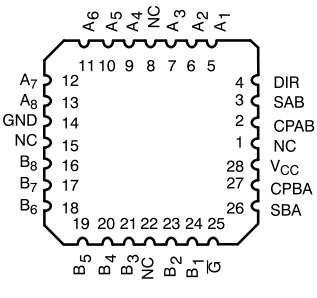
### Function Block Diagrams




FCT646T-1

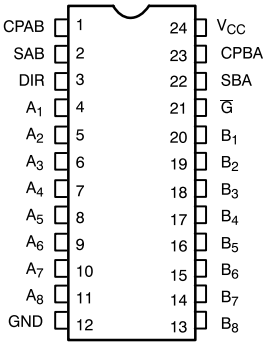
### Pin Configurations

**LCC/PLCC Top View**



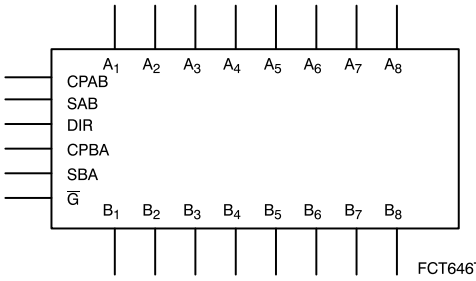

FCT646T-2

**DIP Top View**




FCT646T-3

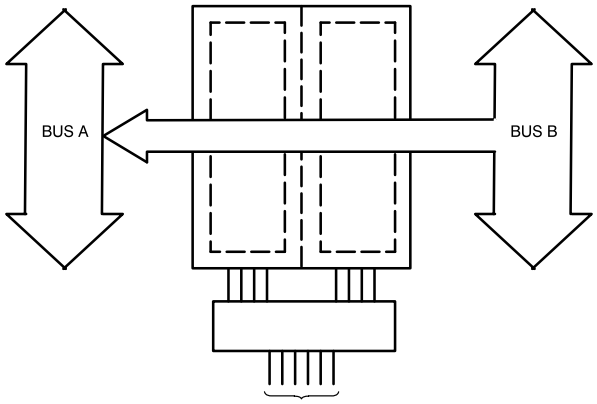
### Logic Block Diagram



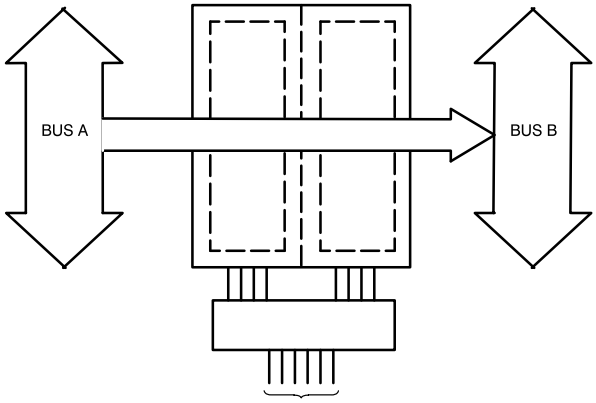

FCT646T-4

### Pin Description

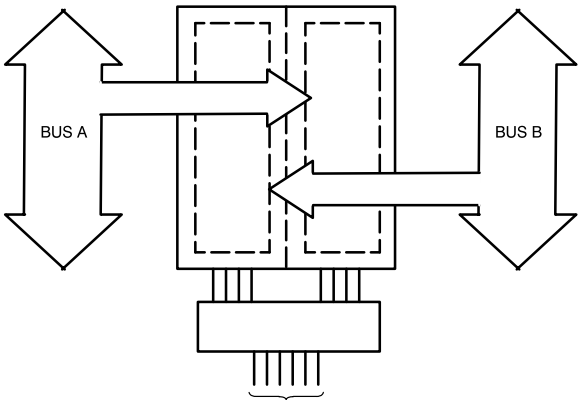
| Name | Description |
|---|---|
| A | Data Register A Inputs, Data Register B Outputs |
| B | Data Register B Inputs, Data Register A Outputs |
| CPAB, CPBA | Clock Pulse Inputs |
| SAB, SBA | Output Data Source Select Inputs |
| DIR, $\overline{G}$ | Output Enable Inputs |



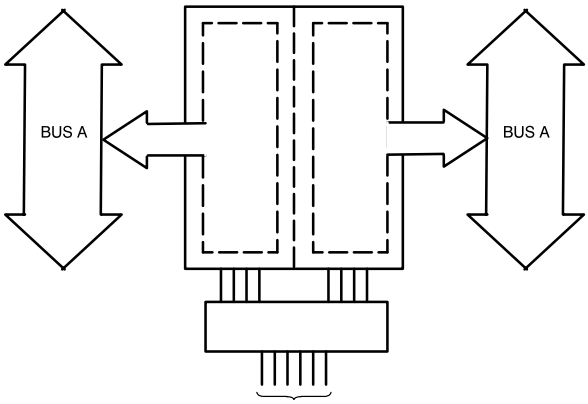

Real-Time Transfer
Bus B to Bus A




Real-Time Transfer
Bus A to Bus B




Storage from
A and/or B




Transfer Stored Data
to A and/or B

## Function Table[2]

| Inputs | | | | | | Data I/O[3] | | Operation or Function | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{G}$ | DIR | CPAB | CPBA | SAB | SBA | $A_1$ thru $A_8$ | $B_1$ thru $B_8$ | FCT646T | FCT648T |
| H | X | H or L | H or L | X | X | Input | Input | Isolation | Isolation |
| H | X | ↓ | ↓ | X | X | | | Store A and B Data | Store A and B Data |
| L | L | X | X | X | L | Output | Input | Real Time B Data to A Bus | Real Time $\overline{B}$ Data to A Bus |
| L | L | X | H or L | X | H | | | Stored B Data to A Bus | Stored $\overline{B}$ Data to A Bus |
| L | H | X | X | L | X | Input | Output | Real Time A Data to B Bus | Real Time $\overline{A}$ Data to B Bus |
| L | H | H or L | X | H | X | | | Stored A Data to B Bus | Stored $\overline{A}$ Data to B Bus |

**Notes:**
1. Cannot transfer data to A bus and B bus simultaneously.
2. H = HIGH Voltage Level, L = LOW Voltage Level, ↓ = LOW-to-HIGH Transition, X = Don't Care.
3. The data output functions may be enabled or disabled by various signals at the G or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

## Maximum Ratings[4, 5]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation ..... 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

## Operating Range

| Range | Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|---|
| Commercial | CT | 0°C to +70°C | 5V ± 5% |
| Commercial | T, AT | −40°C to +85°C | 5V ± 5% |
| Military[6] | All | −55°C to +125°C | 5V ± 10% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | Min. | Typ.[7] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$=Min., $I_{OH}$=−32 mA | Com'l | 2.0 | | | V |
| | | $V_{CC}$=Min., $I_{OH}$=−15 mA | Com'l | 2.4 | 3.3 | | V |
| | | $V_{CC}$=Min., $I_{OH}$=−12 mA | Mil | 2.4 | 3.3 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$=Min., $I_{OL}$=64 mA | Com'l | | 0.3 | 0.55 | V |
| | | $V_{CC}$=Min., $I_{OL}$=48 mA | Mil | | 0.3 | 0.55 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | | | 0.8 | V |
| $V_H$ | Hysteresis[8] | All inputs | | | 0.2 | | V |
| $V_{IK}$ | Input Clamp Diode Voltage | $V_{CC}$=Min., $I_{IN}$=−18 mA | | | −0.7 | −1.2 | V |
| $I_I$ | Input HIGH Current | $V_{CC}$=Max., $V_{IN}$=$V_{CC}$ | | | | 5 | µA |
| $I_{IH}$ | Input HIGH Current[8] | $V_{CC}$=Max., $V_{IN}$=2.7V | | | | ±1 | µA |
| $I_{IL}$ | Input LOW Current[8] | $V_{CC}$=Max., $V_{IN}$=0.5V | | | | ±1 | µA |
| $I_{OS}$ | Output Short Circuit Current[9] | $V_{CC}$=Max., $V_{OUT}$=0.0V | | −60 | −120 | −225 | mA |
| $I_{OFF}$ | Power-Off Disable | $V_{CC}$=0V, $V_{OUT}$=4.5V | | | | ±1 | µA |

## Capacitance[8]

| Parameter | Description | Typ.[7] | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 6 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | 8 | 12 | pF |

**Notes:**

4. Unless otherwise noted, these limits are over the operating free-air temperature range.
5. Unused inputs must always be connected to an appropriate logic voltage level, preferably either $V_{CC}$ or ground.
6. $T_A$ is the "instant on" case temperature.
7. Typical values are at $V_{CC}$=5.0V, $T_A$=+25°C ambient.
8. This parameter is guaranteed but not tested.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.

## Power Supply Characteristics

| Parameter | Description | Test Conditions | Typ.[7] | Max. | Unit |
|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$ | 0.1 | 0.2 | mA |
| $\Delta I_{CC}$ | Quiescent Power Supply Current (TTL inputs HIGH) | $V_{CC}$=Max., $V_{IN}$=3.4V,[10] $f_1$=0, Outputs Open | 0.5 | 2.0 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[11] | $V_{CC}$=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$ | 0.06 | 0.12 | mA/ MHz |
| $I_C$ | Total Power Supply Current[12] | $V_{CC}$=Max., $f_0$=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1$=5 MHz, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$ | 0.7 | 1.4 | mA |
| | | $V_{CC}$=Max., $f_0$=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1$=5 MHz, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, $V_{IN}$=3.4V or $V_{IN}$=GND | 1.2 | 3.4 | mA |
| | | $V_{CC}$=Max., $f_0$=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1$=5 MHz, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$ | 2.8 | 5.6[13] | mA |
| | | $V_{CC}$=Max., $f_0$=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1$=5 MHz, $\overline{G}$=DIR=GND, GAB=$\overline{GBA}$=GND, $V_{IN}$=3.4V or $V_{IN}$=GND | 5.1 | 14.6[13] | mA |

**Notes:**

10. Per TTL driven input ($V_{IN}$=3.4V); all other inputs at $V_{CC}$ or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. $I_C$ = $I_{QUIESCENT}$ + $I_{INPUTS}$ + $I_{DYNAMIC}$
    $I_C$ = $I_{CC}+\Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    $I_{CC}$ = Quiescent Current with CMOS input levels
    $\Delta I_{CC}$ = Power Supply Current for a TTL HIGH input ($V_{IN}$=3.4V)
    $D_H$ = Duty Cycle for TTL inputs HIGH
    $N_T$ = Number of TTL inputs at $D_H$
    $I_{CCD}$ = Dynamic Current caused by an input transition pair (HLH or LHL)
    $f_0$ = Clock frequency for registered devices, otherwise zero
    $f_1$ = Input signal frequency
    $N_1$ = Number of inputs changing at $f_1$
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed but not tested.

## Switching Characteristics Over the Operating Range

| Parameter | Description | FCT646T/FCT648T | | | | FCT646AT/FCT648AT | | | | Unit | Fig. No.[15] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Military | | Commercial | | Military | | Commercial | | | |
| | | Min.[14] | Max. | Min.[14] | Max. | Min.[14] | Max. | Min.[14] | Max. | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Bus to Bus | 2.0 | 11.0 | 1.5 | 9.0 | 2.0 | 7.7 | 1.5 | 6.3 | ns | 1, 3 |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time Enable to Bus and DIR to $A_n$ or $B_n$ | 2.0 | 15.0 | 1.5 | 14.0 | 2.0 | 10.5 | 1.5 | 9.8 | ns | 1, 7, 8 |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time $\overline{G}$ to Bus and DIR toBus | 2.0 | 11.0 | 1.5 | 9.0 | 2.0 | 7.7 | 1.5 | 6.3 | ns | 1, 7, 8 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Clock to Bus | 2.0 | 10.0 | 1.5 | 9.0 | 2.0 | 7.0 | 1.5 | 6.3 | ns | 1, 5 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay SBA or SAB to A or B | 2.0 | 12.0 | 1.5 | 11.0 | 2.0 | 8.4 | 1.5 | 7.7 | ns | 1, 5 |
| $t_S$ | Set-Up Time HIGH or LOW, Bus to Clock | 4.5 | | 4.0 | | 2.0 | | 2.0 | | ns | 4 |
| $t_H$ | Hold Time HIGH or LOW, Bus to Clock | 2.0 | | 2.0 | | 1.5 | | 1.5 | | ns | 4 |
| $t_W$ | Pulse Width,[6] HIGH or LOW | 6.0 | | 6.0 | | 5.0 | | 5.0 | | ns | 5 |

| Parameter | Description | FCT646CT/FCT648CT | | | | Unit | Fig. No.[15] |
|---|---|---|---|---|---|---|---|
| | | Military | | Commercial | | | |
| | | Min.[14] | Max. | Min.[14] | Max. | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Bus to Bus | 1.5 | 6.0 | 1.5 | 5.4 | ns | 1, 3 |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time Enable to Bus and DIR to $A_n$ or $B_n$ | 1.5 | 8.9 | 1.5 | 7.8 | ns | 1, 7, 8 |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time $\overline{G}$ to Bus and DIR toBus | 1.5 | 7.7 | 1.5 | 6.3 | ns | 1, 7, 8 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Clock to Bus | 1.5 | 6.3 | 1.5 | 5.7 | ns | 1, 5 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay SBA or SAB to A or B | 1.5 | 7.0 | 1.5 | 6.2 | ns | 1, 5 |
| $t_S$ | Set-Up Time, HIGH or LOW, Bus to Clock | 2.0 | | 2.0 | | ns | 4 |
| $t_H$ | Hold Time, HIGH or LOW, Bus to Clock | 1.5 | | 1.5 | | ns | 4 |
| $t_W$ | Pulse Width,[6] HIGH or LOW | 5.0 | | 5.0 | | ns | 5 |

**Notes:**
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. See “Parameter Measurement Information” in the General Information Section.

## Ordering Information − FCT646T

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 5.4 | CY74FCT646CTPC | P13/13A | 24-Lead (300-Mil) Molded DIP | Commercial |
| | CY74FCT646CTQC | Q13 | 24-Lead (150-Mil) QSOP | |
| | CY74FCT646CTSOC | S13 | 24-Lead (300-Mil) Molded SOIC | |
| 6.0 | CY54FCT646CTDMB | D14 | 24-Lead (300-Mil) CerDIP | Military |
| | CY54FCT646CTLMB | L64 | 28-Square Leadless Chip Carrier | |
| 6.3 | CY74FCT646ATPC | P13/13A | 24-Lead (300-Mil) Molded DIP | Commercial |
| | CY74FCT646ATQC | Q13 | 24-Lead (150-Mil) QSOP | |
| | CY74FCT646ATSOC | S13 | 24-Lead (300-Mil) Molded SOIC | |
| 7.7 | CY54FCT646ATDMB | D14 | 24-Lead (300-Mil) CerDIP | Military |
| | CY54FCT646ATLMB | L64 | 28-Square Leadless Chip Carrier | |
| 9.0 | CY74FCT646TPC | P13/13A | 24-Lead (300-Mil) Molded DIP | Commercial |
| | CY74FCT646TQC | Q13 | 24-Lead (150-Mil) QSOP | |
| | CY74FCT646TSOC | S13 | 24-Lead (300-Mil) Molded SOIC | |
| 11.0 | CY54FCT646TDMB | D14 | 24-Lead (300-Mil) CerDIP | Military |
| | CY54FCT646TLMB | L64 | 28-Square Leadless Chip Carrier | |

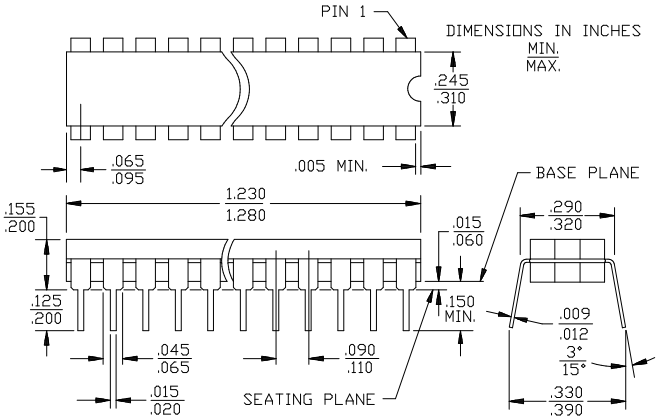
## Ordering Information—FCT648T

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 5.4 | CY74FCT648CTPC | P13/13A | 24-Lead (300-Mil) Molded DIP | Commercial |
| | CY74FCT648CTQC | Q13 | 24-Lead (150-Mil) QSOP | |
| | CY74FCT648CTSOC | S13 | 24-Lead (300-Mil) Molded SOIC | |
| 6.0 | CY54FCT648CTDMB | D14 | 24-Lead (300-Mil) CerDIP | Military |
| | CY54FCT648CTLMB | L64 | 28-Square Leadless Chip Carrier | |
| 6.3 | CY74FCT648ATPC | P13/13A | 24-Lead (300-Mil) Molded DIP | Commercial |
| | CY74FCT648ATQC | Q13 | 24-Lead (150-Mil) QSOP | |
| | CY74FCT648ATSOC | S13 | 24-Lead (300-Mil) Molded SOIC | |
| 7.7 | CY54FCT648ATDMB | D14 | 24-Lead (300-Mil) CerDIP | Military |
| | CY54FCT648ATLMB | L64 | 28-Square Leadless Chip Carrier | |
| 9.0 | CY74FCT648TPC | P13/13A | 24-Lead (300-Mil) Molded DIP | Commercial |
| | CY74FCT648TQC | Q13 | 24-Lead (150-Mil) QSOP | |
| | CY74FCT648TSOC | S13 | 24-Lead (300-Mil) Molded SOIC | |
| 11.0 | CY54FCT648TDMB | D14 | 24-Lead (300-Mil) CerDIP | Military |
| | CY54FCT648TLMB | L64 | 28-Square Leadless Chip Carrier | |

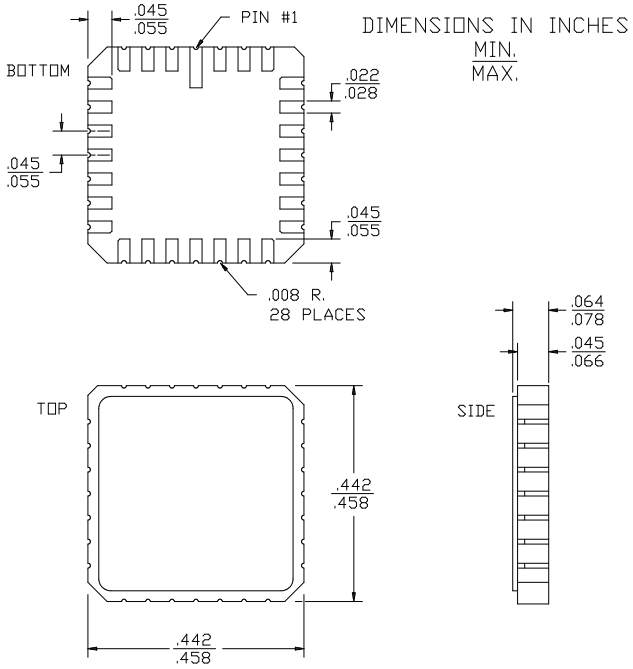
Document #: 38−00267−A

## Package Diagrams

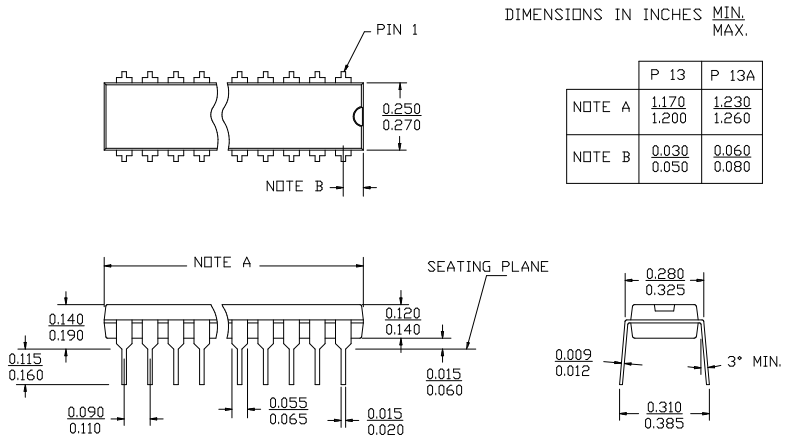
**24-Lead (300-Mil) CerDIP D14**
MIL−STD−1835 D−9 Config. A




**28-Square Leadless Chip Carrier L64**
MIL−STD−1835 C−4




**24-Lead (300-Mil) Molded DIP P13/P13A**




| | P 13 | P 13A |
|---|---|---|
| NOTE A | 1.170<br>1.200 | 1.230<br>1.260 |
| NOTE B | 0.030<br>0.050 | 0.060<br>0.080 |

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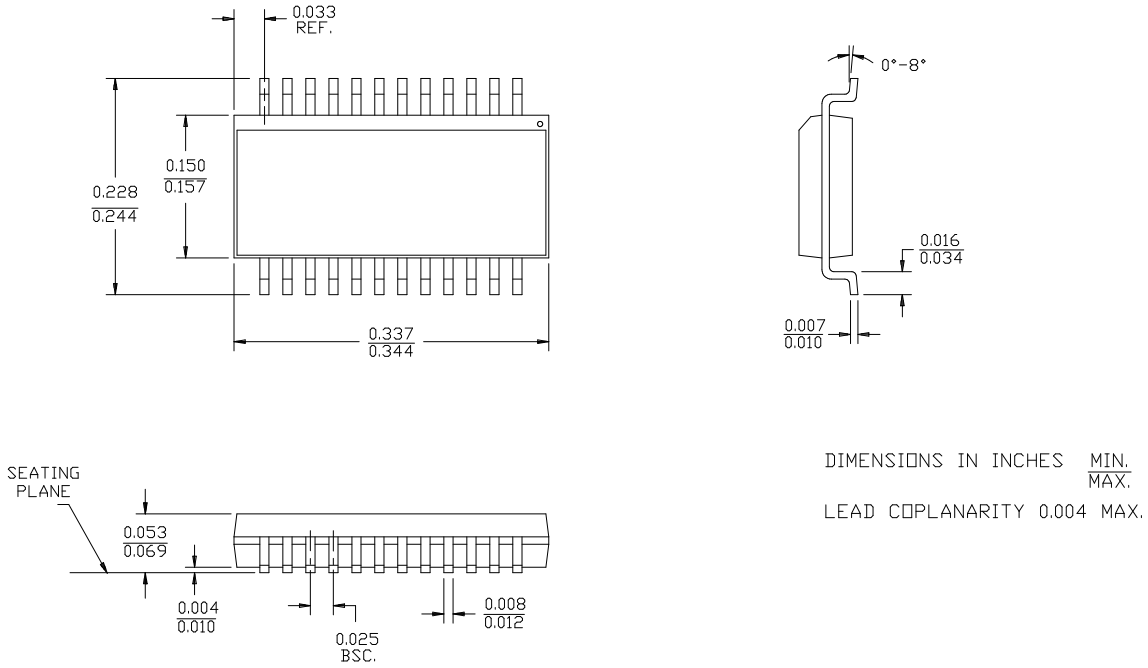
## 24-Lead Quarter Size Outline Q13




## 24-Lead (300-Mil) Molded SOIC S13