Parameter Measurement Information

Features

- **Function, pinout, speed, and drive compatible with F Logic**
- **Meets requirements of FCT Logic JEDEC Standard No. 18A**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature on all families**
- **Matched rise and fall times**
- **CMOS for low power consumption − typically 1/3 of the fastest advanced Schottky TTL logic**
- **Inputs and outputs interface directly with TTL, NMOS, and CMOS devices**
- **Typically 64 mA Sink and 32 mA Source Drive Capability**
- **Three-state outputs on most devices**
- **Operational over the full commercial and military temperature ranges (Octal)**
- **Extended commercial temperature range of −40°C to +85°C (16-bit family)**
- **Products available to latest revision of MIL-STD-8833 class B compliance**

Functional Description

Overview

FCT-T, FCT2-T, and FCT16-T are logic families consisting of high-performance, low power, CMOS integrated circuits that either meet or exceed the speed and drive capability of their popular functional equivalents. These families represent a technology crossover point that occurred when the performance achieved using CMOS technology matched that of bipolar technology at one-third the power.

All logic families are TTL compatible, which means that they conform to the industry-standard TTL voltage levels and threshold point, and operate from a 5V V_{CC} power source. The TTL threshold point is 1.5V. All inputs have hysteresis. The benefit to the user is increased static and dynamic noise immunity, as well as less sensitivity to noise superimposed on slowly rising or falling inputs.

The outputs of the original FCT family swing rail-to-rail, i.e., from V_{OL}=0.4V to V_{OH}=V_{CC}−0.2V. The datasheets specify V_{OH} minimum as 2.4V when sourcing 15 mA and typical as 4.3. The output pull-up transistor is a p-channel device. Typical unloaded output signal rise and fall times are one nanosecond.

The new FCT-T logic families feature output buffers that use n-channel pullup transistors and controlled rise and fall time edge rates. Typical unloaded output signal rise and fall times are two nanoseconds. The maximum unloaded output high voltage, V_{OH}, is V_{CC} minus the n-channel threshold, V_T. The transistor drain is connected to V_{CC}, so V_T is approximately one volt. The loaded V_{OH} is typically 3.3 Volts when sourcing 15 mA with a V_{CC} of 5.0V.

The reduced output voltage swing of FCT-T results in lower crosstalk. The controlled edge rates reduce crosstalk as well as ground bounce.

The FCT2-T logic family is identical to the FCT-T logic family, except that the FCT2-T devices have a 25-Ohm resistor in series with the output. The purpose of the resistor is to provide series damping when driving a transmission line. These products with series damping resistors should be used only when driving lumped (or single) loads, and should not be used for driving multiple or distributed loads. For a description of series damping, see the application note "System Design Considerations When Using Cypress CMOS Circuits" in the *Cypress Applications Handbook.*

The FCT16-T logic family is a 16-bit version of the FCT-T family. The commercial temperature range of the family has been extended to −40°C to +85°C and Vcc tolerance has been loosened to ±10%. Multiple power and grounds have been added to reduce typical ground bounce to below 1.0V.

The FCT162-T logic family is a 24 mA balanced drive version of the FCT16-T family and is intended for use in driving transmission lines.

CMOS Process Technology

All products are manufactured using the Logic 2.7 process and are fabricated in a Class 1 facility on six inch wafers. The minimum drawn channel length is 0.65 microns. The process uses one layer of polysilicon and two layers of metal. There is no substrate bias generator. In addition to providing high density, the technology assures latch-up protection, single event upset protection, and excellent ESD protection.

Switching Characteristics

The circuit of *Figure 1* is used to load each output for specifying and measuring device propagation delays. It is a de facto industry standard and does not represent device behavior in any application.

The switch is open for all measurements except those having to do with the outputs entering or leaving the high impedance state as a result of a control input changing.

These conditions are illustrated in *Figures 7* and *8*. The parameter t_{PZL} is the amount of time it takes an output to go from the high-impedance state to a low state. The parameter t_{PLZ} is the amount of time it takes an output to go from the LOW state to the high-impedance state: defined as 300 mV above V_{OL}. The parameter t_{PZH} is the amount of time it takes an output to go from a high-impedance state to the HIGH state. The parameter t_{PHZ} is the amount of time it takes an output to go from a HIGH state to the high-impedance state; defined as 300 mV below V_{OH}.

Figures 2 through *9* illustrate the various propagation delay, set-up times, and hold times that are referred to in the Switching Characteristics section of the various datasheets. Note that except for entering the high impedance state, all measurements are made between the 1.5V amplitude voltage levels.

The input waveform amplitude levels recommended for AC testing of Cypress logic products are illustrated in *Figure 10*. Input signals should have maximum rise and fall times of 2.5 ns and signal swings of zero to three volts. Input signals with rise and fall times of one nanosecond should be used for testing minimum pulse width or maximum frequency.

When performing AC tests, care must be taken to insure that the input signals do not return to the transition region due to signal overshoot or undershoot. It is recommended that the load capacitor be a leaderless chipcap. If this is not possible, keep the leads as short as possible in order to avoid signal overshoot and undershoot due to lead inductance. The same reasoning applies to the load resistors and power supply decoupling and filtering capacitors. Solid grounding is required and a ground plane is recommended.

Power Specifications

Cypress logic devices do not use a substrate bias generator. As a result, the quiescent or standby current is typically a few microamperes when the voltage at the inputs are either less than 0.2V or greater than $V_{CC}-0.2V$. On the datasheet this current is described as Quiescent Power Supply Current, given the symbol I_{CC}, and specified on a per IC basis. No inputs are switching and all outputs are open, and if possible, disabled.

When the input signal transitions between the logic levels, both the p-channel pull-up transistor and the n-channel pulldown transistor in the input TTL to CMOS translator are partially turned on, which creates a low-impedance path between V_{CC} and ground. On the datasheet this current is described as "Quiescent Power Supply Current (TTL inputs)," given the symbol ΔI_{CC}, and specified on a per input basis. One input is at $V_{IN}=3.4V$ and other inputs at either V_{CC} or 0 Volts, and all outputs are open, and if possible, disabled.

The Dynamic Power Supply Current, given the symbol I_{CCD}, is not measured directly, but is provided so that the user can calculate total current. It is specified in mA per Megahertz at 50% duty cycle, with one input toggling and one output toggling (enabled) but open (unloaded).

Note that the preceding three currents are specified with the outputs open. The AC CVf current required to charge and discharge parasitic capacitances (e.g., other inputs being driven by the outputs), as well as any DC load currents must be calculated separately.

Total supply current, I_C, is specified on the data sheet for several different conditions. The inputs are switched between ground and either TTL (3.4V) or CMOS ($V_{CC}-0.2V$) levels with rise and fall times of 2.5 ns. Slow rise and fall times can cause the dynamic current to increase, because the input signals are within the transition region for longer times. A characterization curve of normalized ($I_{CC}/\Delta I_{CC}$) currents versus V_{IN} is shown in *Figure 14*.

Total device current can be estimated by using the following formula to calculate the total current. This equation implies calculating the current associated with each input and adding them up. The same procedure must be followed to calculate the CVf current required to charge and discharge the load capacitances.

$$I_C=I_{CC}+\Delta I_{CC} D_H N_T+I_{CCD} (f_{cp}/2+f_n N_n)$$

Where:

I_{CC} = Quiescent Current
I_{CC} = Power Supply Current for a TTL HIGH input (V_{IN} = 3.4 V)
D_H = Duty Cycle for TTL inputs HIGH
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f_{CP} = Clock frequency for registered devices, otherwise zero
f_n = Input signal frequency
N_n = Number of inputs changing at Fn

ESD (Electrostatic Discharge) Precautions

Large electrical fields can damage the thin gate oxides of MOS transistors. Special input protection circuits are used at every input pin of all Cypress products to provide protection against ESD. This circuitry has been designed to withstand repeated applications of high voltages without failure or performance degradation. This is accomplished by preventing the high voltage (ESD) from reaching the thin gate oxides of the internal transistors. For a description of the ESD protection circuit and an explanation of its operation, please see the application note titled "Input/Output Characteristics of Cypress Circuits" in the *Cypress Applications Handbook.*

Precautions should be taken by persons handling CMOS devices. It is recommended that individuals wear a grounded wrist strap or ankle strap when handling Cypress FCT-T devices.

Maximum Ratings[1, 2]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range FCT-T, FCT2-T

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT, DT	0°C to +70°C	5V ± 5%
Commercial	T, AT, BT	−40°C to +85°C	5V ± 5%
Military[3]	All	−55°C to +125°C	5V ± 10%

Operating Range FCT16-T

Range	Ambient Temperature	V_{CC}
Commercial	−40°C to +85°C	5V ± 10%

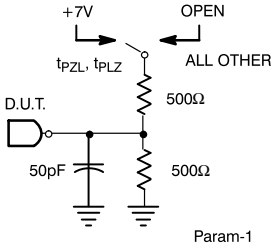

Figure 1. Test Load

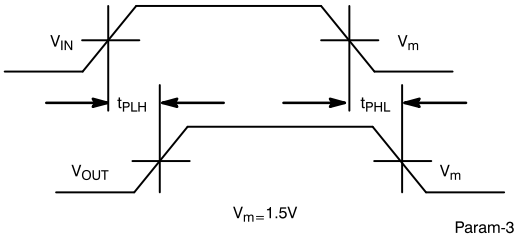

Figure 3. Waveform for Non-Inverting Functions

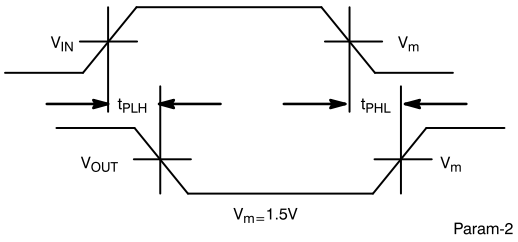

Figure 2. Waveform for Inverting Functions

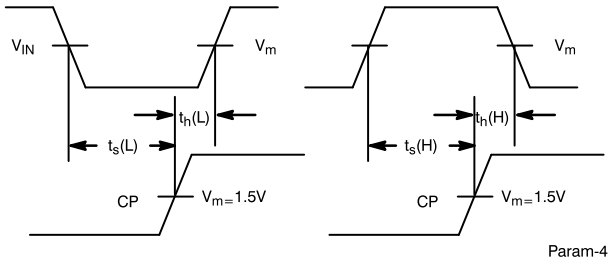

Figure 4. Set-Up and Hold Times, Rising-Edge Clock

Notes:

1. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. T_A is the "instant on" case temperature.

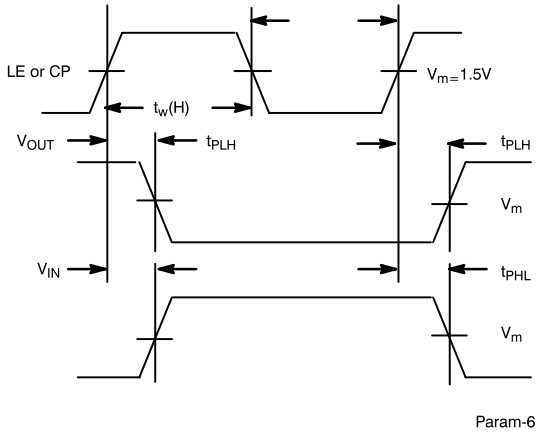

Figure 5. Propagation Delays from Rising-Edge Clock or Enable

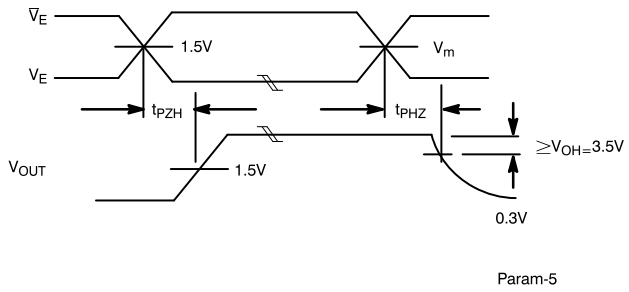

Figure 8. Three-State Output HIGH Enable and Disable Times

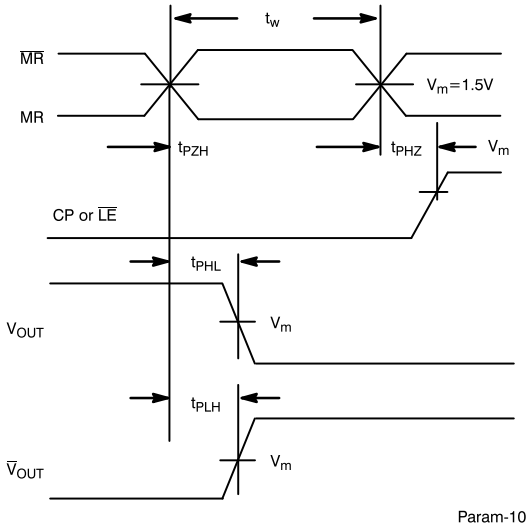

Figure 6. Asynchronous Reset, Active Rising-Edge Clock or Active LOW Enable

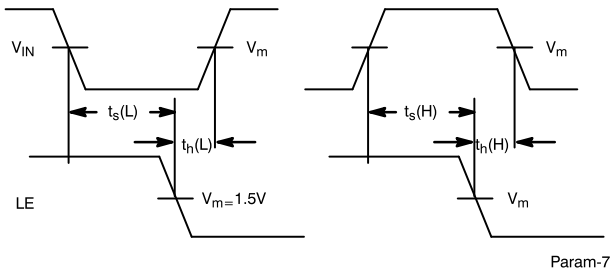

Figure 9. Set-Up and Hold Times to Active HIGH Enable or Parallel Load

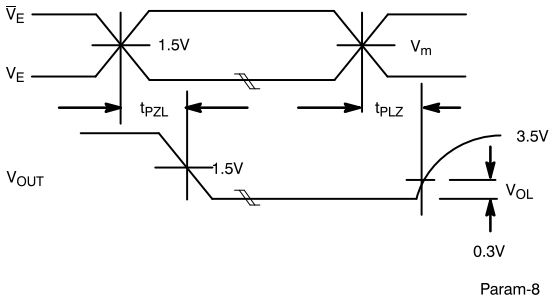

Figure 7. Three-State Output LOW Enable and Disable Times

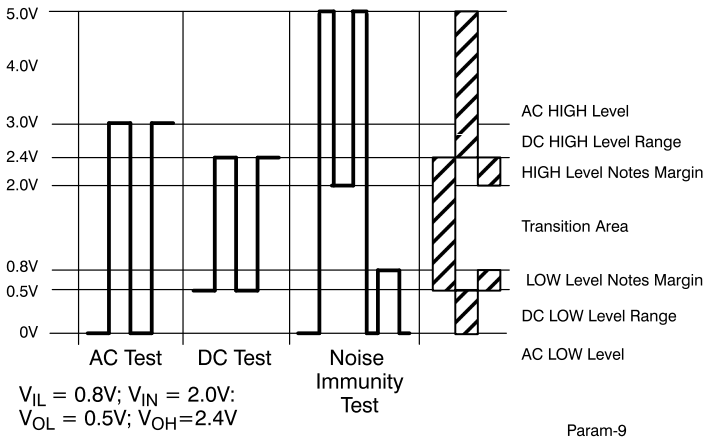

Figure 10. Input Signal Levels

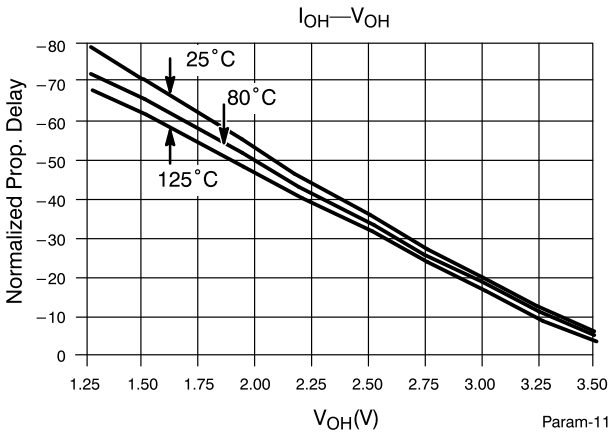

Figure 11. Output Source Current vs. Output Voltage

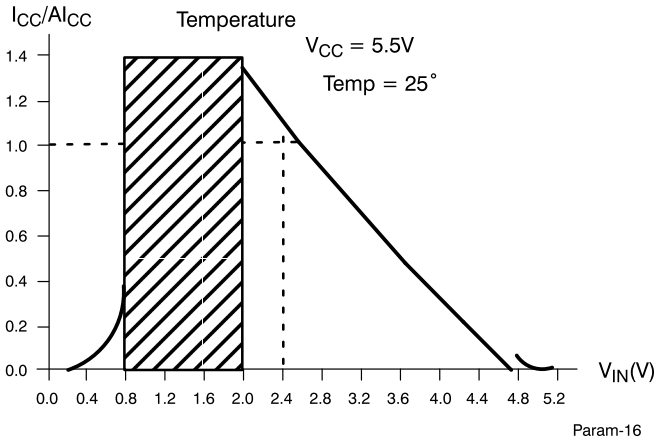

Figure 14. Normalized Current vs. Input Voltage

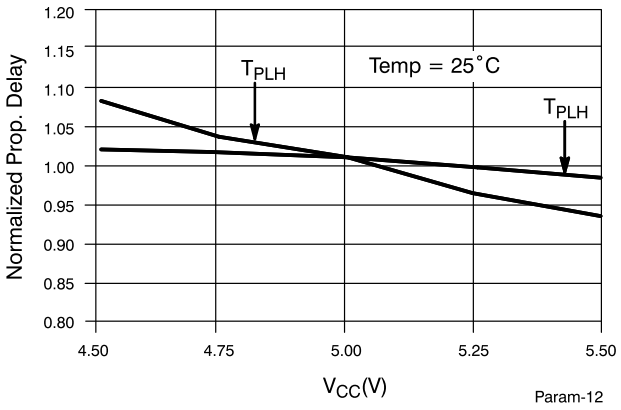

Figure 12. Normalized Propagation Delay vs. V_{CC}

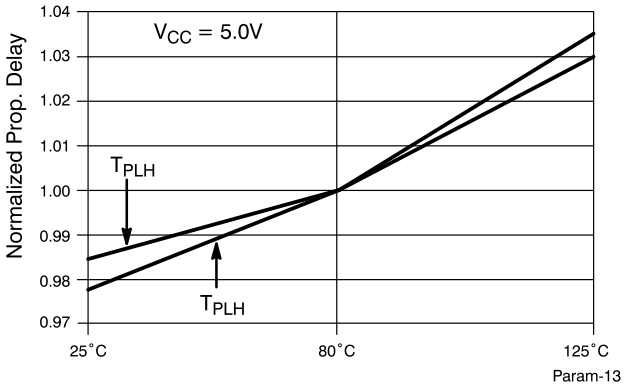

Figure 15. Normalized Propagation Delay vs. Temperature

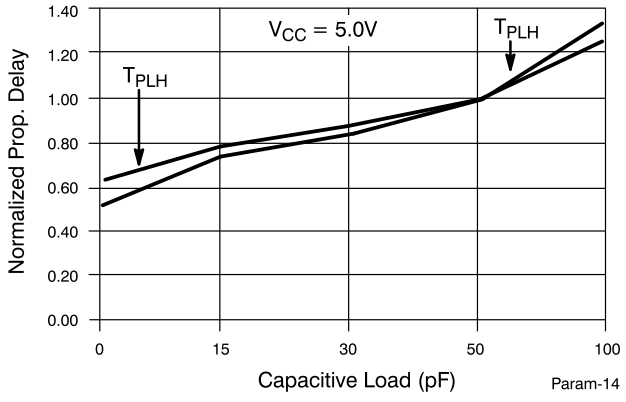

Figure 13. Normalized Propagation Delay vs. Output Loading

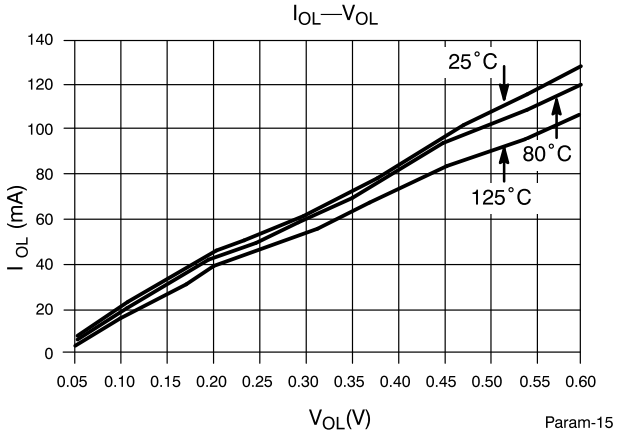

Figure 16. Output Sink Current vs. Output Voltage