

Intel® 82430FX PCIset Level II Cache Module Family

Features

- **Pin-compatible secondary cache module family that adheres to the Intel COAST 1.1 specification**
- **Asynchronous (CYM74B430), synchronous pipelined (CYM74P430, CYM74P431), or synchronous (CYM74S430, CYM74S431) configurations with presence and configuration detect pins**
- **Ideal for Intel® P54C-based systems with the 82430FX (Triton) chipset**
- **Operates at 50, 60, and 66 MHz**
- **Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs**
- **160-position Burndy DIMM CELP2X80SC3Z48 connector**

- **3.3V compatible inputs/data outputs**

Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the 82430FX (Triton) chipset.

CYM74B430 is an asynchronous 256-Kbyte cache module that provides a low-cost, high-performance solution with industry standard 32Kx8 5V SRAMs and 3.3V level translators. The CYM74B430 is organized as 32K by 64-bits with an 8Kx8 tag that supports 3-2-2-2 read and 4-2-2-2 write cycles at CPU bus speeds up to 66 MHz.

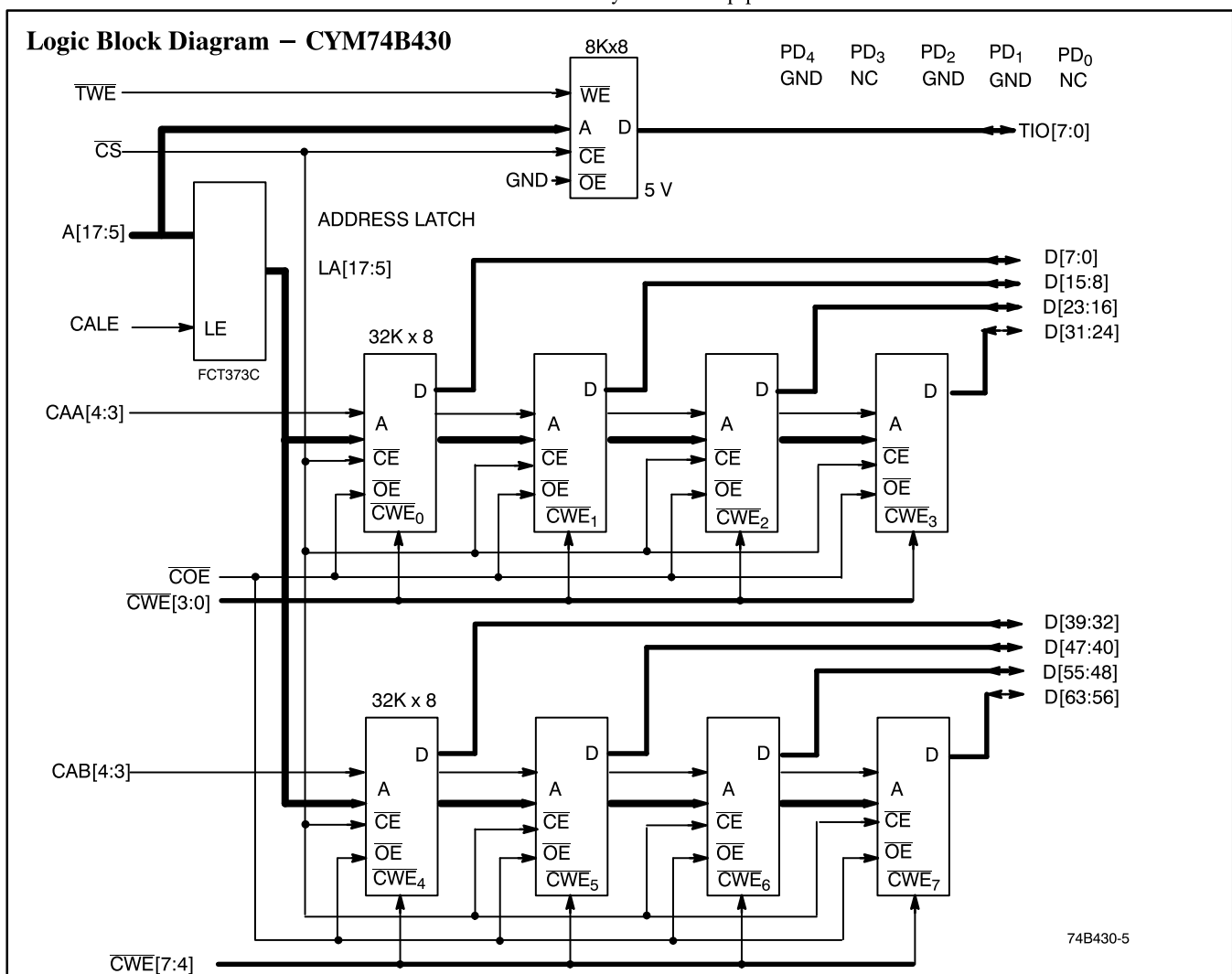
The synchronous modules are available with low cost synchronous pipelined RAMs, or high performance synchronous burst RAMs. The synchronous pipelined

modules are based on a 16Kx64 RAM. The CYM74P430 is a 256-KB module while the CYM74P431 is a 512-KB module.

The CYM74S430 and CYM74S431 are high performance synchronous burst cache modules that provide 256 KB and 512 KB of cache respectively. The modules support 3-1-1 performance at 66 MHz.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 150 micro-inches of nickel covered by 10 micro-inches of gold flash.



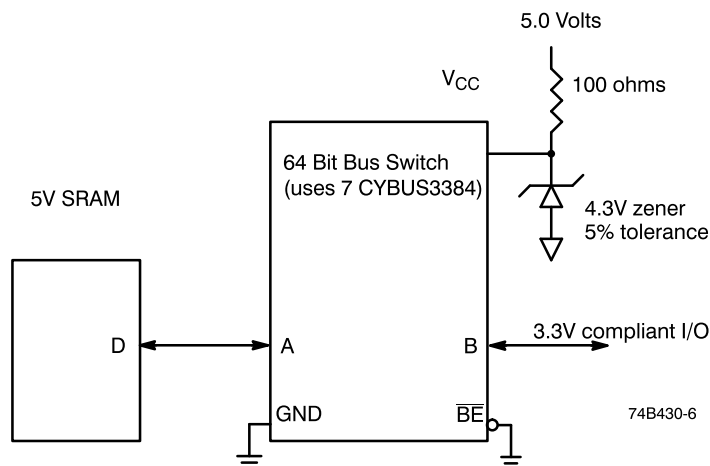
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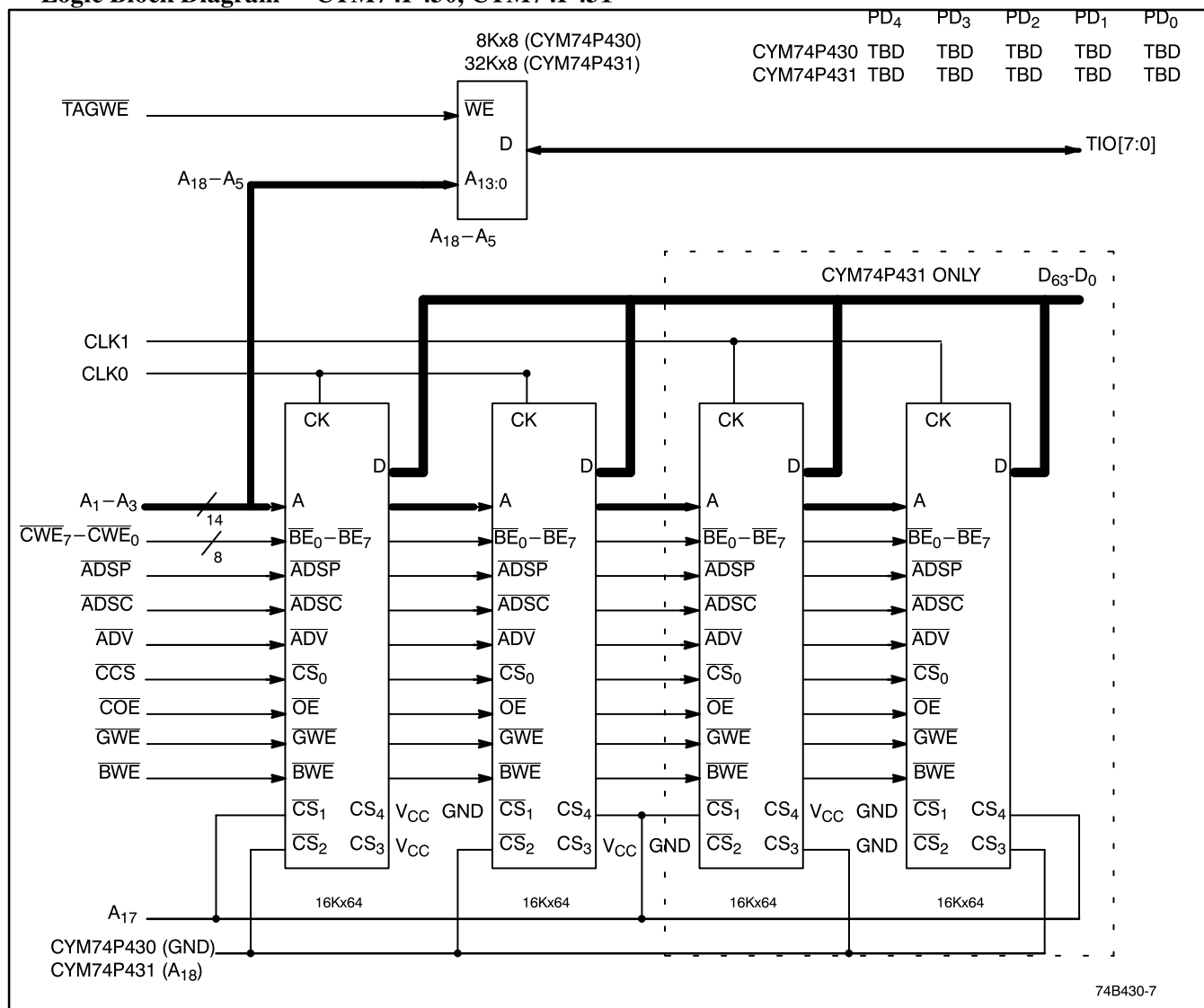
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CYM74B430
CYM74P430/31
CYM74S430/31

Block Diagram: 5V to 3.3V Level Conversion (CYM74B430)

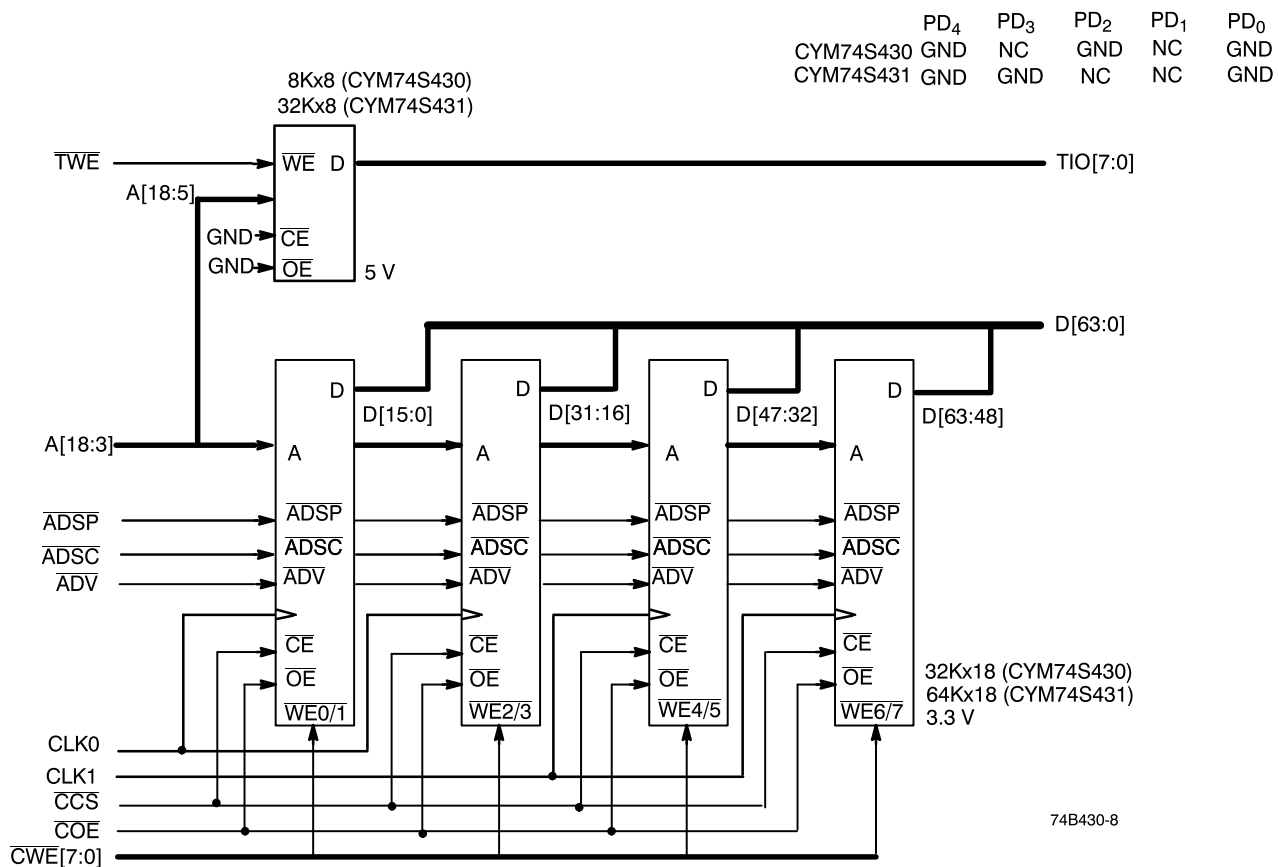


Logic Block Diagram – CYM74P430, CYM74P431





Logic Block Diagram – CYM74S430/CYM74S431^[1]



Note:

1. A18 is not used by CYM74S430. DP pins are pulled high through 10KΩ



Selection Guide

	Asynchronous Cache Modules		
Part Number	74B430–50	74B430–60	74B430–66
Cache Size	256 KB		
System Clock (MHz)	50	60	66
Data t_{AA}	20 ns	17 ns	15 ns
Tag t_{AA}	30 ns	20 ns	15 ns

	Synchronous Pipelined Cache Modules					
Part Number	74P430–50	74P430–60	74P430–66	74P431–50	74P431–60	74P431–66
Cache Size	256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66
Data t_{CDV}	13.5 ns	10 ns	8.5 ns	13.5 ns	10 ns	8.5 ns
Tag t_{AA}	30 ns	20 ns	15 ns	30 ns	20 ns	15 ns

	Synchronous Burst Cache Modules					
Part Number	74S430–50	74S430–60	74S430–66	74S431–50	74S431–60	74S431–66
Cache Size	256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66
Data t_{CDV}	13.5 ns	10 ns	8.5 ns	13.5 ns	10 ns	8.5 ns
Tag t_{AA}	30 ns	20 ns	15 ns	30 ns	20 ns	15 ns



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CYM74B430
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Pin Configuration

Dual Read-Out SIMM (DIMM)

Top View

GND	81	1	GND
TIO ₁	82	2	TIO ₀
TIO ₇	83	3	TIO ₂
TIO ₅	84	4	TIO ₆
TIO ₃	85	5	TIO ₄
RSVD	86	6	RSVD
V _{CC}	87	7	NC (CYM74B430) / V _{CCQ} (CYM74P43X, CYM74S43X)
RSVD	88	8	TWE
(CYM74P43X, CYM74S43X) \overline{ADV} / (CYM74B430) CAA ₄	89	9	CAA ₃ (CYM74B430) / \overline{ADSC} (CYM74P43X, CYM74S43X)
GND	90	10	GND
COE	91	11	CWE ₄
CWE ₅	92	12	CWE ₆
CWE ₇	93	13	CWE ₀
CWE ₁	94	14	CWE ₂
V _{CC}	95	15	NC (CYM74B430) / V _{CCQ} (CYM74P43X, CYM74S43X)
CWE ₃	96	16	CAB ₄ (CYM74B430) / CCS (CYM74P43X, CYM74S43X)
(CYM74P43X, CYM74S43X) NC / (CYM74B430) CAB ₃	97	17	(GWE) (CYM74P43X)
(CYM74P43X, CYM74S43X) NC / (CYM74B430) CALE	98	18	(BWE) (CYM74P43X)
GND	99	19	GND
RSVD	100	20	A ₃
A ₄	101	21	A ₇
A ₆	102	22	A ₅
A ₈	103	23	A ₁₁
A ₁₀	104	24	A ₁₆
V _{CC}	105	25	NC (CYM74B430) / V _{CCQ} (CYM74P43X, CYM74S43X)
A ₁₇	106	26	NC (74B430, 74S430) / GND (74P430) / A ₁₈ (74P431, 74S431)
GND	107	27	GND
A ₉	108	28	A ₁₂
A ₁₄	109	29	A ₁₃
A ₁₅	110	30	NC (CYM74B430) / \overline{ADSP} (CYM74P43X, CYM74S43X)
RSVD	111	31	CS (CYM74B430) / NC (CYM74P43X, CYM74S43X)
PD ₀	112	32	NC (ECS2)
PD ₂	113	33	PD ₁
PD ₄	114	34	PD ₃
GND	115	35	GND
(CYM74P43X, CYM74S43X) CLK ₀ / (CYM74B430) NC	116	36	NC (CYM74B430, CYM74P430) / CLK ₁ (CYM74P431, CYM74S43X)
GND	117	37	GND
D ₆₃	118	38	D ₆₂
V _{CC}	119	39	NC (CYM74B430) / V _{CCQ} (CYM74P43X, CYM74S43X)
D ₆₁	120	40	D ₆₀
D ₅₉	121	41	D ₅₈
D ₅₇	122	42	D ₅₆
GND	123	43	GND
D ₅₅	124	44	D ₅₄
D ₅₃	125	45	D ₅₂
D ₅₁	126	46	D ₅₀
D ₄₉	127	47	D ₄₈
GND	128	48	GND
D ₄₇	129	49	D ₄₆
D ₄₅	130	50	D ₄₄
D ₄₃	131	51	D ₄₂
V _{CC}	132	52	NC (CYM74B430) / V _{CCQ} (CYM74P43X, CYM74S43X)
D ₄₁	133	53	D ₄₀
D ₃₉	134	54	D ₃₈
D ₃₇	135	55	D ₃₆
GND	136	56	GND
D ₃₅	137	57	D ₃₄
D ₃₃	138	58	D ₃₂
D ₃₁	139	59	D ₃₀
V _{CC}	140	60	NC (CYM74B430) / V _{CCQ} (CYM74P43X, CYM74S43X)
D ₂₉	141	61	D ₂₈
D ₂₇	142	62	D ₂₆
D ₂₅	143	63	D ₂₄
GND	144	64	GND
D ₂₃	145	65	D ₂₂
D ₂₁	146	66	D ₂₀
D ₁₉	147	67	D ₁₈
V _{CC}	148	68	NC (CYM74B430) / V _{CCQ} (CYM74P43X, CYM74S43X)
D ₁₇	149	69	D ₁₆
D ₁₅	150	70	D ₁₄
D ₁₃	151	71	D ₁₂
GND	152	72	GND
D ₁₁	153	73	D ₁₀
D ₉	154	74	D ₈
D ₇	155	75	D ₆
V _{CC}	156	76	NC (CYM74B430) / V _{CCQ} (CYM74P43X, CYM74S43X)
D ₅	157	77	D ₄
D ₃	158	78	D ₂
D ₁	159	79	D ₀
GND	160	80	GND

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Pin Definitions

Common Signals	Description
V _{CC}	5V Supply
GND	Ground
A[18:3]	Addresses from processor
$\overline{\text{COE}}$	Output Enable
$\overline{\text{CWE}}[7:0]$	Byte Write Enables
PD ₀ –PD ₄	Presence Detect output pins
D[63:0]	Data lines from processor
TIO[7:0]	Tag data bits
$\overline{\text{TWE}}$	Tag Write Enable signal
NC	Signal not connected on module
RSVD	Reserved
CYM74B430 Only Signals	Description
CAA[4:3]	Lower two address bits for bank 0
CAB[4:3]	Lower two address bits for bank 1
CALE	Latch Enable
$\overline{\text{CS}}$	Chip Select
CYM74P43X, CYM74S43X Signals	Description
V _{CCQ}	3.3V Supply
ADSP	Processor Address Strobe
$\overline{\text{ADSC}}$	Cache Controller Address Strobe
ADV	Burst Address Advance
$\overline{\text{CCS}}$	Chip Select
CLK[1:0]	Clock signals, CLK1 not used on CYM74P430

Presence Detect Pins

	PD ₄	PD ₃	PD ₂	PD ₁	PD ₀
Asynchronous – CYM74B430	GND	NC	GND	GND	NC
Synchronous Pipelined – CYM74P430	TBD	TBD	TBD	TBD	TBD
Synchronous Pipelined – CYM74P431	TBD	TBD	TBD	TBD	TBD
Synchronous Burst – CYM74S430	GND	NC	GND	NC	GND
Synchronous Burst – CYM74S431	GND	GND	NC	NC	GND



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to $+125^{\circ}\text{C}$
Ambient Temperature
with Power Applied -0°C to $+70^{\circ}\text{C}$
3.3V Supply Voltage to Ground Potential ... -0.5V to $+5.25\text{V}$
5V Supply Voltage to Ground Potential -0.5V to $+5.25\text{V}$
DC Voltage Applied to Outputs
in High Z State -0.5V to $+4.6\text{V}$
DC Input Voltage -0.5V to $+4.6\text{V}$
Output Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature	V _{CC}	V _{CCQ}
Commercial (CYM74B430)	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 5\%$	N/A
Commercial (CYM74P43X, CYM74S43X)	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 5\%$	$5\text{V} \pm 5\%$ $3.3\text{V} + 10\%$ $- 5\%$

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage	CYM74B430	-0.5	0.8	V
V _{IL}	Input LOW Voltage	CYM74P43X, CYM74S43X	-0.3	0.8	V
V _{OH}	Output HIGH Voltage	V _{CC} =Min. I _{OH} = -4 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} =Min. I _{OL} = 8 mA		0.4	V
I _{CC} (74B430)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1600	mA
I _{CC} (74P430)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		TBD	mA
I _{CC} (74P431)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		TBD	mA
I _{CC} (74S430)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1200	mA
I _{CC} (74S431)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1400	mA

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM74B430PM-50C	PM34	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74P430PM-50C	TBD		Sync pipelined 256 KB	
	CYM74P431PM-50C	TBD		Sync pipelined 512 KB	
	CYM74S430PM-50C	PM28		Sync Burst 256 KB	
	CYM74S431PM-50C	PM28		Sync Burst 512 KB	
60	CYM74B430PM-60C	PM34	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74P430PM-60C	TBD		Sync pipelined 256 KB	
	CYM74P431PM-60C	TBD		Sync pipelined 512 KB	
	CYM74S430PM-60C	PM28		Sync Burst 256 KB	
	CYM74S431PM-60C	PM28		Sync Burst 512 KB	
66	CYM74B430PM-66C	PM34	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74P430PM-66C	TBD		Sync pipelined 256 KB	
	CYM74P431PM-66C	TBD		Sync pipelined 512 KB	
	CYM74S430PM-66C	PM28		Sync Burst 256 KB	
	CYM74S431PM-66C	PM28		Sync Burst 512 KB	

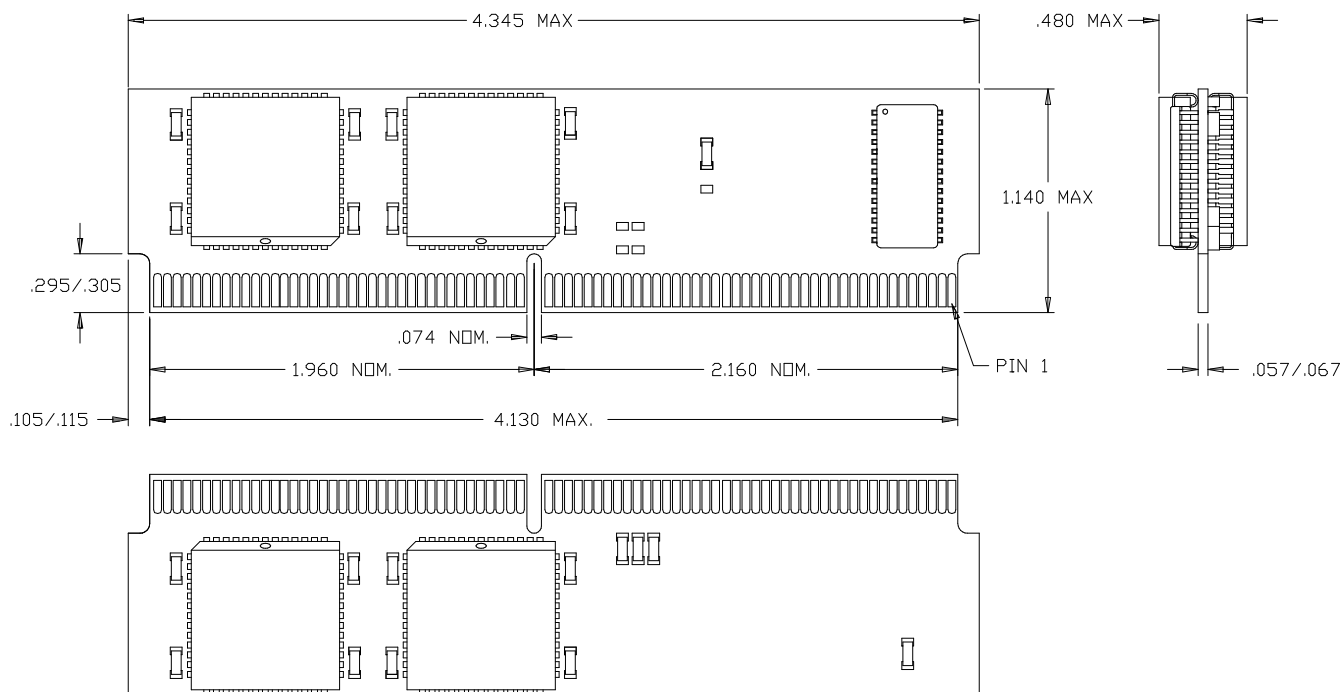


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CYM74B430
CYM74P430/31
CYM74S430/31

Package Diagrams

160-Pin Dual Readout SIMM PM28



160-Pin Dual Readout SIMM PM34

