



PRELIMINARY

# CYM74P430B/431B CYM74P434B/435B

## Intel™ 82430FX, HX, VX PCIset Pipelined L2 Cache Modules

### Features

- Secondary cache modules that are ideal for the Intel 82430FX, 82430HX, and 82430VX chip sets
- Complies with Intel COAST 3.0 cache module specifications
- High-performance cache modules based on synchronous pipelined 32Kx32 data BSRAM
- All modules contain series damping resistors on the data lines to improve system signal quality
- Operates at 50, 60, and 66 MHz

- 160-position connector is compatible with all four Keying Options defined in COAST 3.0.
- 3.3V compatible inputs/data outputs

### Functional Description

The cache modules are designed for Intel P54C/P55C systems with the 82430FX, 82430HX, and 82430VX chip sets. The CYM74P430B/431B/434B/435B modules are based on industry standard 32Kx32 synchronous pipelined BSRAM.

The CYM74P430B (256-Kbyte) and CYM74P431B (512-Kbyte) are high performance modules compatible with all three chipsets.

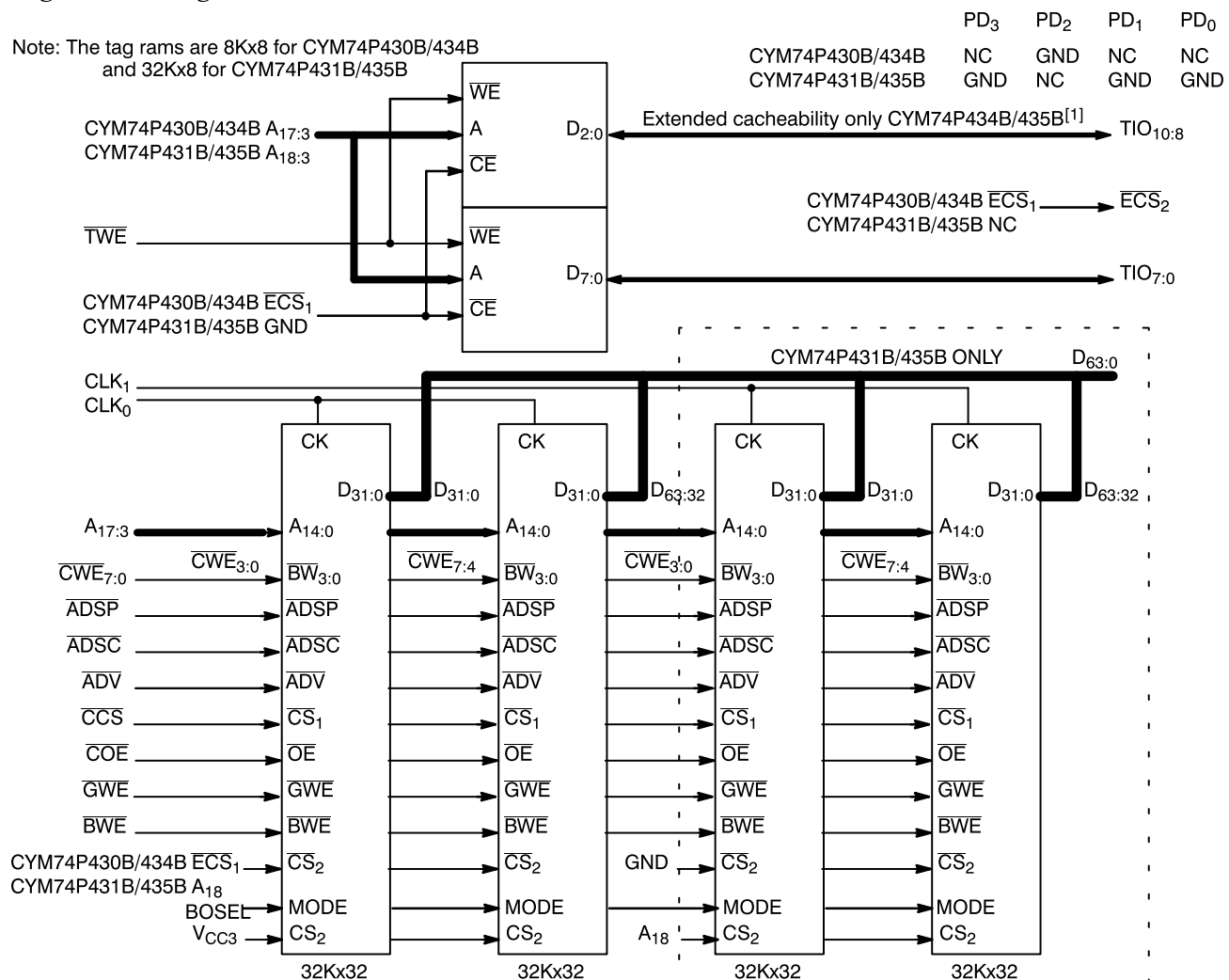
The CYM74P434B (256-Kbyte) and CYM74P435B (512-Kbyte) are high performance modules with extended cacheability for systems based on the 82430HX chipset.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity. All modules have series damping resistors on the data lines.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 150 micro-inches of gold covered by 30 micro-inches of gold.

### Logic Block Diagram

Note: The tag rams are 8Kx8 for CYM74P430B/434B and 32Kx8 for CYM74P431B/435B



Note: All modules have series damping resistors on each data line between the SRAM and the module connector.

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CYM74P430B,CYM74P431B  
CYM74P434B,CYM74P435B

## Selection Guide

	Synchronous Pipelined Cache Modules					
Part Number	74P430B-50	74P430B-60	74P430B-66	74P431B-50	74P431B-60	74P431B-66
Cache Size	256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66
Data SRAM $t_{CO}$ w/0 pF loading	13.5 ns	10 ns	8.5 ns	13.5 ns	10 ns	8.5 ns
Tag SRAM $t_{AA}$	20 ns	15 ns	15 ns	20 ns	15 ns	15 ns

	Synchronous Pipelined Cache Modules with Extended Cacheability					
Part Number	74P434B-50	74P434B-60	74P434B-66	74P435B-50	74P435B-60	74P435B-66
Cache Size	256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66
Data SRAM $t_{CO}$ w/0 pF loading	13.5 ns	10 ns	8.5 ns	13.5 ns	10 ns	8.5 ns
Tag SRAM $t_{AA}$	20 ns	15 ns	15 ns	20 ns	15 ns	15 ns



# Pin Configuration

## Dual Read-Out SIMM (DIMM)

### Top View

GND	81	1	GND
TIO <sub>1</sub>	82	2	TIO <sub>0</sub>
TIO <sub>7</sub>	83	3	TIO <sub>2</sub>
TIO <sub>5</sub>	84	4	TIO <sub>6</sub>
TIO <sub>3</sub>	85	5	TIO <sub>4</sub>
NOTE 1 (CYM74P434B, CYM74P435B) TIO <sub>9</sub>	86	6	TIO <sub>8</sub> (CYM74P434B, CYM74P435B) NOTE 1
V <sub>CC5</sub>	87	7	V <sub>CC3</sub>
NOTE 1 (CYM74P434B, CYM74P435B) TIO <sub>10</sub>	88	8	TWE
ADV	89	9	ADSC
GND	90	10	GND
COE	91	11	CWE <sub>4</sub>
CWE <sub>5</sub>	92	12	CWE <sub>6</sub>
CWE <sub>7</sub>	93	13	CWE <sub>0</sub>
CWE <sub>1</sub>	94	14	CWE <sub>2</sub>
V <sub>CC5</sub>	95	15	V <sub>CC3</sub>
CWE <sub>3</sub>	96	16	CCS
NC	97	17	GWE
NC	98	18	BWE
GND	99	19	GND
RSVD	100	20	A <sub>3</sub>
A <sub>4</sub>	101	21	A <sub>7</sub>
A <sub>6</sub>	102	22	A <sub>5</sub>
A <sub>8</sub>	103	23	A <sub>11</sub>
A <sub>10</sub>	104	24	A <sub>16</sub>
V <sub>CC5</sub>	105	25	V <sub>CC3</sub>
A <sub>17</sub>	106	26	A <sub>18</sub> (CYM74P431B, CYM74P435B)
GND	107	27	GND
A <sub>9</sub>	108	28	A <sub>12</sub>
A <sub>14</sub>	109	29	A <sub>13</sub>
A <sub>15</sub>	110	30	ADSP
RSVD	111	31	ECS <sub>1</sub>
PD <sub>0</sub>	112	32	ECS <sub>2</sub>
PD <sub>2</sub>	113	33	PD <sub>1</sub>
NOTE 2 BOSEL	114	34	PD <sub>3</sub>
GND	115	35	GND
CLK <sub>0</sub>	116	36	CLK <sub>1</sub> (CYM74P431B, CYM74P435B)
GND	117	37	GND
D <sub>63</sub>	118	38	D <sub>62</sub>
V <sub>CC5</sub>	119	39	V <sub>CC3</sub>
D <sub>61</sub>	120	40	D <sub>60</sub>
D <sub>59</sub>	121	41	D <sub>58</sub>
D <sub>57</sub>	122	42	D <sub>56</sub>
GND	123	43	GND
D <sub>55</sub>	124	44	D <sub>54</sub>
D <sub>53</sub>	125	45	D <sub>52</sub>
D <sub>51</sub>	126	46	D <sub>50</sub>
D <sub>49</sub>	127	47	D <sub>48</sub>
GND	128	48	GND
D <sub>47</sub>	129	49	D <sub>46</sub>
D <sub>45</sub>	130	50	D <sub>44</sub>
D <sub>43</sub>	131	51	D <sub>42</sub>
V <sub>CC5</sub>	132	52	V <sub>CC3</sub>
D <sub>41</sub>	133	53	D <sub>40</sub>
D <sub>39</sub>	134	54	D <sub>38</sub>
D <sub>37</sub>	135	55	D <sub>36</sub>
GND	136	56	GND
D <sub>35</sub>	137	57	D <sub>34</sub>
D <sub>33</sub>	138	58	D <sub>32</sub>
D <sub>31</sub>	139	59	D <sub>30</sub>
V <sub>CC</sub>	140	60	V <sub>CC3</sub>
D <sub>29</sub>	141	61	D <sub>28</sub>
D <sub>27</sub>	142	62	D <sub>26</sub>
D <sub>25</sub>	143	63	D <sub>24</sub>
GND	144	64	GND
D <sub>23</sub>	145	65	D <sub>22</sub>
D <sub>21</sub>	146	66	D <sub>20</sub>
D <sub>19</sub>	147	67	D <sub>18</sub>
V <sub>CC5</sub>	148	68	V <sub>CC3</sub>
D <sub>17</sub>	149	69	D <sub>16</sub>
D <sub>15</sub>	150	70	D <sub>14</sub>
D <sub>13</sub>	151	71	D <sub>12</sub>
GND	152	72	GND
D <sub>11</sub>	153	73	D <sub>10</sub>
D <sub>9</sub>	154	74	D <sub>8</sub>
D <sub>7</sub>	155	75	D <sub>6</sub>
V <sub>CC5</sub>	156	76	V <sub>CC3</sub>
D <sub>5</sub>	157	77	D <sub>4</sub>
D <sub>3</sub>	158	78	D <sub>2</sub>
D <sub>1</sub>	159	79	D <sub>0</sub>
GND	160	80	GND

#### Notes:

- For the CYM74P434B and CYM74P435B TIO<sub>8</sub> and TIO<sub>9</sub> are pulled up on the module through a 8.2K $\Omega$  resistor. TIO<sub>10</sub> is pulled to ground on the module through an 8.2K $\Omega$  resistor.
- BOSEL is pulled up through a 4.7K $\Omega$  resistor on the module for backward compatible operation in systems not supporting BOSEL operation.



## Pin Definitions

Common Signals	Description
V <sub>CC5</sub>	5V Supply
V <sub>CC3</sub>	3.3V Supply
GND	Ground
A <sub>18:3</sub>	Addresses from processor
COE	Output Enable
$\overline{\text{CWE}}_{7:0}$	Byte Write Selects
$\overline{\text{BWE}}$	Byte Write Enable
$\overline{\text{GWE}}$	Global Write Enable
D <sub>63:0</sub>	Data lines from processor
TIO <sub>7:0</sub>	Tag data bits
TIO <sub>10:8</sub>	Extended cacheability tag data bits for CYM74P434B or CYM74P435B
$\overline{\text{TWE}}$	Tag Write Enable signal
ADSP	Processor Address Strobe
ADSC	Cache Controller Address Strobe
ADV	Burst Address Advance
$\overline{\text{CCS}}$	Cache Chip Select
$\overline{\text{ECS}}_1$	256-Kbyte Expansion Chip Select input pin (CYM74P430B or CYM74P434B)
$\overline{\text{ECS}}_2$	256-Kbyte Expansion Chip Select output pin (CYM74P430B or CYM74P434B)
CLK <sub>1:0</sub>	Clock signals, CLK <sub>1</sub> is not used on CYM74P430B or CYM74P434B
PD <sub>3:0</sub>	Presence Detect output pins
BOSEL	Burst Order Select. When LOW, linear burst sequence is selected. When HIGH, interleaved burst sequence is selected. If not driven (a no-connect on the motherboard) a pull-up resistor on the module will default to interleaved burst sequence.
RSVD	Reserved.
NC	Signal not connected on module.

## Presence Detect Pins

	PD <sub>3</sub>	PD <sub>2</sub>	PD <sub>1</sub>	PD <sub>0</sub>
CYM74P430B, CYM74P434B	NC	GND	NC	NC
CYM74P431B, CYM74P435B	GND	NC	GND	GND



### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Ambient Temperature  
with Power Applied .....  $-0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$

3.3V Supply Voltage to Ground Potential ....  $-0.5\text{V}$  to  $+4.6\text{V}$

5V Supply Voltage to Ground Potential .....  $-0.5\text{V}$  to  $+7.0\text{V}$

DC Voltage Applied to Outputs  
in High Z State .....  $-0.5\text{V}$  to  $+4.6\text{V}$

DC Input Voltage .....  $-0.5\text{V}$  to  $+4.6\text{V}$

Output Current into Outputs (LOW) ..... 20 mA

### Operating Range

Range	Ambient Temperature	V <sub>CC5</sub>	V <sub>CC3</sub>
Commercial	0° to 70°C	5V ± 5%	3.3V +10%–5%

### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC3</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		–0.3	0.8	V
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min. I <sub>OH</sub> = –4 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min. I <sub>OL</sub> = 8 mA		0.4	V
I <sub>CC</sub> (74P430B)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub>		750	mA
I <sub>CC</sub> (74P431B)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub>		1400	mA
I <sub>CC</sub> (74P434B)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub>		900	mA
I <sub>CC</sub> (74P435B)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub>		1550	mA

### Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM74P430BPM–50C	PM38	160-Pin Dual-Readout SIMM	256 KB	Commercial
	CYM74P431BPM–50C	PM40		512 KB	
	CYM74P434BPM–50C	PM39		256 KB extended cache	
	CYM74P435BPM–50C	PM41		512 KB extended cache	
60	CYM74P430BPM–60C	PM38	160-Pin Dual-Readout SIMM	256 KB	Commercial
	CYM74P431BPM–60C	PM40		512 KB	
	CYM74P434BPM–60C	PM39		256 KB extended cache	
	CYM74P435BPM–60C	PM41		512 KB extended cache	
66	CYM74P430BPM–66C	PM38	160-Pin Dual-Readout SIMM	256 KB	Commercial
	CYM74P431BPM–66C	PM40		512 KB	
	CYM74P434BPM–66C	PM39		256 KB extended cache	
	CYM74P435BPM–66C	PM41		512 KB extended cache	

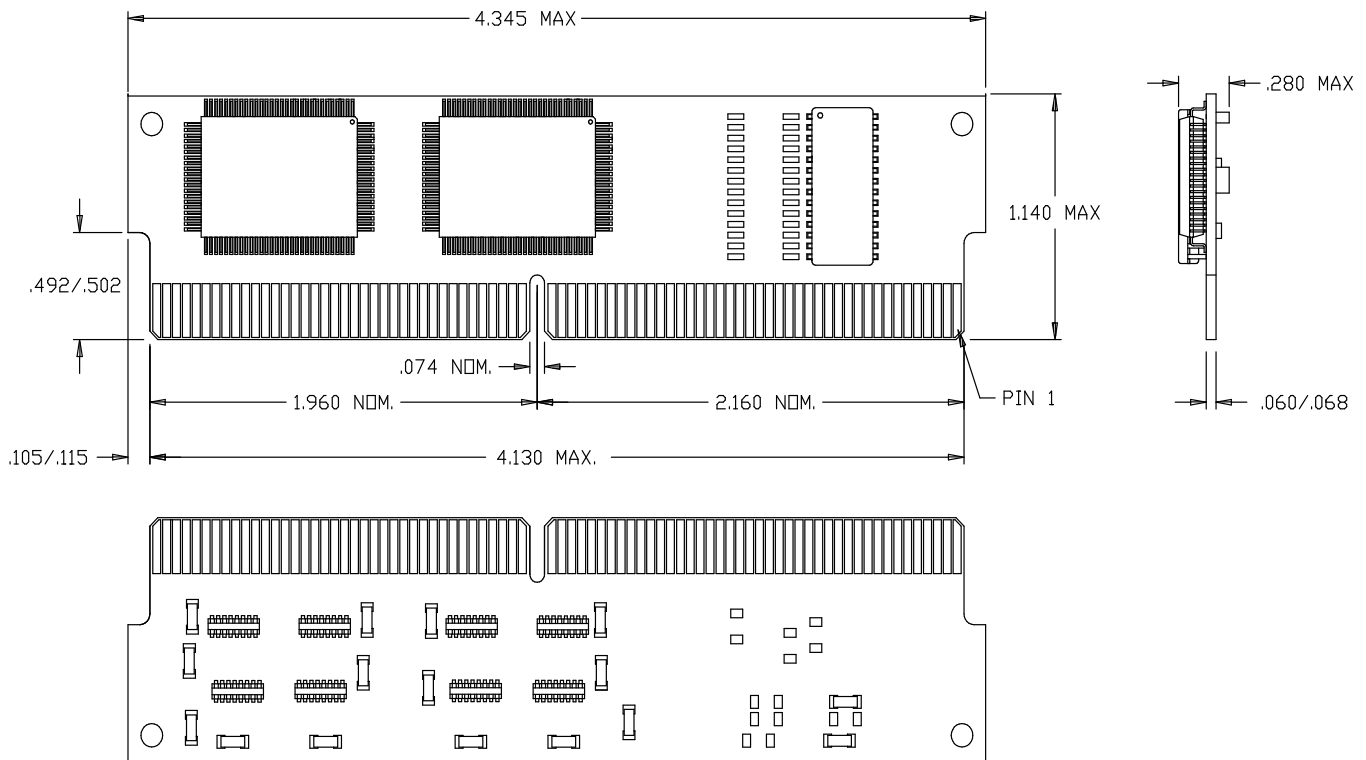


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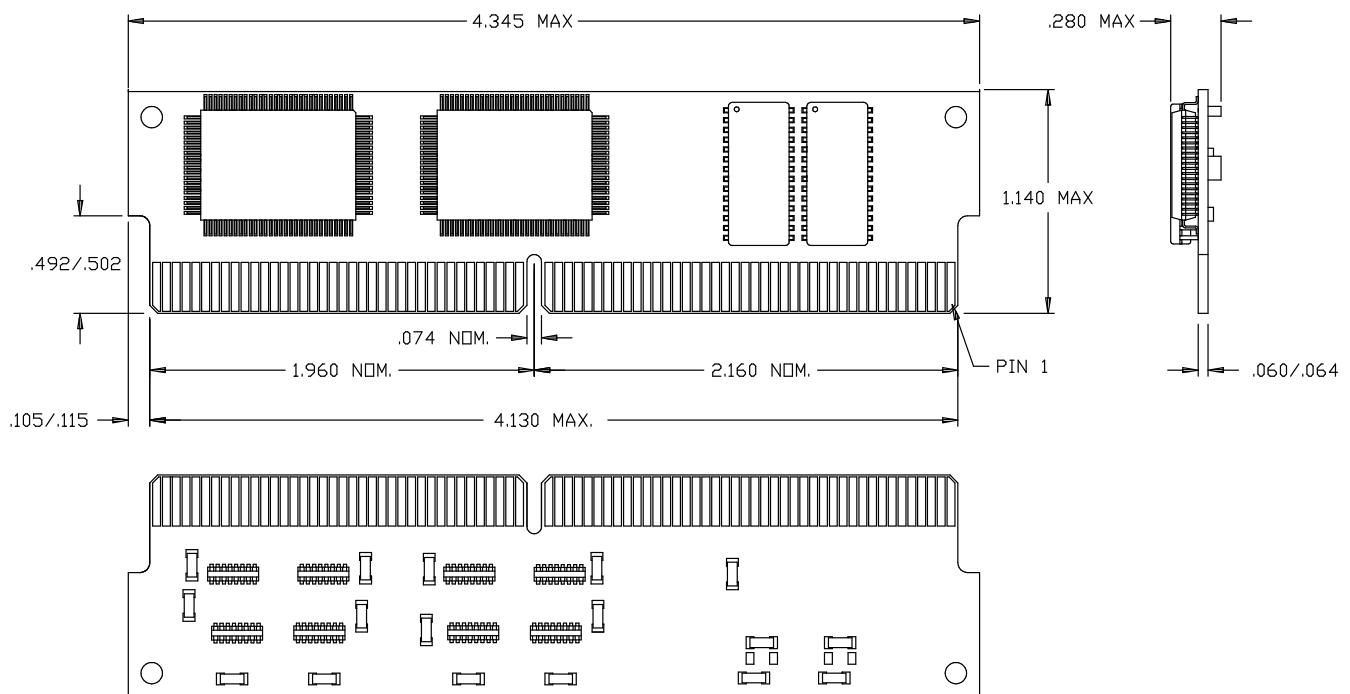
CYM74P430B, CYM74P431B  
CYM74P434B, CYM74P435B

## Package Diagrams

CYM74P430BPM in 160-pin Dual Readout SIMM PM38



CYM74P434BPM in 160-pin Dual Readout SIMM PM39



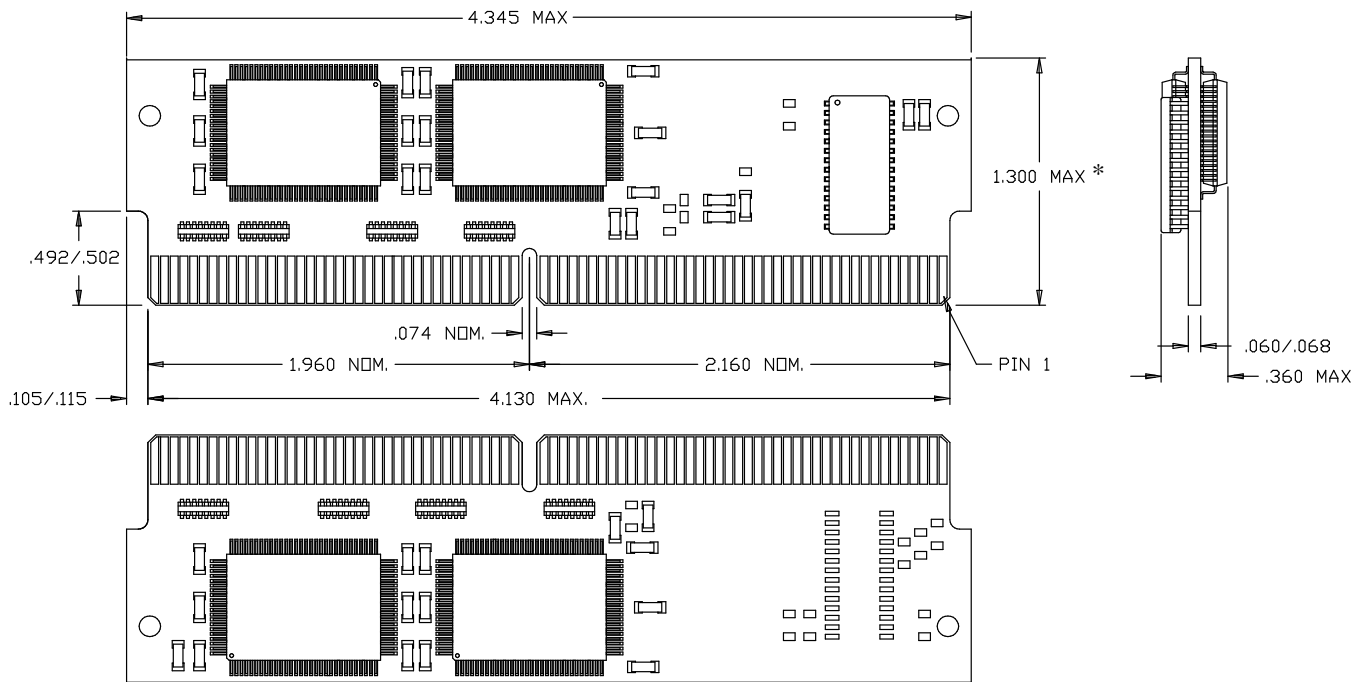


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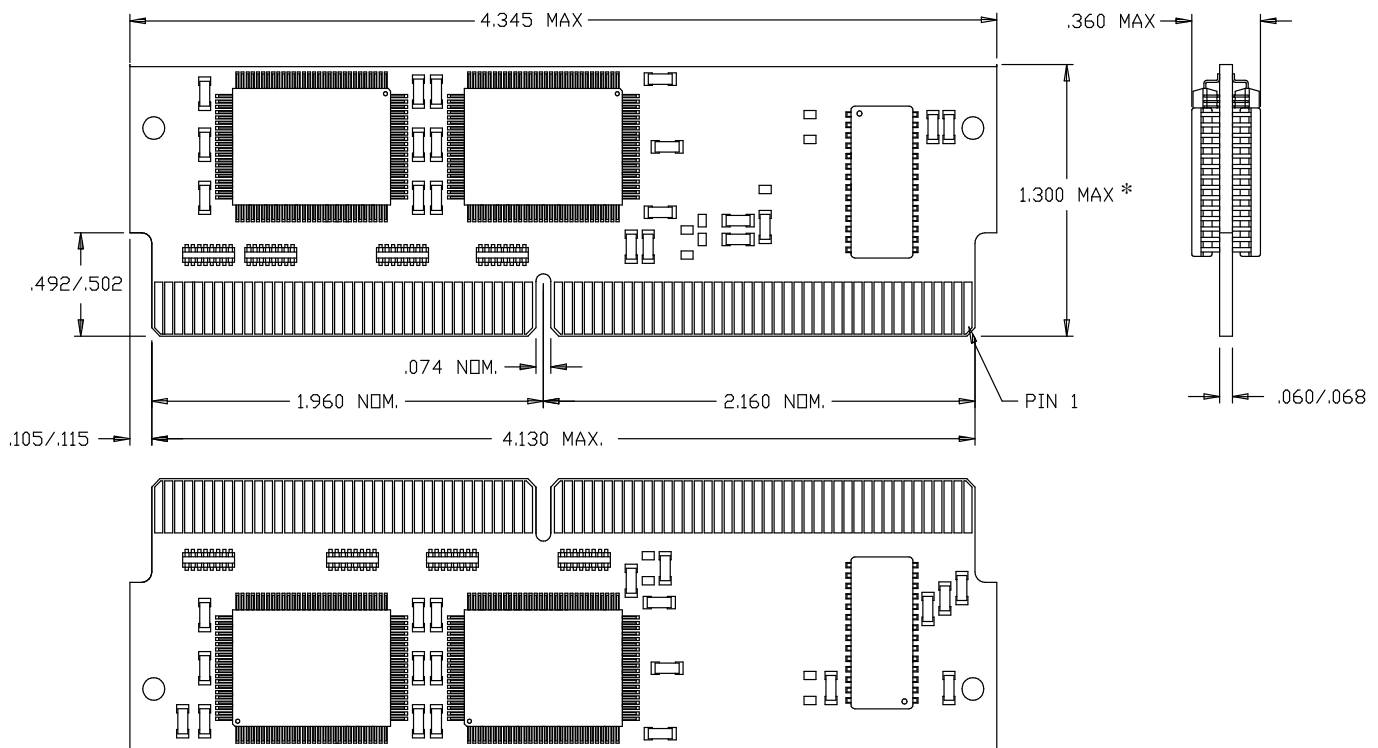
CYM74P430B, CYM74P431B  
CYM74P434B, CYM74P435B

Package Diagrams (continued)

CYM74P431BPM in 160-pin Dual Readout SIMM PM40



CYM74P435BPM in 160-pin Dual Readout SIMM PM41



\* The 512-KByte modules CYM74P431B and CYM74P435B have a 1.300 max. height vs. 1.140 for the 256-KB modules.