



CYM74A550, CYM74A551 PRELIMINARY CYM74S550, CYM74S551

OPTi Viper™ Chip Set Level II Cache Module Family

Features

- Pin-compatible secondary cache module family
- Asynchronous (CYM74A550, CYM74A551) or synchronous (CYM74S550, CYM74S551) modules with presence and configuration detect pins
- Ideal for Intel P54C-based systems with the OPTi Viper™ chipset
- Operates at 50, 60, and 66 MHz
- Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs
- 160-position Burndy DIMM CELP2X80SC3Z48 connector
- 3.3V inputs/outputs

Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the OPTi Viper chip set.

CYM74A550 and CYM74A551 are low-cost asynchronous cache modules that provide 256-Kbytes and 512-Kbytes of cache respectively. These modules offer 3-2-2-2 performance at CPU bus speeds up to 66 MHz.

The CYM74S550 and CYM74S551 are high performance synchronous cache modules that provide 256-Kbytes and 512-Kbytes of cache respectively. These modules support 3-1-1-1 performance at 66 MHz.

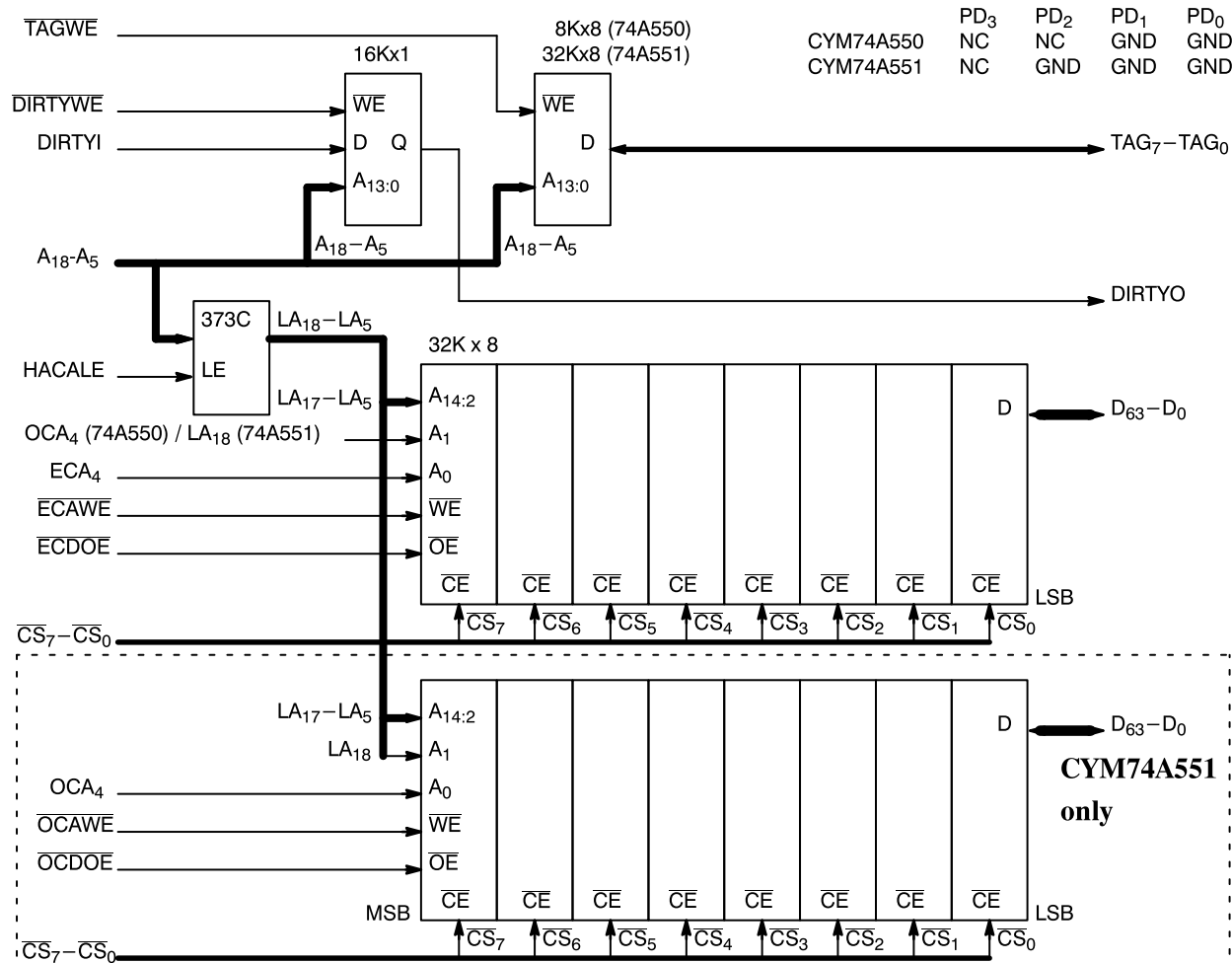
All of these modules include storage for 8 bits of tag and one dirty bit.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. All inputs and outputs of this family of modules are (3.3V) TTL compatible. Provisions are made on-board to support both mixed-mode (5V/3.3V) and 3.3V-only SRAMs. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

Logic Block Diagram – CYM74A550, CYM74A551

Note: A₁₈ is not used by CYM74A550

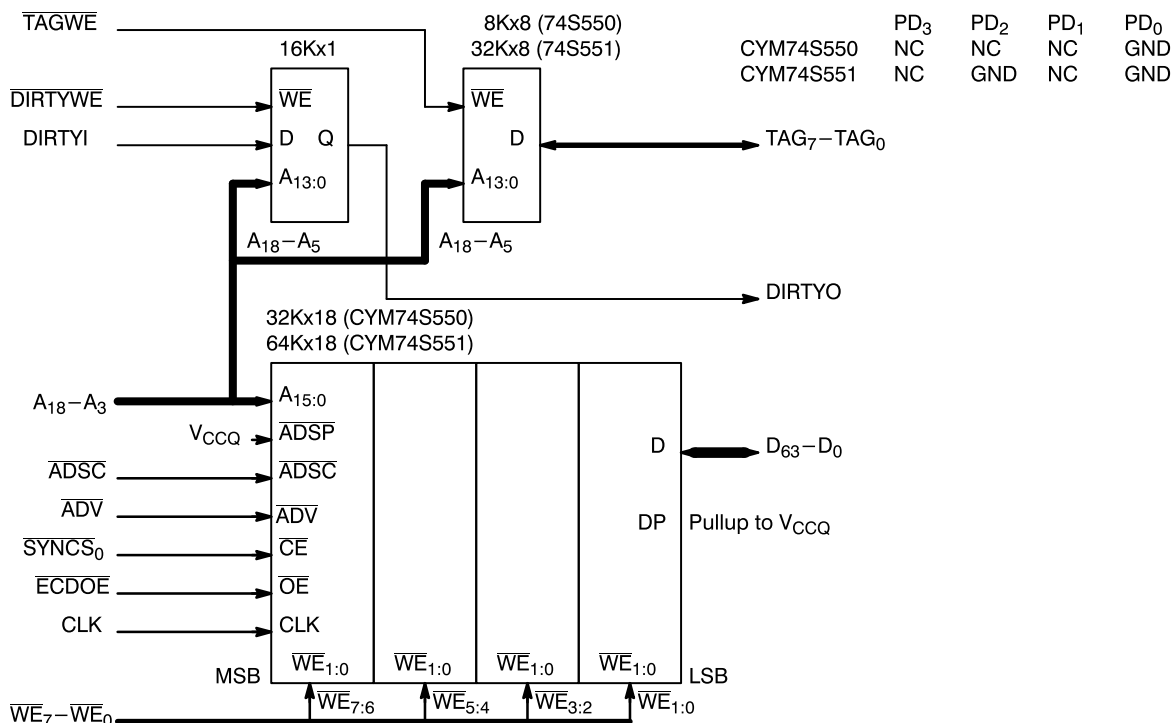


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Logic Block Diagram – CYM74S550, CYM74S551

Note: A₁₈ is not used by CYM74S550



Selection Guide

Asynchronous Cache Modules						
Part Number	74A550-50	74A550-60	74A550-66	74A551-50	74A551-60	74A551-66
Cache Size	256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66
Data t _{AA}	25 ns	15 ns	15 ns	25 ns	15 ns	15 ns
Tag t _{AA}	20 ns	15 ns	12 ns	20 ns	15 ns	12 ns

Synchronous Cache Modules						
Part Number	74S550-50	74S550-60	74S550-66	74S551-50	74S551-60	74S551-66
Cache Size	256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66
Data t _{CDV}	12 ns	9 ns	9 ns	12 ns	9 ns	9 ns
Tag t _{AA}	20 ns	15 ns	12 ns	20 ns	15 ns	12 ns



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Pin Configuration

Dual Read-Out SIMM (DIMM)

Top View

GND	81	1	GND
D ₆₃	82	2	D ₆₂
D ₆₁	83	3	D ₆₀
V _{CC}	84	4	V _{CCQ}
D ₅₉	85	5	D ₅₈
D ₅₇	86	6	D ₅₆
D ₅₅	87	7	D ₅₄
GND	88	8	GND
D ₅₃	89	9	D ₅₂
D ₅₁	90	10	D ₅₀
D ₄₉	91	11	D ₄₈
V _{CC}	92	12	V _{CCQ}
D ₄₇	93	13	D ₄₆
D ₄₅	94	14	D ₄₄
GND	95	15	GND
D ₄₃	96	16	D ₄₂
D ₄₁	97	17	D ₄₀
D ₃₉	98	18	D ₃₈
D ₃₇	99	19	D ₃₆
GND	100	20	GND
D ₃₅	101	21	D ₃₄
D ₃₃	102	22	D ₃₂
D ₃₁	103	23	D ₃₀
D ₂₉	104	24	D ₂₈
GND	105	25	GND
D ₂₇	106	26	D ₂₆
D ₂₅	107	27	D ₂₄
V _{CC}	108	28	V _{CCQ}
D ₂₃	109	29	D ₂₂
D ₂₁	110	30	D ₂₀
D ₁₉	111	31	D ₁₈
GND	112	32	GND
D ₁₇	113	33	D ₁₆
D ₁₅	114	34	D ₁₄
D ₁₃	115	35	D ₁₂
GND	116	36	GND
D ₁₁	117	37	D ₁₀
V _{CC}	118	38	V _{CCQ}
D ₉	119	39	D ₈
D ₇	120	40	D ₆
GND	121	41	GND
D ₅	122	42	D ₄
V _{CC}	123	43	V _{CCQ}
D ₃	124	44	D ₂
D ₁	125	45	D ₀
V _{CC}	126	46	V _{CCQ}
(74S55X) \overline{ADSC} / (74A55X) ECA ₄	127	47	OCA ₄ (74A55X) / \overline{ADV} (74S55X)
(74S55X) SYNC ₀ / (74A55X) ECAWE	128	48	OCAWE (74A55X) / SYNC ₁ (74S55X)
ECDOE	129	49	OCDOE
(74S55X) \overline{WE}_0 / (74A55X) CS ₀	130	50	CS ₁ (74A55X) / \overline{WE}_1 (74S55X)
GND	131	51	GND
(74S55X) \overline{WE}_2 / (74A55X) CS ₂	132	52	CS ₃ (74A55X) / \overline{WE}_3 (74S55X)
(74S55X) \overline{WE}_4 / (74A55X) CS ₄	133	53	CS ₅ (74A55X) / \overline{WE}_5 (74S55X)
V _{CC}	134	54	V _{CCQ}
(74S55X) \overline{WE}_6 / (74A55X) CS ₆	135	55	CS ₇ (74A55X) / \overline{WE}_7 (74S55X)
(74S55X) CLK / (74A55X) NC	136	56	HACALE (74A55X) / NC (74S55X)
GND	137	57	GND
DIRTYWE	138	58	TAGWE
(74S55X) A ₃ / (74A55X) NC	139	59	NC (74A55X) / A ₄ (74S55X)
A ₅	140	60	A ₆
A ₇	141	61	A ₈
GND	142	62	GND
A ₉	143	63	A ₁₀
A ₁₁	144	64	A ₁₂
A ₁₃	145	65	A ₁₄
V _{CC}	146	66	V _{CCQ}
A ₁₅	147	67	A ₁₆
A ₁₇	148	68	NC (74A55X) / A ₁₈ (74S55X)
(Reserved A ₁₉) NC	149	69	NC (Reserved A ₂₀)
GND	150	70	GND
DIRTYI	151	71	DIRTYO
TAG ₀	152	72	TAG ₁
V _{CC}	153	73	V _{CCQ}
TAG ₂	154	74	TAG ₃
TAG ₄	155	75	TAG ₅
GND	156	76	GND
TAG ₆	157	77	TAG ₇
PD ₀	158	78	PD ₁
PD ₂	159	79	PD ₃
V _{CC}	160	80	V _{CCQ}



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Pin Definitions

Common Signals	Description
V _{CC}	5V Supply
V _{CCQ}	3.3V Supply
GND	Ground
A ₁₈ –A ₅	Addresses from processor
D ₆₃ –D ₀	64-bit Data bus from processor
$\overline{\text{ECDOE}}$	Even bank output enable input
TAG ₇ –TAG ₀	8-bit Tag RAM bidirectional bus
$\overline{\text{TAGWE}}$	Tag RAM write enable input
DIRTYI	1-bit Dirty RAM input
DIRTYO	1-bit Dirty RAM output
$\overline{\text{DIRTYWE}}$	Dirty RAM write enable input
PD ₃ –PD ₀	Presence Detect pins
NC	Signal not connected on module.
CYM74A55X Only Signals	Description
HACALE	Address Latch Enable input to transparent address latches
OCA ₄	Address bit A ₃ in single bank async cache module (CYM74A550) Address bit A ₄ of odd bank in two bank async cache module (CYM74A551)
ECA ₄	Address bit A ₄ in single bank async cache module (CYM74A550) Address bit A ₄ of even bank in two bank async cache module (CYM74A551)
$\overline{\text{CS}}_7$ – $\overline{\text{CS}}_0$	Data RAM Chip Select inputs
$\overline{\text{ECAWE}}$	Even bank write enable input
$\overline{\text{OCAWE}}$	Odd bank write enable input (CYM74A551 only)
CYM74S55X Only Signals	Description
CLK	Clock input
A ₄ –A ₃	Lower order address bits from processor
$\overline{\text{ADSC}}$	Cache Controller Address Strobe input
$\overline{\text{ADV}}$	Burst Address Advance input
$\overline{\text{SYNCS}}_0$	Even bank synchronous burst RAM chip select input
$\overline{\text{SYNCS}}_1$	Odd bank synchronous burst RAM chip select input (not used)
WE ₇ –WE ₀	Write enable inputs to Data RAMs



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to $+125^{\circ}\text{C}$
Ambient Temperature
with Power Applied -0°C to $+70^{\circ}\text{C}$
3.3V Supply Voltage to Ground Potential -0.5V to $+4.6\text{V}$
5V Supply Voltage to Ground Potential -0.5V to $+5.25\text{V}$
DC Voltage Applied to Outputs
in High Z State -0.5V to $+4.6\text{V}$

DC Input Voltage -0.5V to $+4.6\text{V}$
Output Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 5\%$ $3.3\text{V} \pm 5\%$

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V _{IH}	Input HIGH Voltage		2.2	V _{CCQ} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	V
V _{OH}	Output HIGH Voltage	V _{CC} =Min. I _{OH} = -4 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} =Min. I _{OL} = 8 mA		0.4	V
I _{CC} (74A550)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1500	mA
I _{CC} (74A551)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		2700	mA
I _{CC} (74S550)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1500	mA
I _{CC} (74S551)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1500	mA

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM74A550PM-50C	PM31	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74A551PM-50C	PM32		Async 512 KB	
	CYM74S550PM-50C	PM33		Sync 256 KB	
	CYM74S551PM-50C	PM33		Sync 512 KB	
60	CYM74A550PM-60C	PM31	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74A551PM-60C	PM32		Async 512 KB	
	CYM74S550PM-60C	PM33		Sync 256 KB	
	CYM74S551PM-60C	PM33		Sync 512 KB	
66	CYM74A550PM-66C	PM31	160-Pin Dual-Readout SIMM	Async 256 KB	Commercial
	CYM74A551PM-66C	PM32		Async 512 KB	
	CYM74S550PM-66C	PM33		Sync 256 KB	
	CYM74S551PM-66C	PM33		Sync 512 KB	

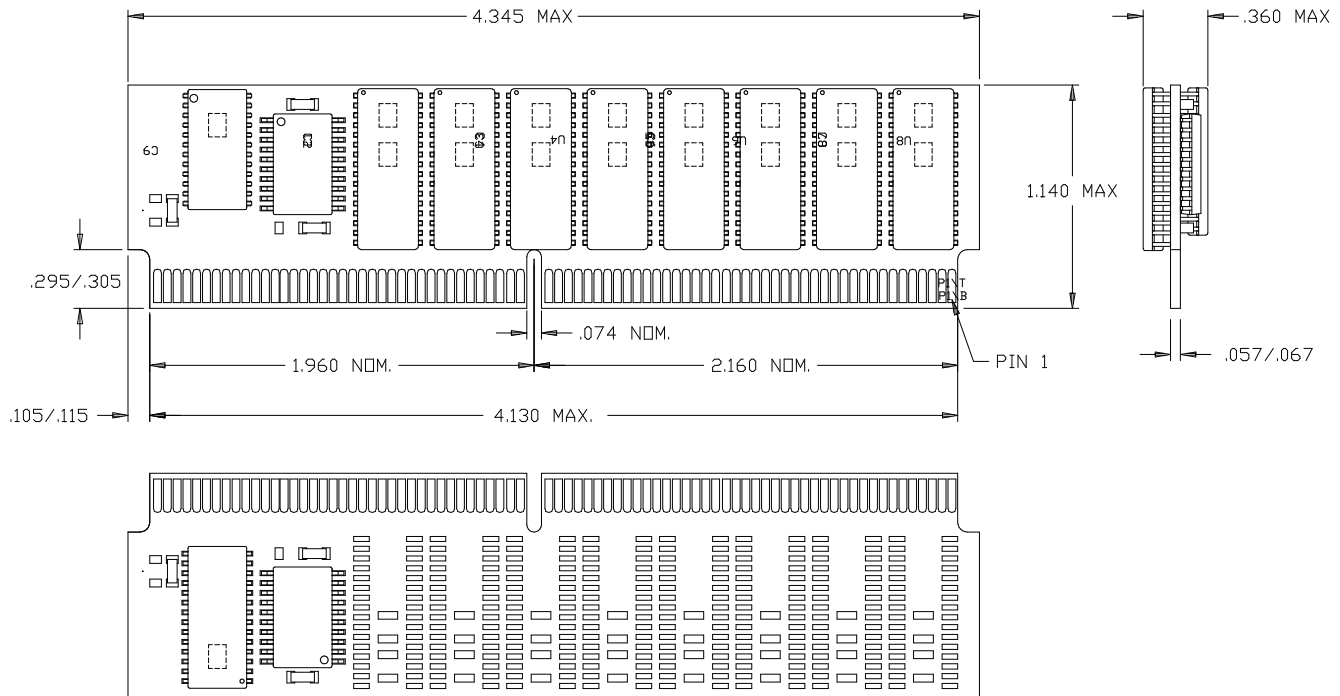
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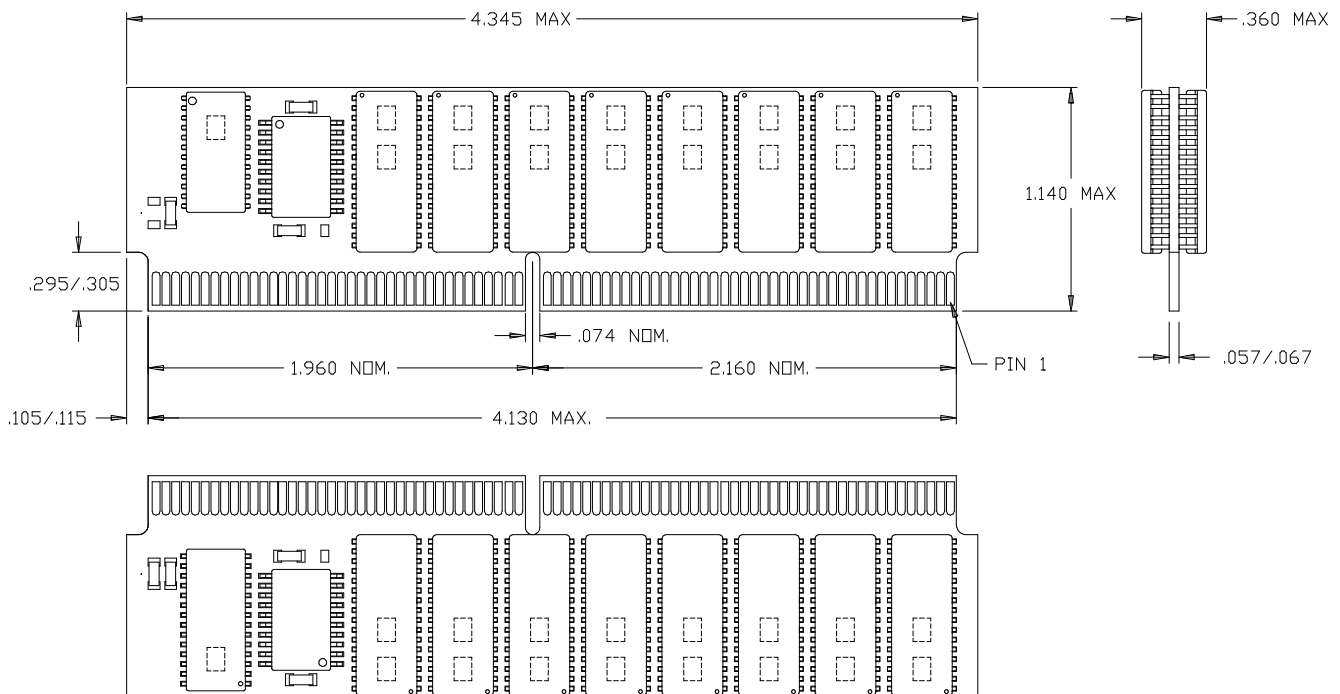
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Package Diagrams

160-Pin Dual Readout SIMM PM31



160-Pin Dual Readout SIMM PM32





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Package Diagrams (continued)

160-Pin Dual Readout SIMM PM33

