PRELIMINARY

CYM9230
CYM9231

82420 PCIset-Compatible Level II Cache Modules

Features

- **128K-byte (CYM9230) or 256K-byte (CYM9231) cache moducle organized as 32K by 32 or 64K by 32**
- **Tag width of 9 bits plus valid bit**
- **Independent dirty bit**
- **Operates with systems based on the Intel™ 82420 core logic**
- **Zero-wait state operation at 33 Mhz**
- **Constructed using sandard asynchronous SRAMs**
- **112-pin Burndy Connector, Part Number CELP2X56SC3Z48**
- **Single 5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

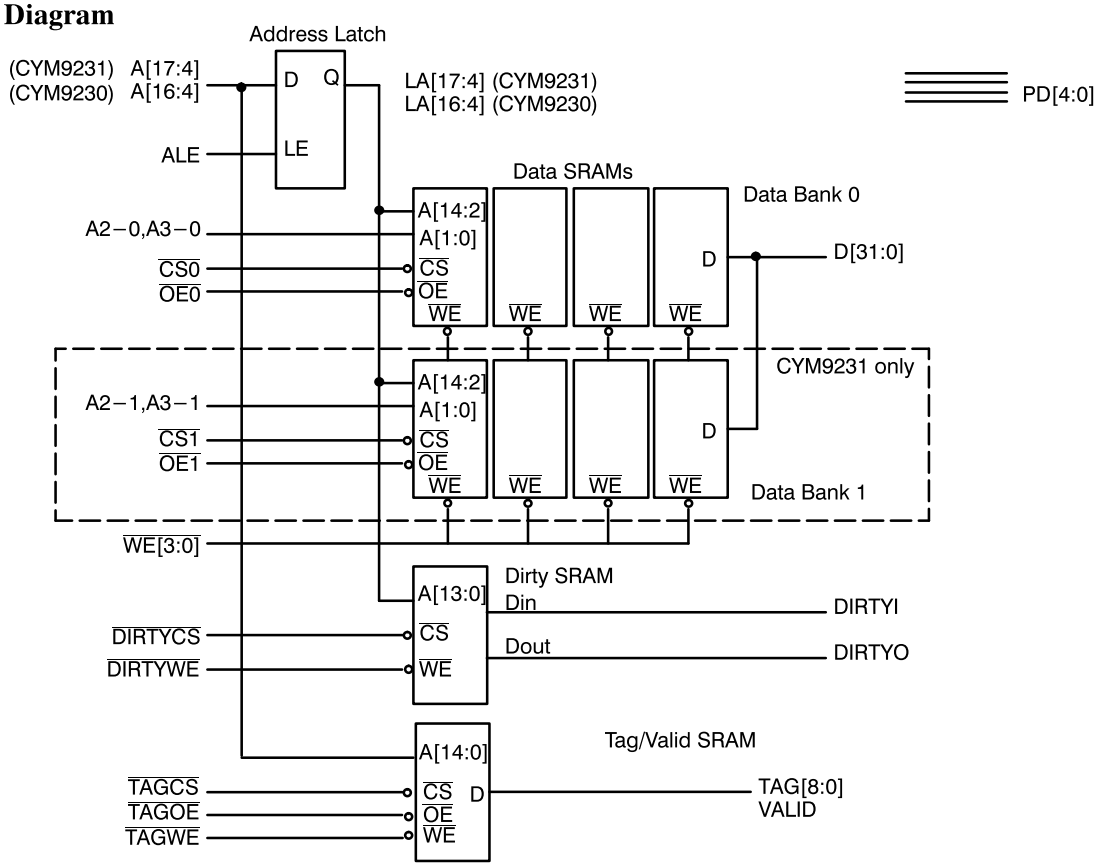
Functional Description

The CYM9230 module series is a family of cache memory subsystems for Intel 486-based systems. The CYM9230 (128Kbytes) contains one memory bank organized as 32K by 32. The CYM9231 (256Kbytes) contains two banks for interleaved operation. In addition, each module contains two SRAMs, supporting a 9-bit tag and valid bit, and a single-bit, separate I/O SRAM supporting a dirty bit. The address signals for the Data and Dirty SRAMs are latched.

These modules are designed for zero wait state operation in 486-based systems operating at a bus speed of 33 Mhz. They are designed for compatibility with the Intel 82420 PCIset and other chip sets. The baseline speed grade is built using 12 nanosecond Tag SRAMs and 20 nanosecond Data SRAMs.

The modules are configured as a 112-pin card-edge memory module. It is constructed using standard asynchronous SRAMs in SOJ packages mounted on an epoxy laminate substrate. The module dimensions are 3.145 inches long by 1.105 inches high by 0.365 inches thick.

Logic Block Diagram



Selection Guide

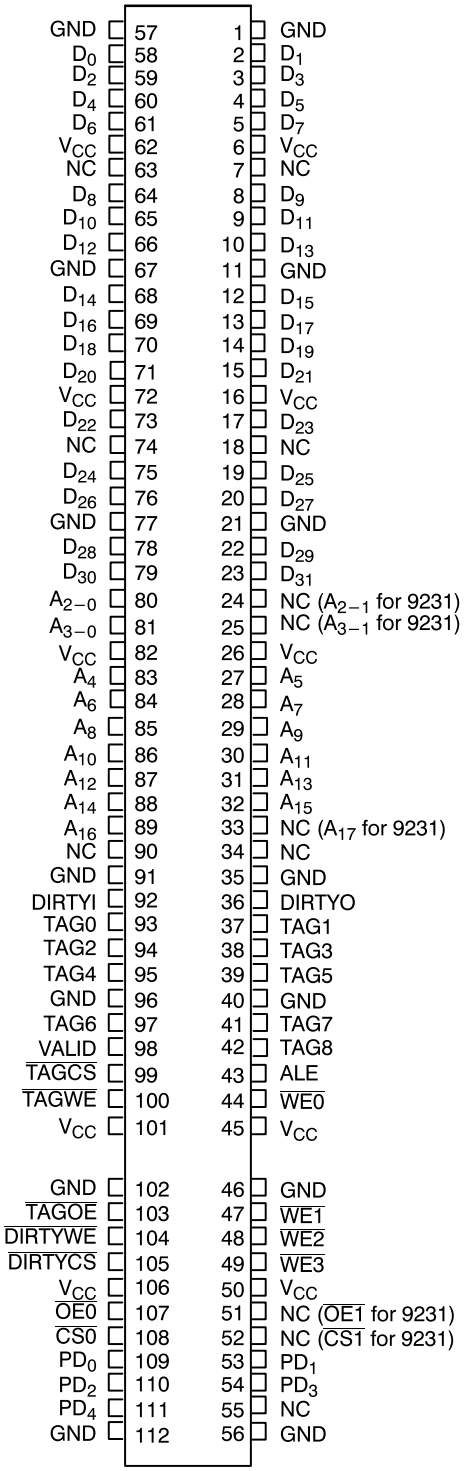
	CYM9230PB−20	CYM9231PB−20
Cache Size (KB)	128	256
Data SRAM (ns)	20	20
Dirty SRAM (ns)	15	15
Tag/Valid SRAM (ns)	12	12

Intel is a trademark of Intel Corporation.

Pin Configuration

Dual Read-out SIMM

Top View



9230-2

Pin Descriptions

Name	Description
A[18:4]	Host Address Bus
A3−A0	Host Address Bit 3, Bank 0
A2−A0	Host Address Bit 2, Bank 0
D[31:0]	Host Data Bus
$\overline{CS0}$	Bank 0 Chip Set
$\overline{WE}$[3:0]	Cache Byte Write Enables
$\overline{OE0}$	Bank 0 Output Enable
ALE	Address Latch Enable
TAG[7:0]	Tag Data Bus
VALID	Valid Bit
$\overline{TAGCS}$	Tag Chip Select
$\overline{TAGOE}$	Tag Output Enable
$\overline{TAGWE}$	Tag Write Enable
DIRTYI	Dirty Bit Input
DIRTYO	Dirty Bit Output
$\overline{DIRTYCS}$	Dirty Chip Select
$\overline{DIRTYWE}$	Dirty Write Enable
PD[4:0]	Presence Detect Output Pins
NC	No Connection
A3−A1	Host Address Bit 3, Bank 1
A2−A1	Host Address Bit 2, Bank 1
$\overline{CS1}$	Bank 1 Chip Select
$\overline{OE1}$	Bank 1 Output Enable

Presence Detect Table

	PD_4	PD_3	PD_2	PD_1	PD_0
CYM9230	V_{CC}	NC	V_{CC}	NC	V_{CC}
CYM9231	V_{CC}	NC	V_{CC}	V_{CC}	NC

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Static Discharge Voltage ..... >2001V

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

Electrical Characteristics Over the Operating Range[12]

Parameter	Description	Test Conditions	CYM9230 CYM9231		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{CC}	V_{CC} Operating Supply Current (CYM9230 only).	V_{CC} = Max., I_{OUT} = 0 mA f=fmax = $1/t_{RC}$		1050	mA
I_{CC}	V_{CC} Operating Supply Current (CYM9231 only).	V_{CC} = Max., I_{OUT} = 0 mA f=fmax = $1/t_{RC}$		1800	mA

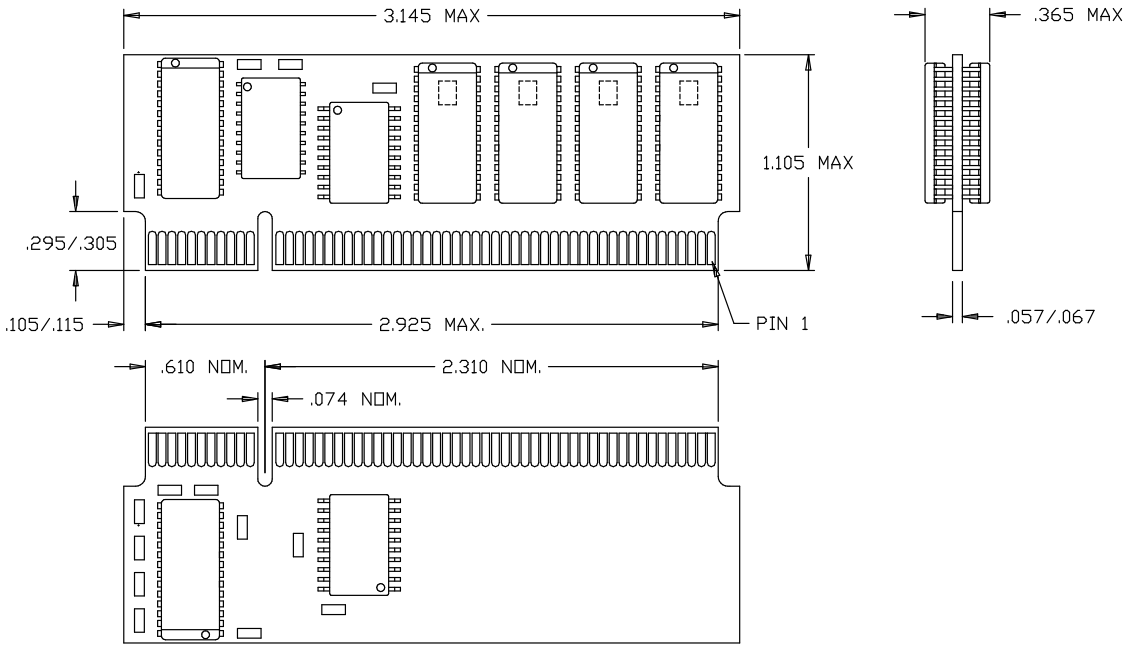
Ordering Information

Cache Memory Size	Ordering Code	Package Type	Package Name	Operating Range
128K	CYM9230PB-20C	PM15	112-Pin Dual-Readout SIMM	Commercial
256K	CYM9231PB-20C	PM16	112-Pin Dual-Readout SIMM	Commercial

Document #: 38−M−00064

Package Diagram

112-Pin Dual-Readout SIMM PM15



112-Pin Dual-Readout SIMM PM16