

## 256K x 4 Static RAM with Separate I/O

### Features

- **High speed**  
—  $t_{AA} = 12$  ns
- **Transparent write (7C101A)**
- **CMOS for optimum speed/power**
- **Low active power**  
— 910 mW
- **Low standby power**  
— 275 mW
- **2.0V data retention (optional)**  
— 100  $\mu$ W
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

### Functional Description

The CY7C101A and CY7C102A are high-performance CMOS static RAMs organized as 262,144 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ( $\overline{CE}$ ) and three-state drivers. Both devices have an automatic power-down feature, reducing the power consumption by more than 65% when deselected.

Writing to the device is accomplished by taking both chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs LOW. Data on the four input pins ( $I_0$  through  $I_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{17}$ ).

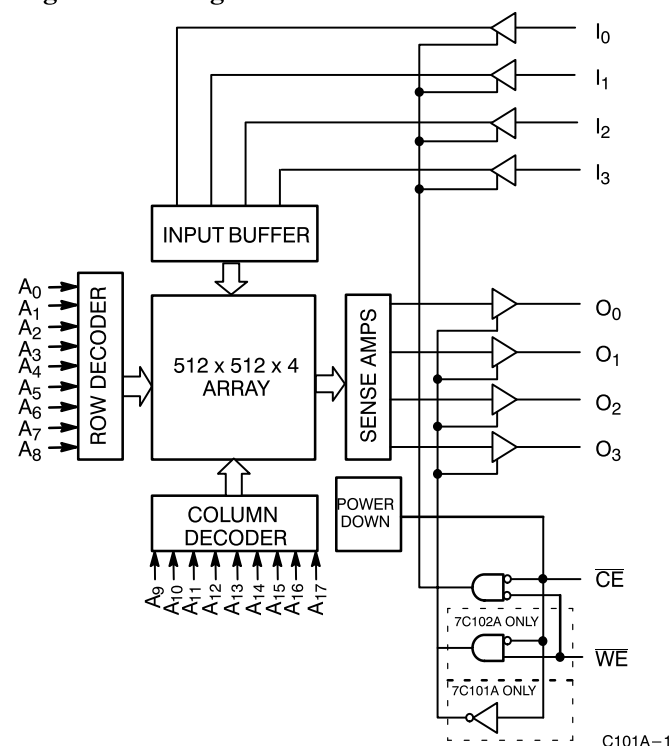
Reading the device is accomplished by taking chip enable ( $\overline{CE}$ ) LOW while write en-

able ( $\overline{WE}$ ) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins ( $O_0$  through  $O_3$ ).

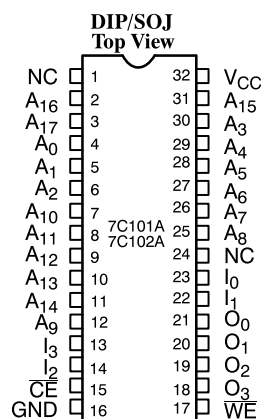
The data output pins on the CY7C101A and the CY7C102A are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH). The CY7C102A's outputs are also placed in a high-impedance state during a write operation ( $\overline{CE}$  and  $\overline{WE}$  LOW). In a write operation on the CY7C101A, the output pins will carry the same data as the inputs after a specified delay.

The CY7C101A and CY7C102A are available in standard 400-mil-wide DIPs and SOJs.

### Logic Block Diagram



### Pin Configuration



C101A-2

### Selection Guide

		7C101A-12 7C102A-12	7C101A-15 7C102A-15	7C101A-20 7C102A-20	7C101A-25 7C102A-25	7C101A-35 7C102A-35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)	Commercial	165	155	140	130	125
	Military		165	150	140	135
Maximum Standby Current (mA)	Commercial	50	40	30	30	25
	Military		40	30	30	25



### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$   
 Ambient Temperature with  
 Power Applied .....  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
 Supply Voltage on  $V_{CC}$  Relative to GND<sup>[1]</sup> .  $-0.5\text{V}$  to  $+7.0\text{V}$   
 DC Voltage Applied to Outputs  
 in High Z State<sup>[1]</sup> .....  $-0.5\text{V}$  to  $V_{CC} + 0.5\text{V}$   
 DC Input Voltage<sup>[1]</sup> .....  $-0.5\text{V}$  to  $V_{CC} + 0.5\text{V}$   
 Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage .....  $>2001\text{V}$   
 (per MIL-STD-883, Method 3015)

Latch-Up Current .....  $>200\text{ mA}$

### Operating Range

Range	Ambient Temperature	$V_{CC}$
Commercial	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$
Military <sup>[2]</sup>	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	$5\text{V} \pm 10\%$

#### Notes:

- $V_{IL}$  (min.) =  $-2.0\text{V}$  for pulse durations of less than 20 ns.
- $T_A$  is the “instant on” case temperature.

### Electrical Characteristics Over the Operating Range<sup>[3]</sup>

Parameter	Description	Test Conditions	7C101A–12 7C102A–12		7C101A–15 7C102A–15		7C101A–20 7C102A–20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0\text{ mA}$	2.4		2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0\text{ mA}$		0.4		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>[1]</sup>		$-0.3$	0.8	$-0.3$	0.8	$-0.3$	0.8	V
$I_{IX}$	Input Load Current	$\text{GND} \leq V_I \leq V_{CC}$	$-1$	$+1$	$-1$	$+1$	$-1$	$+1$	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$\text{GND} \leq V_I \leq V_{CC},$ Output Disabled	$-5$	$+5$	$-5$	$+5$	$-5$	$+5$	$\mu\text{A}$
$I_{OS}$	Output Short Circuit Current <sup>[4]</sup>	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}$		$-300$		$-300$		$-300$	mA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.},$ $I_{OUT} = 0\text{ mA},$ $f = f_{\text{MAX}} = 1/t_{\text{RC}}$	Com'l	165		155		140	mA
			Mil			165		150	
$I_{SB1}$	Automatic CE Power-Down Current — TTL Inputs	Max. $V_{CC},$ $\overline{\text{CE}} \geq V_{IH},$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{\text{MAX}}$	Com'l	50		40		30	mA
			Mil			40		30	
$I_{SB2}$	Automatic CE Power-Down Current — CMOS Inputs	Max. $V_{CC},$ $\overline{\text{CE}} \geq V_{CC} - 0.3\text{V},$ $V_{IN} \geq V_{CC} - 0.3\text{V}$ or $V_{IN} \leq 0.3\text{V}, f = 0$	Com'l	2		2		2	mA
			Mil			2		2	



**Electrical Characteristics** Over the Operating Range<sup>[3]</sup> (continued)

Parameter	Description	Test Conditions	7C101A-25 7C102A-25		7C101A-35 7C102A-35		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[NO TAG]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com'l	130		125	mA
			Mil	140		135	
I <sub>SB1</sub>	Automatic CE Power-Down Current — TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Com'l	30		25	mA
			Mil	30		25	
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l	2		2	mA
			Mil	2		2	

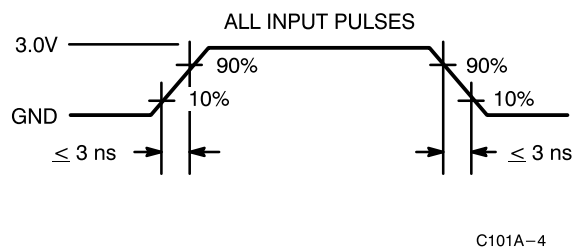
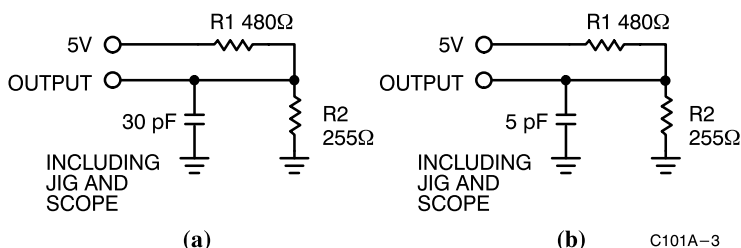
**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub> : Addresses	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	7	pF
C <sub>IN</sub> : Controls			10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**Notes:**

- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

**AC Test Loads and Waveforms**



Equivalent to: THÉVENIN EQUIVALENT

OUTPUT — 167Ω — 1.73V



**Switching Characteristics** Over the Operating Range<sup>[3, 6]</sup>

Parameter	Description	7C101A–12 7C102A–12		7C101A–15 7C102A–15		7C101A–20 7C102A–20		7C101A–25 7C102A–25		7C101A–35 7C102A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t <sub>RC</sub>	Read Cycle Time	12		15		20		25		35		ns
t <sub>AA</sub>	Address to Data Valid		12		15		20		25		35	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		3		3		ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to Data Valid		12		15		20		25		35	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to Low Z <sup>[7]</sup>	3		3		3		3		3		ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to High Z <sup>[7, 8]</sup>		6		7		8		10		10	ns
t <sub>PU</sub>	$\overline{\text{CE}}$ LOW to Power-Up	0		0		0		0		0		ns
t <sub>PD</sub>	$\overline{\text{CE}}$ HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE <sup>[9]</sup>												
t <sub>WC</sub>	Write Cycle Time	12		15		20		25		35		ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to Write End	10		12		15		20		25		ns
t <sub>AW</sub>	Address Set-Up to Write End	10		12		15		20		25		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		0		ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	10		12		15		20		25		ns
t <sub>SD</sub>	Data Set-Up to Write End	7		8		10		15		20		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		0		ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to Low Z <sup>[7]</sup>	3		3		3		3		3		ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to High Z <sup>[7, 8]</sup>		6		7		8		10		10	ns
t <sub>DWE</sub>	$\overline{\text{WE}}$ LOW to Data Valid (7C101A)		12		15		20		25		35	ns
t <sub>DCE</sub>	$\overline{\text{CE}}$ LOW to Data Valid (7C101A)		12		15		20		25		35	ns
t <sub>ADV</sub>	Data Valid to Output Valid (7C101A)		12		15		20		25		35	ns

**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.



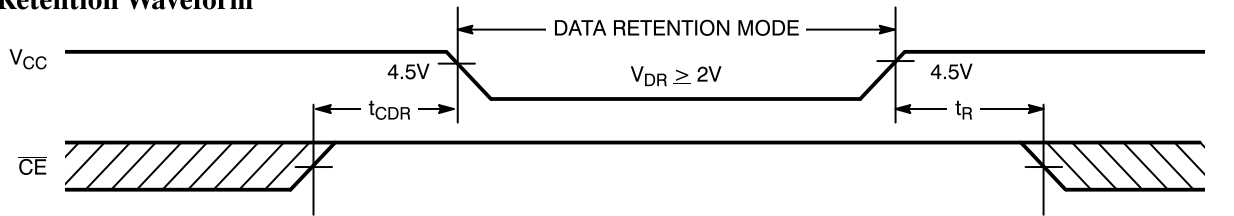
**Data Retention Characteristics** Over the Operating Range (L Version Only)

Parameter	Description	Conditions <sup>[10]</sup>	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V <sub>DR</sub>	V <sub>CC</sub> for Retention Data		2.0		2.0		V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = V <sub>DR</sub> = 2.0V, CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 or V <sub>IN</sub> ≤ 0.3V		50		70	μA
t <sub>CDR</sub> <sup>[5]</sup>	Chip Deselect to Data Retention Time		0		0		ns
t <sub>R</sub> <sup>[5]</sup>	Operation Recovery Time		t <sub>RC</sub>		t <sub>RC</sub>		ns

**Note:**

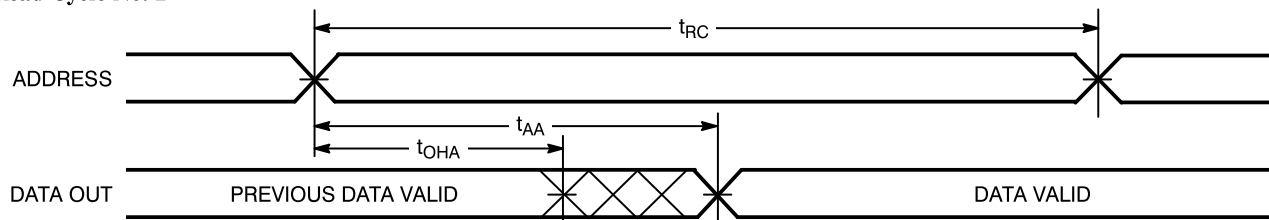
10. No input may exceed V<sub>CC</sub> + 0.5V.

**Data Retention Waveform**

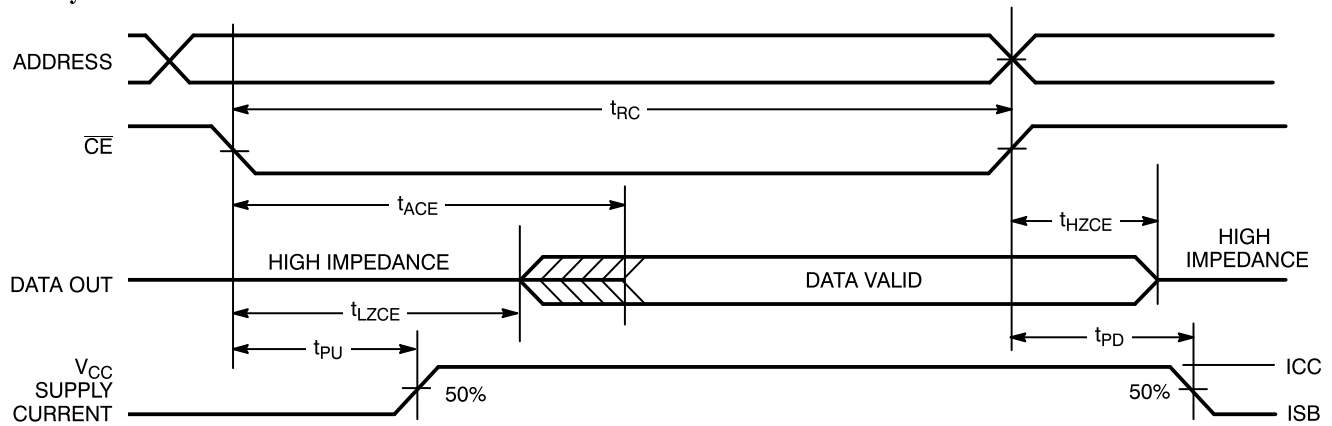


**Switching Waveforms**

**Read Cycle No. 1<sup>[11, 12]</sup>**



**Read Cycle No. 2<sup>[12, 13]</sup>**



**Notes:**

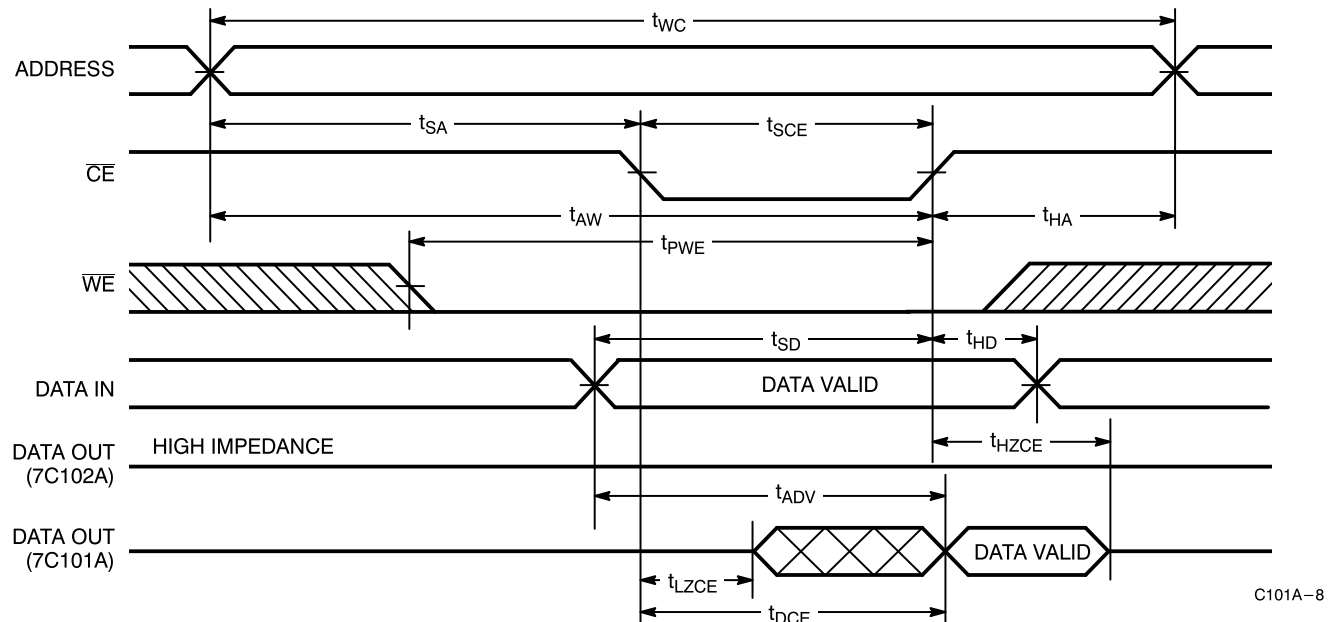
11. Device is continuously selected, CE = V<sub>IL</sub>.  
12. WE is HIGH for read cycle.

13. Address valid prior to or coincident with CE transition LOW.

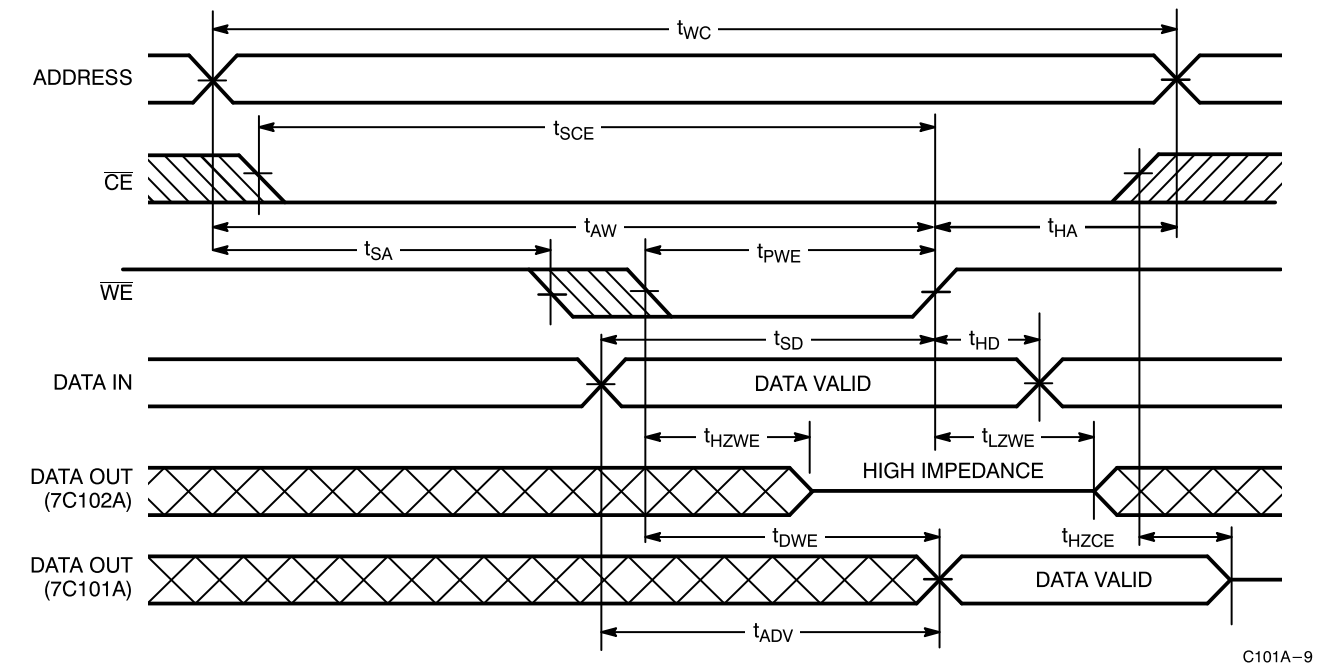


# Switching Waveforms (continued)

## Write Cycle No. 1 ( $\overline{CE}$ Controlled)<sup>[9, 14]</sup>



## Write Cycle No. 2 ( $\overline{WE}$ Controlled)<sup>[9]</sup>



### Note:

14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state (7C102A only).



### Truth Table

$\overline{CE}$	$\overline{WE}$	$O_0 - O_3$	Mode	Power
H	X	High Z	Power-Down	Standby ( $I_{SB}$ )
L	H	Data Out	Read	Active ( $I_{CC}$ )
L	L	High Z	7C102A: Standard Write	Active ( $I_{CC}$ )
L	L	Input Tracking	7C101A: Transparent Write <sup>[15]</sup>	Active ( $I_{CC}$ )

**Note:**

15. Outputs track inputs after specified delay.

### Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C101A–12PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C101A–15PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–15VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–15DMB	D44	32-Lead (400-Mil) CerDIP	Military
20	CY7C101A–20PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–20VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–20DMB	D44	32-Lead (400-Mil) CerDIP	Military
25	CY7C101A–25PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–25VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–25DMB	D44	32-Lead (400-Mil) CerDIP	Military
35	CY7C101A–35PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–35VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–35DMB	D44	32-Lead (400-Mil) CerDIP	Military

Contact factory for “L” version availability.

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C102A–12PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C102A–15PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–15VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–15DMB	D44	32-Lead (400-Mil) CerDIP	Military
20	CY7C102A–20PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–20VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–20DMB	D44	32-Lead (400-Mil) CerDIP	Military
25	CY7C102A–25PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–25VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–25DMB	D44	32-Lead (400-Mil) CerDIP	Military
35	CY7C102A–35PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–35VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–35DMB	D44	32-Lead (400-Mil) CerDIP	Military

Contact factory for “L” version availability.



## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

Parameter	Subgroups
V <sub>OH</sub>	1, 2, 3
V <sub>OL</sub>	1, 2, 3
V <sub>IH</sub>	1, 2, 3
V <sub>IL</sub> Max.	1, 2, 3
I <sub>Ix</sub>	1, 2, 3
I <sub>OZ</sub>	1, 2, 3
I <sub>CC</sub>	1, 2, 3
I <sub>SB1</sub>	1, 2, 3
I <sub>SB2</sub>	1, 2, 3

#### Switching Characteristics

Parameter	Subgroups
<b>READ CYCLE</b>	
t <sub>RC</sub>	7, 8, 9, 10, 11
t <sub>AA</sub>	7, 8, 9, 10, 11
t <sub>OHA</sub>	7, 8, 9, 10, 11
t <sub>ACE</sub>	7, 8, 9, 10, 11
<b>WRITE CYCLE</b>	
t <sub>WC</sub>	7, 8, 9, 10, 11
t <sub>SCE</sub>	7, 8, 9, 10, 11
t <sub>AW</sub>	7, 8, 9, 10, 11
t <sub>HA</sub>	7, 8, 9, 10, 11
t <sub>SA</sub>	7, 8, 9, 10, 11
t <sub>PWE</sub>	7, 8, 9, 10, 11
t <sub>SD</sub>	7, 8, 9, 10, 11
t <sub>HD</sub>	7, 8, 9, 10, 11
t <sub>DWE</sub> <sup>[16]</sup>	7, 8, 9, 10, 11
t <sub>ADV</sub> <sup>[16]</sup>	7, 8, 9, 10, 11

**Note:**

16. 7C101A only.

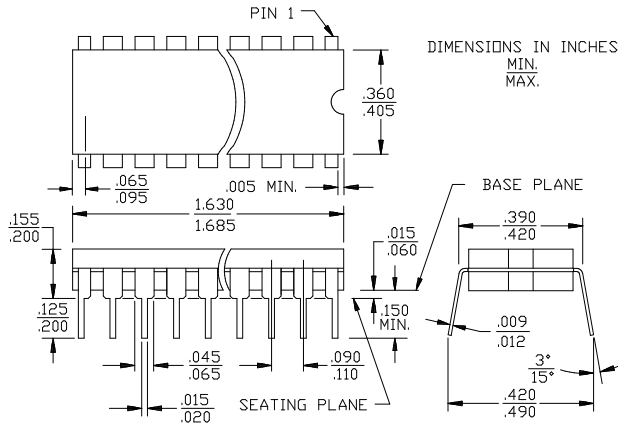
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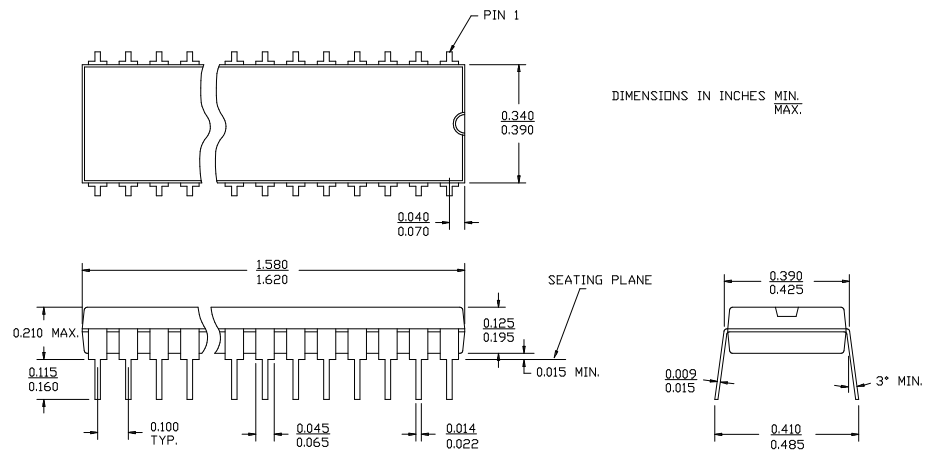


## Package Diagrams

### 32-Lead (400-Mil) CerDIP D44



### 32-Lead (400-Mil) Molded DIP P43

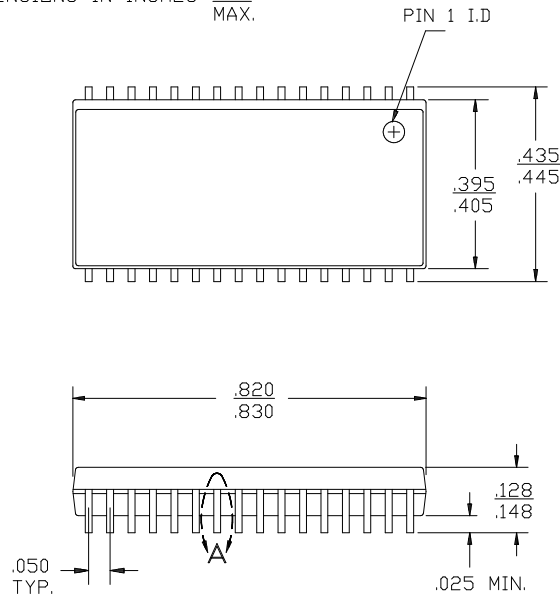




**Package Diagrams (continued)**

**32-Lead (400-Mil) Molded SOJ V33**

DIMENSIONS IN INCHES MIN.  
MAX.



DETAIL A  
EXTERNAL LEAD DESIGN

