7c1021: March 31, 1995
Revised: June 25, 1996

ADVANCED INFORMATION

CY7C1021

64K x 16 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 1020 mW**
- **Available in 450 x 550-mil LCC**
- **Automatic power-down when deselected**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options**

Functional Description

The CY7C1021 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

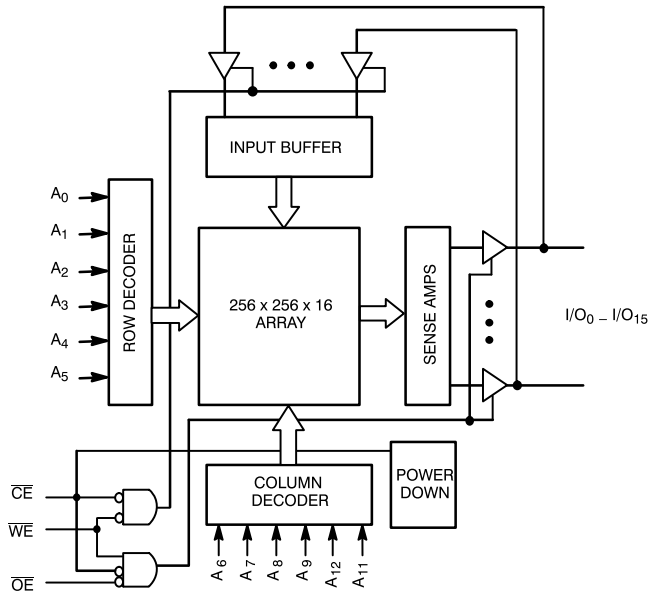
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and byte write enable ($\overline{BHE}$/$\overline{LBE}$) inputs LOW. Data on the appropiate eight I/O pins (I/O_0 through I/O_7 and/or I/O_8 through I/O_{15}) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing the write enables ($\overline{BHE}$ and/or $\overline{BLE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the appropiate I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1021 is available in standard 400-mil-wide DIPs and SOJs.

Logic Block Diagram



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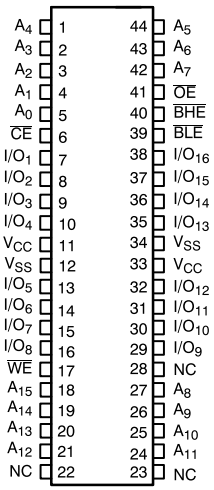
Pin Configurations

DIP/SOJ
Top View



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Selection Guide

		7C1021–12	7C1021–15	7C1021–20
Maximum Access Time (ns)		12	15	20
Maximum Operating Current (mA)	Commercial	195	180	165
	Military		195	180

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