CY7C123

256 x 4 Static RAM

Features

- **256 x 4 static RAM for control store in high-speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 7 ns (commercial)**
  - **— 10 ns (military)**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 825 mW (military)**
- **Separate inputs and outputs**
- **5-volt power supply ±10% tolerance both commercial and military**
- **TTL-compatible inputs and outputs**
- **24 pins**
- **300-mil package**

Functional Description

The CY7C123 is a high-performance CMOS static RAM organized as 256 words by 4 bits. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS}_1$) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

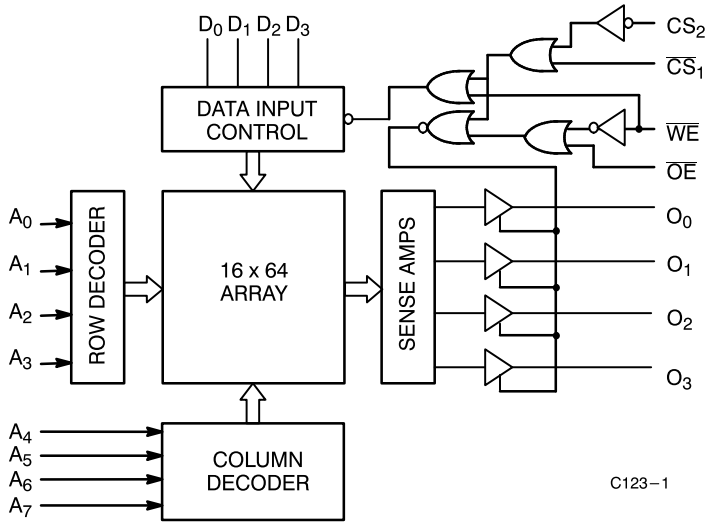
Writing to the device is accomplished when the chip select one ($\overline{CS}_1$) and write enable ($\overline{WE}$) inputs are both LOW and the chip select two input is HIGH. Data on the four data inputs (D_0 through D_3) is written into the memory location specified on the address pins (A_0 through A_7). The outputs are preconditioned so that the write data is present at the outputs when the write cycle is complete. This precondition operation ensures minimum write recovery times by eliminating the "write recovery glitch."

Reading the device is accomplished by taking the chip select one ($\overline{CS}_1$) and output enable ($\overline{OE}$) inputs LOW, while the write enable ($\overline{WE}$) and chip select two ($\overline{CS}_2$) inputs remain HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins (O_0 through O_3).

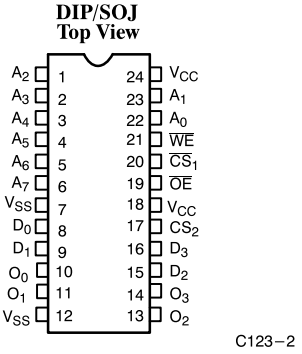
The output pins remain in high-impedance state when chip select one ($\overline{CS}_1$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) or chip select two ($\overline{CS}_2$) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C123–7	7C123–9	7C123–10	7C123–12	7C123–15
Maximum Access Time (ns)	Commercial	7	9		12	
	Military			10	12	15
Maximum Operating Current (mA)	Commercial	120	120		120	
	Military			150	150	150

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pins 24 and 18 to Pins 7 and 12)[1] ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to +7.0V

DC Input Voltage[1] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[2]	−55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C123−7 7C123−9 Min.	7C123−7 7C123−9 Max.	7C123−10 7C123−15 Min.	7C123−10 7C123−15 Max.	7C123−12 Min.	7C123−12 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −5.2 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			−0.8	+0.8	−0.8	+0.8	−0.8	+0.8	V
I_{IX}	Input Load Current	$V_{SS} \le V_I \le V_{CC}$		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Current (High Z)	$V_{SS} \le V_{OUT} \le V_{CC}$, Output Disabled		−10	+10	−10	+10	−10	+10	µA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = $f_{MAX} = 1/t_{RC}$	Commercial		120				120	mA
			Military				150		150	mA

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

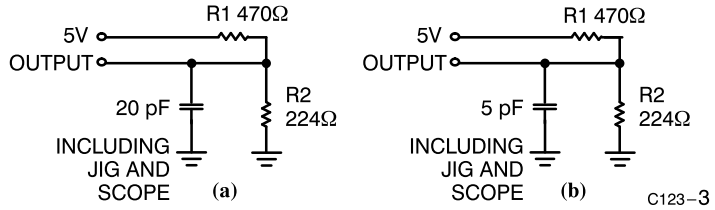
Logic Table[5]

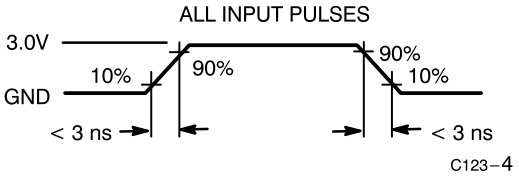
Input					Outputs	Mode
$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	$D_0 - D_3$		
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
L	L	H	H	X	$O_0 - O_3$	Read Stored Data
X	L	H	L	L	High Z	Write “0”
X	L	H	L	H	High Z	Write “1”
H	L	H	H	X	High Z	Output Disabled

Notes:

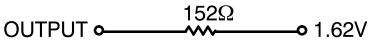
1. V_{IL}(min.) = −3.0V for pulse durations of less than 20 ns.
2. T_A is the “instant on” case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Tested initially and after any design or process changes that may affect these parameters.
5. H = High Voltage, L = Low Voltage, X = Don’t Care, and High Z = High Impedance.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

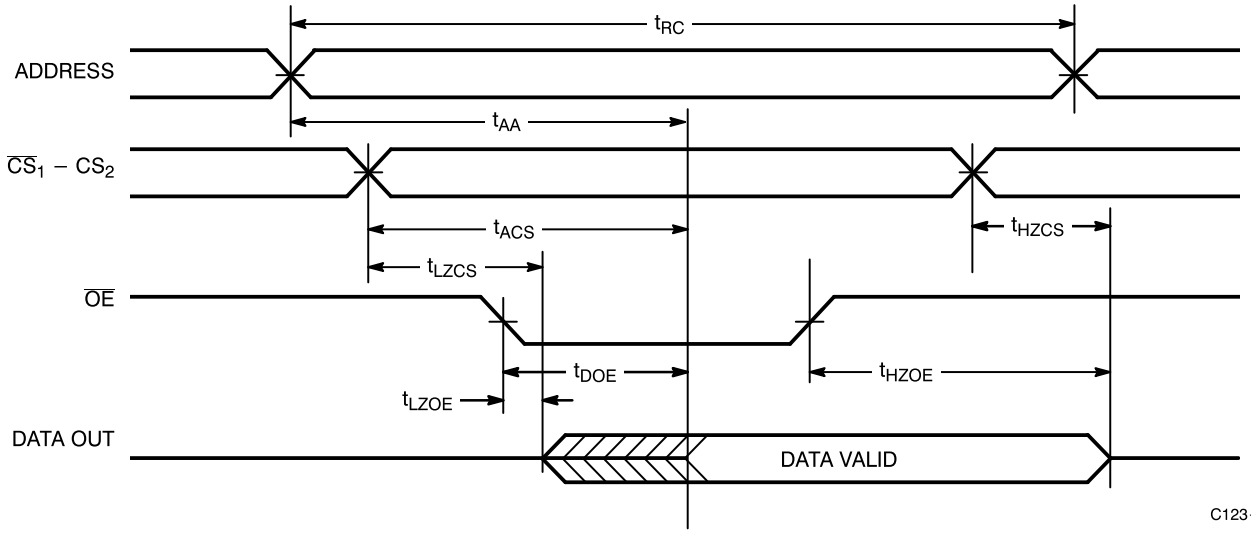
Parameter	Description	7C123–7		7C123–9		7C123–10		7C123–12		7C123–15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	7		9		10		12		15		ns
t_{AA}	Address to Data Valid		7		9		10		12		15	ns
t_{ACS}	Chip Select to Data Valid		7		8		8		8		10	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		8		8		8		10	ns
t_{HZCS}	Chip Select to High Z[6, 7]		5		6		6		6.5		8	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		5		6		6		6.5		8	ns
t_{LZCS}	Chip Select to Low Z[7]	2		2		2		2		2		ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		2		2		2		ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	7		9		10		12		15		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		5.5		6		6		7		8	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	2		2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	5		6.5		7		8		11		ns
t_{SD}	Data Set-Up to Write End	5		6		7		8		11		ns
t_{HD}	Data Hold from Write End	1		1		1		1		1		ns
t_{SA}	Address Set-Up to Write Start	0.5		1		1		2		2		ns
t_{HA}	Address Hold from Write End	1.5		1.5		2		2		2		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	5		6.5		7		8		11		ns
t_{AW}	Address Set-Up to Write End	5.5		7.5		8		10		13		ns

Notes:

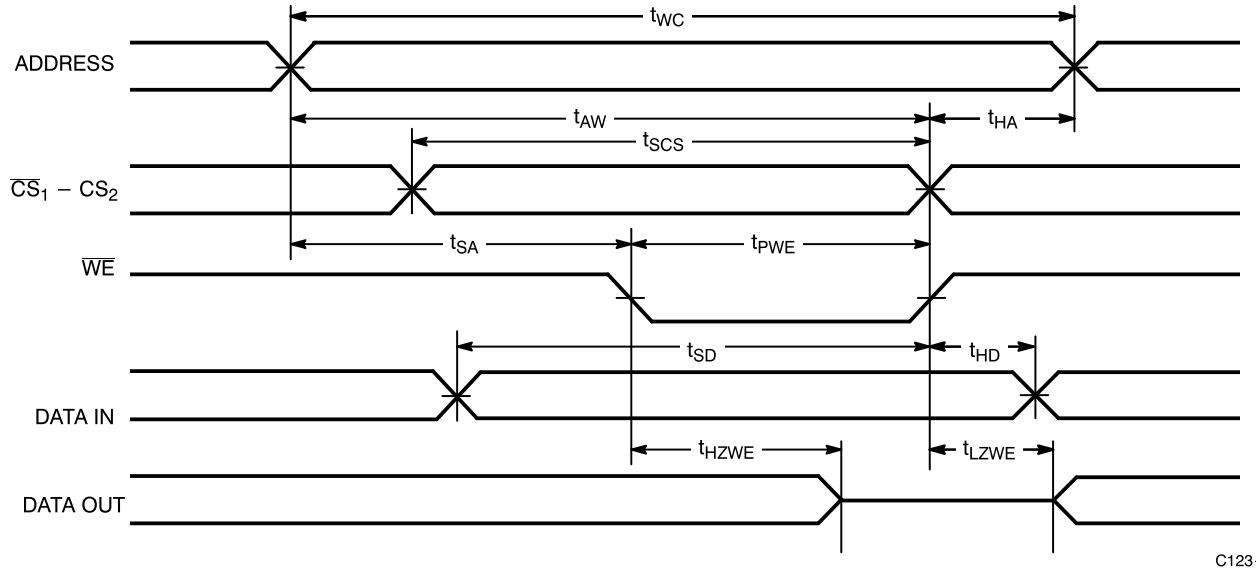
6. Transition is measured at steady-state HIGH level − 500 mV or steady-state LOW level +500 mV on the output from 1.5V level on the input with load shown in part (b) of AC Test Loads.
7. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.

Switching Waveforms

Read Cycle [8, 9]



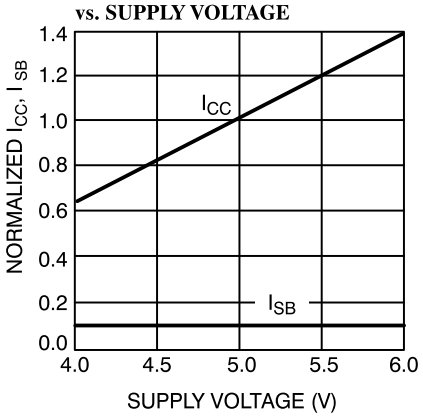
Write Cycle [8, 9]



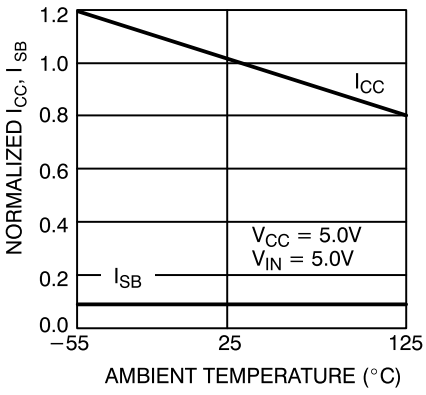
Notes:
8. Measurements are referenced to 1.5V unless otherwise stated.
9. Timing diagram represents one solution that results in an optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.

Typical DC and AC Characteristics

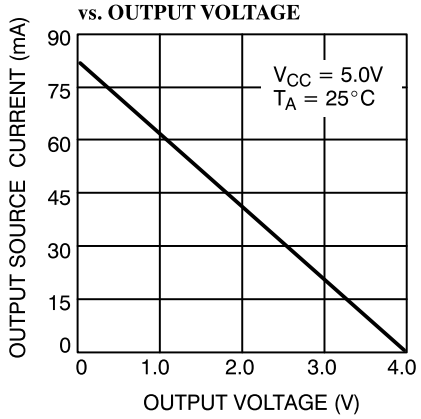
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



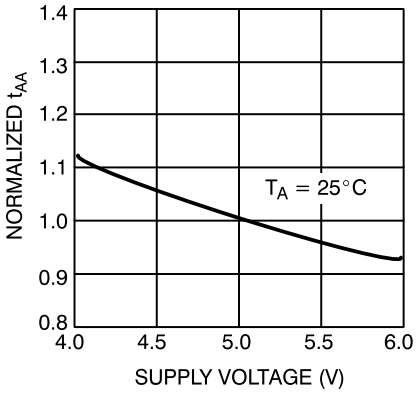
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



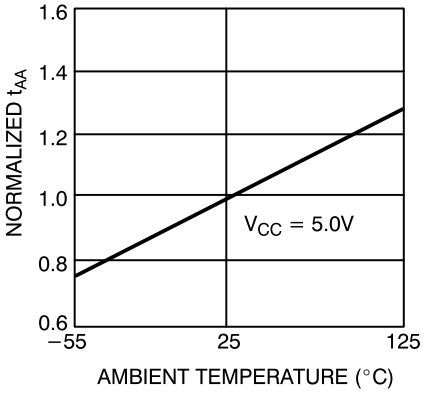
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



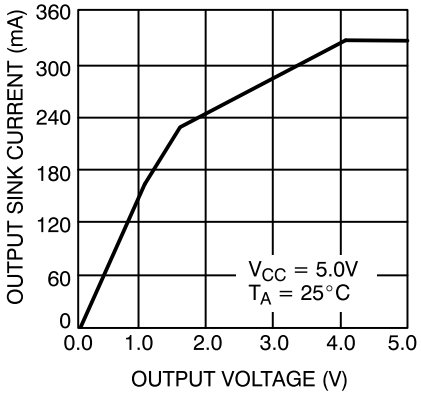
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



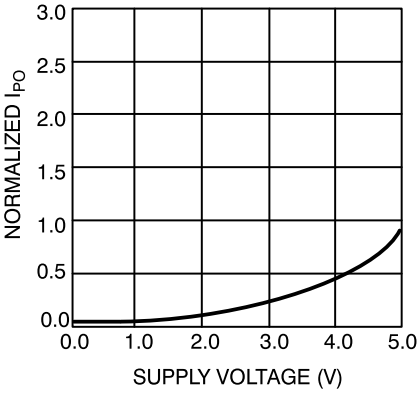
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



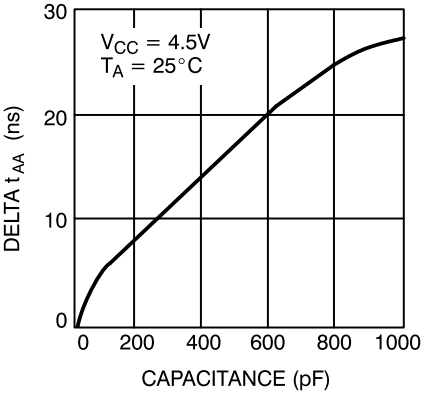
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



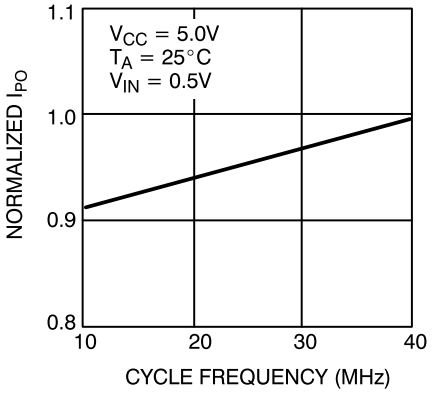
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TOTAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C123−7PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C123−7VC	V13	24-Lead Molded SOJ	
9	CY7C123−9PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C123−9VC	V13	24-Lead Molded SOJ	
10	CY7C123−10DMB	D14	24-Lead (300-Mil) CerDIP	Military
12	CY7C123−12PC	P13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C123−12DMB	D14	24-Lead (300-Mil) CerDIP	Military
15	CY7C123−15DMB	D14	24-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SCS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11

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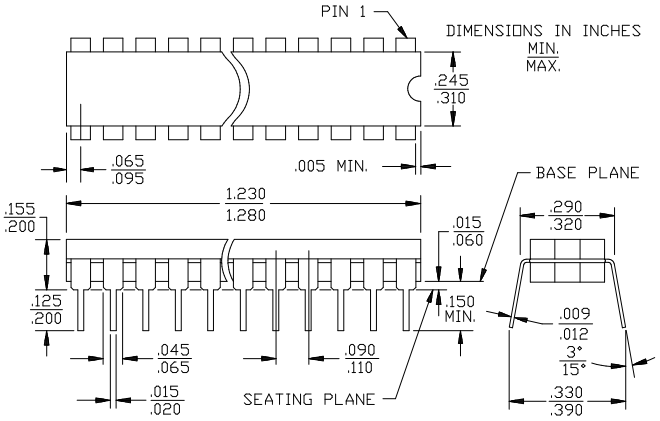
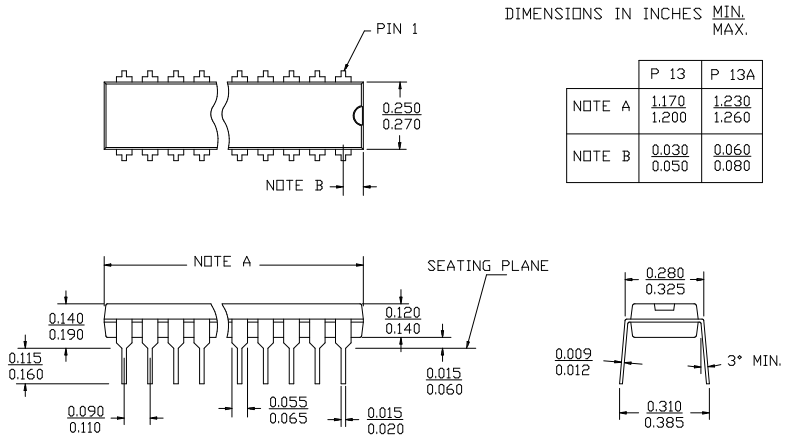
Package Diagrams

24-Lead (300-Mil) CerDIP D14
MIL−STD−1835 D−9 Config. A



24-Lead (300-Mil) Molded DIP P13/P13A



	P 13	P 13A
NOTE A	1.170 / 1.200	1.230 / 1.260
NOTE B	0.030 / 0.050	0.060 / 0.080

Package Diagrams (continued)

24-Lead Molded SOJ V13