ADVANCED INFORMATION

CY7C1335
CY7C1336

32K x 32 Synchronous Cache RAM

Features

- **Supports 75-MHz Pentium™ and PowerPC™ operations with zero wait states**
- **Fully registers inputs and outputs for pipelined operation**
- **32K x 32 common I/O architecture**
- **Single 3.3V power supply**
- **Fast Clock-to-output times**
  - **— 7.0 ns with 0 pF (for 75-MHz systems)**
  - **— 8.5 ns with 0 pF (for 66-MHz systems)**
  - **— 10 ns with 0 pF (for 60-MHz systems)**
- **Burst counter supporting Intel Pentium processor (7C1335)**
- **Burst counter supporting PowerPC (7C1336)**
- **Separate processor and controller address strobes**
- **Synchronous self-timed writes**
- **Asynchronous output enable**
- **JEDEC-standard 100 TQFP pinout**

Functional Description

The CY7C1335 and CY7C1336 are 3.3V 32K by 32 synchronous cache SRAMs designed to support zero wait state secondary cache with minimal glue logic.

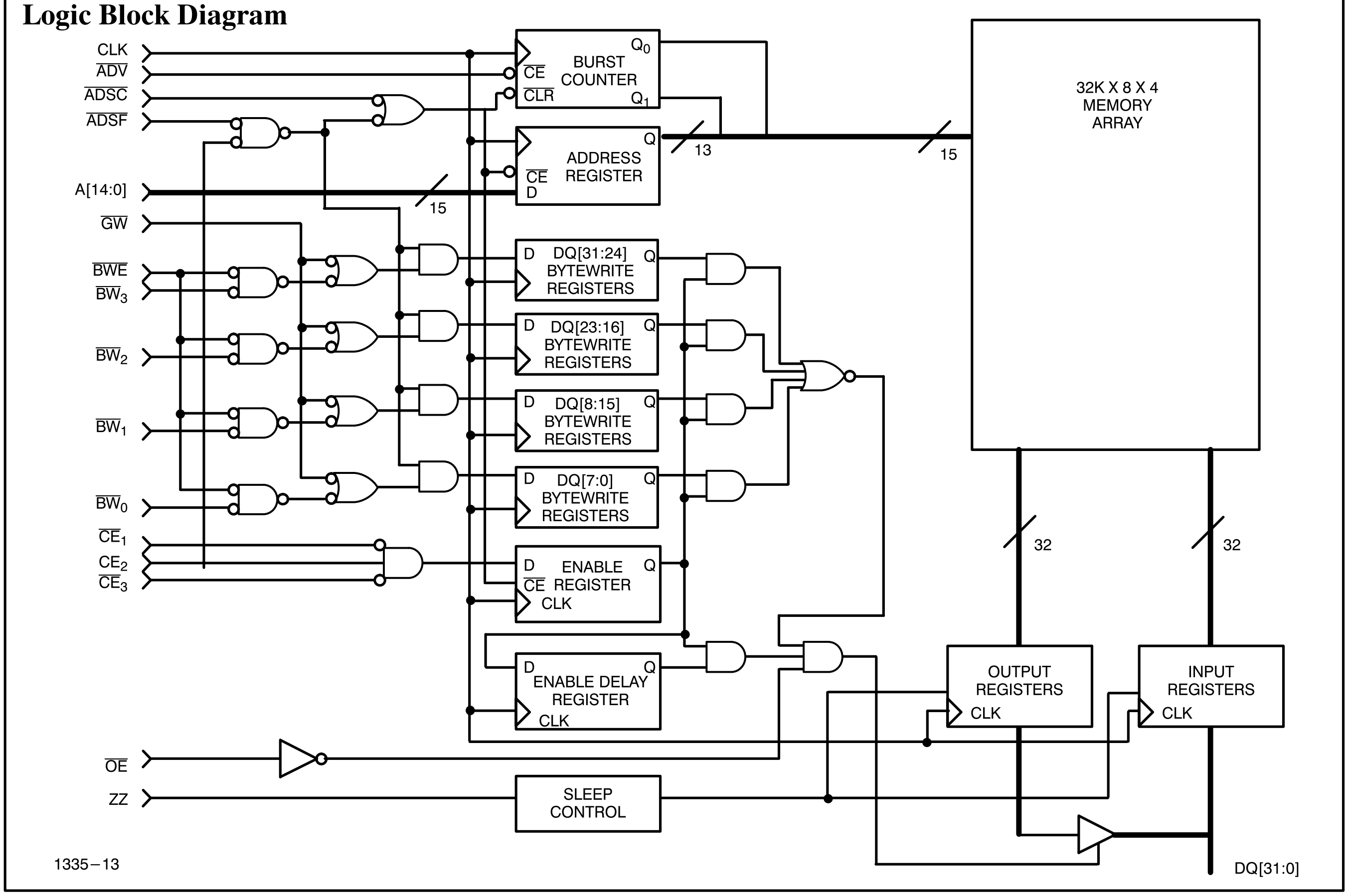
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise is 7.0 ns (0 pF load). A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

The CY7C1335 supports secondary cache in systems utilizing Pentium possessors. Its counter follows the burst sequence of the Pentium processor. The CY7C1336 is designed for processors that utilize a linear burst sequence, such as the PowerPC. Accesses can be initiated with either the processor address strobe ($\overline{ADSP}$) of the controller address strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input.

Byte write operations are qualified with the four Byte Write Select ($\overline{BW}_{0\text{-}3}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and write data to all four bytes. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous chip selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output three-state control. In order to provide proper data during depth expansion, $\overline{OE}$ is masking during the first clock of a read cycle.

Logic Block Diagram



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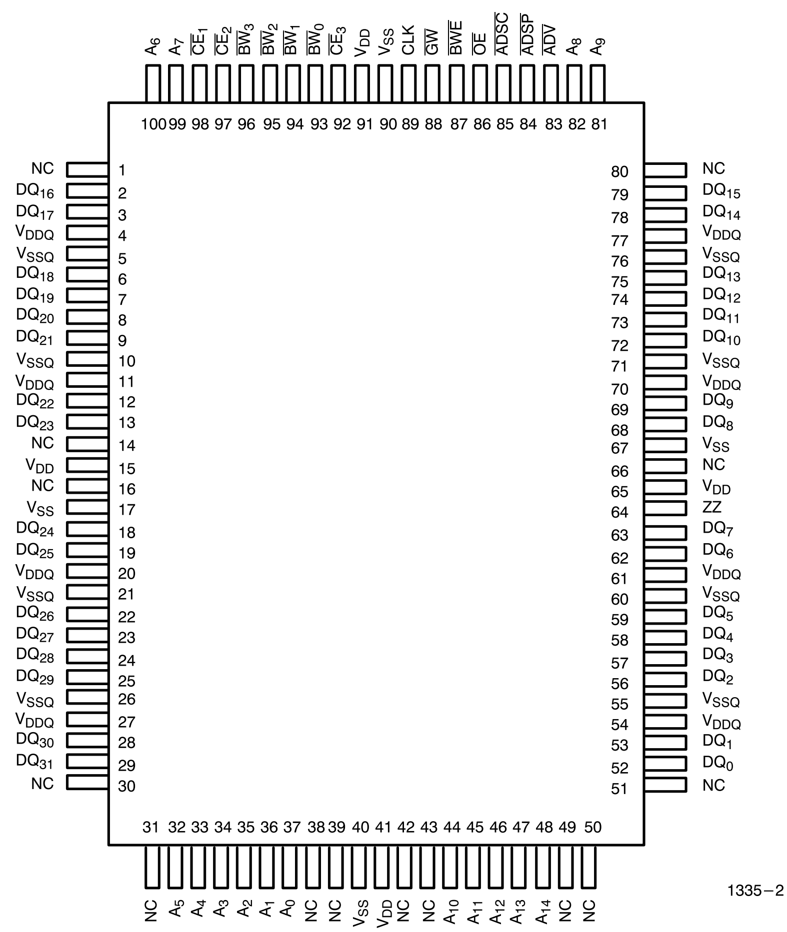
Pin Configuration



Selection Guide

		7C1335−7 7C1336−7	7C1335−8 7C1336−8	7C1335−10 7C1336−10
Maximum Access Time (ns) (0-pF load)		7.0	8.5	10
Maximum Operating Current (mA)	Commercial	180	170	160

Pin Definitions

Pin Number	Name	I/O	Description
32−37, 44−48, 81, 82, 99, 100	A[14:0]	Input-Synchronous	Address Inputs used to select one of the 32K address locations. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW.
93−96	BW[3:0]	Input-Synchronous	Byte Write Select Inputs, active LOW. Qualified with $\overline{BW}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
88	$\overline{GW}$	Input-Synchronous	Global Write Enable Input, active LOW. When asserted LOW on the rising edge of CLK, a global write is conducted. (ALL bytes are written, regardless of the values on $\overline{BW}$[3:0].)
87	$\overline{BWE}$	Input-Synchronous	Byte Write Enable Input, active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
89	CLK	Input-Clock	Clock input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
98	$\overline{CE}_1$	Input-Synchronous	Chip Select 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device. Also used to gate $\overline{ADSP}$.
97	CE_2	Input-Synchronous	Chip Select 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device. Also used to gate $\overline{ADSP}$.
92	$\overline{CE}_3$	Input-Synchronous	Chip Select 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
86	$\overline{OE}$	Input-Synchronous	Output Enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked (deasserted) during the first clock of a read cycle.
83	$\overline{ADV}$	Input-Synchronous	Advance Input signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
84	$\overline{ADSP}$	Input-Synchronous	Address Strobe from Processor, sampled on the rising edge of CLK. When asserted LOW, A[0−14] is captured in the address registers. A_0 and A_1 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
85	$\overline{ADSC}$	Input-Synchronous	Address Strobe from Controller, sampled on the rising edge of CLK. When asserted LOW, A[0−14] is captured in the address registers. A_0 and A_1 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
64	ZZ	Input-Synchronous	ZZ "sleep" Input. When ZZ is implemented, places the device in a non-time critical "sleep" condition with data integrity preserved.
29, 28, 25−22, 19, 18, 13, 12, 9−6, 3, 2, 79, 78, 75−72, 69, 68, 63, 62 59−56, 53, 52	DQ[31:0]	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A[14:0] during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ[31:0] are placed in a three-state condition.
15,41,65, 91	V_{DD}	Power Supply	Power supply inputs to the core of the device. Should be connected to 3.3V power supply.
17,40,67, 91	V_{SS}	Ground	Ground for the core of the device. Should be connected to ground of the system.
4, 11, 20, 27, 54,61,70, 77	V_{DDQ}	I/O Power Supply	Power supply for the I/O circuitry. Should be connected to a 3.3V power supply.
5, 10, 21, 26, 55,60,71, 76	V_{SSQ}	I/O Ground	Ground for the I/O circuitry. Should be connected to ground of the system.

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