



CY7C185

8K x 8 Static RAM

Features

- **High speed**
— 15 ns
- **Fast t_{DOE}**
- **Low active power**
— 715 mW
- **Low standby power**
— 220 mW
- **CMOS for optimum speed/power**
- **Easy memory expansion with \overline{CE}_1 , CE_2 and OE features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

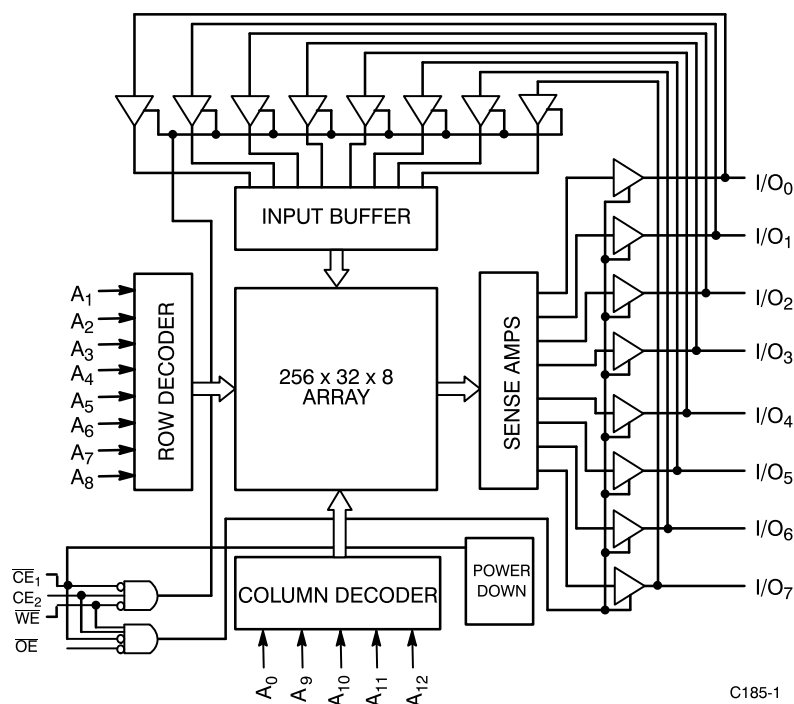
The CY7C185 is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}_1), an active HIGH chip enable (CE_2), and active LOW output enable (OE) and three-state drivers. This device has an automatic power-down feature (\overline{CE}_1), reducing the power consumption by 70% when deselected. The CY7C185 is in a standard 300-mil-wide DIP and SOJ package.

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE}_1 and \overline{WE} inputs are both LOW and CE_2 is HIGH, data on

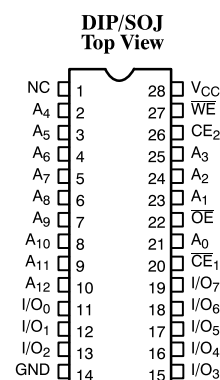
the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE}_1 and OE active LOW, CE_2 active HIGH, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH. A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



C185-2

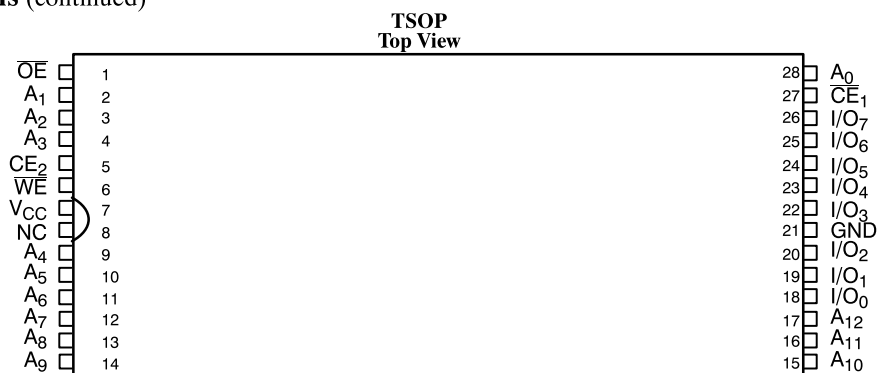
Selection Guide^[1]

	7C185-12	7C185-15	7C185-20	7C185-25	7C185-35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	140	130	110	100	100
Maximum Standby Current (mA)	40/15	40/15	20/15	20/15	20/15

Shaded areas contain preliminary information.

Note:

1. For military specifications, see the CY7C185A/CY7C186A datasheet.

Pin Configurations (continued)


C185-3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State^[2] -0.5V to +7.0V

DC Input Voltage^[2] -0.5V to +7.0V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C185-12		7C185-15		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		140		130	mA
I _{SB1}	Automatic $\overline{CE_1}$ Power-Down Current	Max. V _{CC} , $\overline{CE_1} \geq V_{IH}$, Min. Duty Cycle = 100%		40		40	mA
I _{SB2}	Automatic $\overline{CE_1}$ Power-Down Current	Max. V _{CC} , $\overline{CE_1} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		15		15	mA

Shaded areas contain preliminary information.

Notes:

- Minimum voltage is equal to -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range (continued)

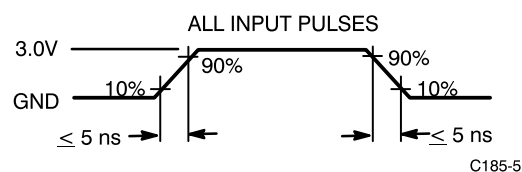
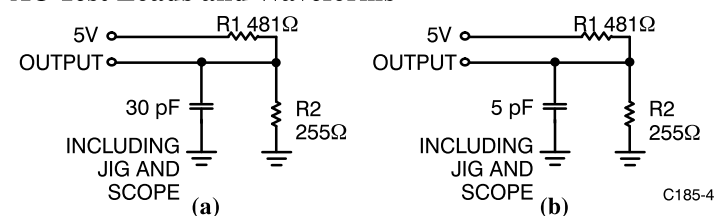
Parameter	Description	Test Conditions	7C185–20		7C185–25, 35		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = –4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		–0.5	0.8	–0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	–5	+5	–5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	–5	+5	–5	+5	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		–300		–300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		110		100	mA
I _{SB1}	Automatic \overline{CE}_1 Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{IH}$, Min. Duty Cycle = 100%		20		20	mA
I _{SB2}	Automatic \overline{CE}_1 Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} – 0.3V or V _{IN} ≤ 0.3V		15		15	mA

Capacitance^[4]

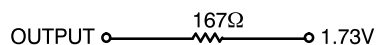
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 5.0V	7	pF
C _{OUT}	Output Capacitance		7	pF

Notes:

4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range^[5]

Parameter	Description	7C185–12		7C185–15		7C185–20		7C185–25		7C185–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	12		15		20		25		35		ns
t _{AA}	Address to Data Valid		12		15		20		25		35	ns
t _{OHA}	Data Hold from Address Change	3		3		5		5		5		ns
t _{ACE1}	\overline{CE}_1 LOW to Data Valid		12		15		20		25		35	ns
t _{ACE2}	CE ₂ HIGH to Data Valid		12		15		20		25		35	ns
t _{DOE}	\overline{OE} LOW to Data Valid		6		8		9		12		15	ns
t _{LZOE}	\overline{OE} LOW to Low Z	2		3		3		3		3		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[6]		6		7		8		10		10	ns
t _{LZCE1}	\overline{CE}_1 LOW to Low Z ^[7]	3		3		5		5		5		ns
t _{LZCE2}	CE ₂ HIGH to Low Z	3		3		3		3		3		ns
t _{HZCE}	\overline{CE}_1 HIGH to High Z ^[6, 7] CE ₂ LOW to High Z		6		7		8		10		10	ns
t _{PU}	\overline{CE}_1 LOW to Power-Up	0		0		0		0		0		ns
t _{PD}	\overline{CE}_1 HIGH to Power-Down		12		15		20		20		20	ns
WRITE CYCLE ^[8]												
t _{WC}	Write Cycle Time	12		15		20		25		35		ns
t _{SCE1}	\overline{CE}_1 LOW to Write End	8		12		15		20		20		ns
t _{SCE2}	CE ₂ HIGH to Write End	8		12		15		20		20		ns
t _{AW}	Address Set-Up to Write End	9		12		15		20		25		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	8		12		15		15		20		ns
t _{SD}	Data Set-Up to Write End	6		8		10		10		12		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6]		6		7		7		7		8	ns
t _{LZWE}	\overline{WE} HIGH to Low Z	3		3		5		5		5		ns

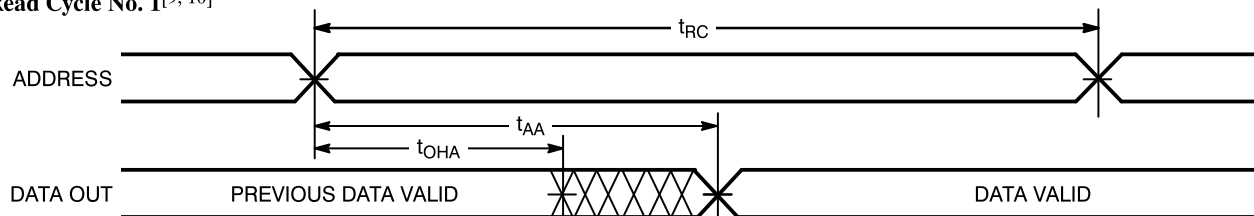
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Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, CE₂ HIGH, and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

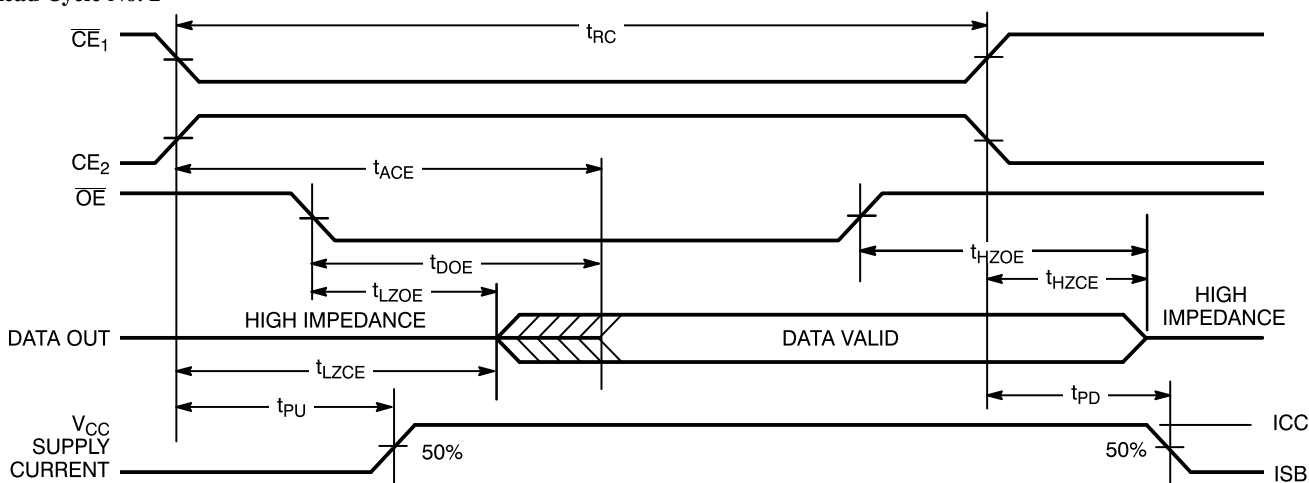
Switching Waveforms

Read Cycle No. 1^[9, 10]



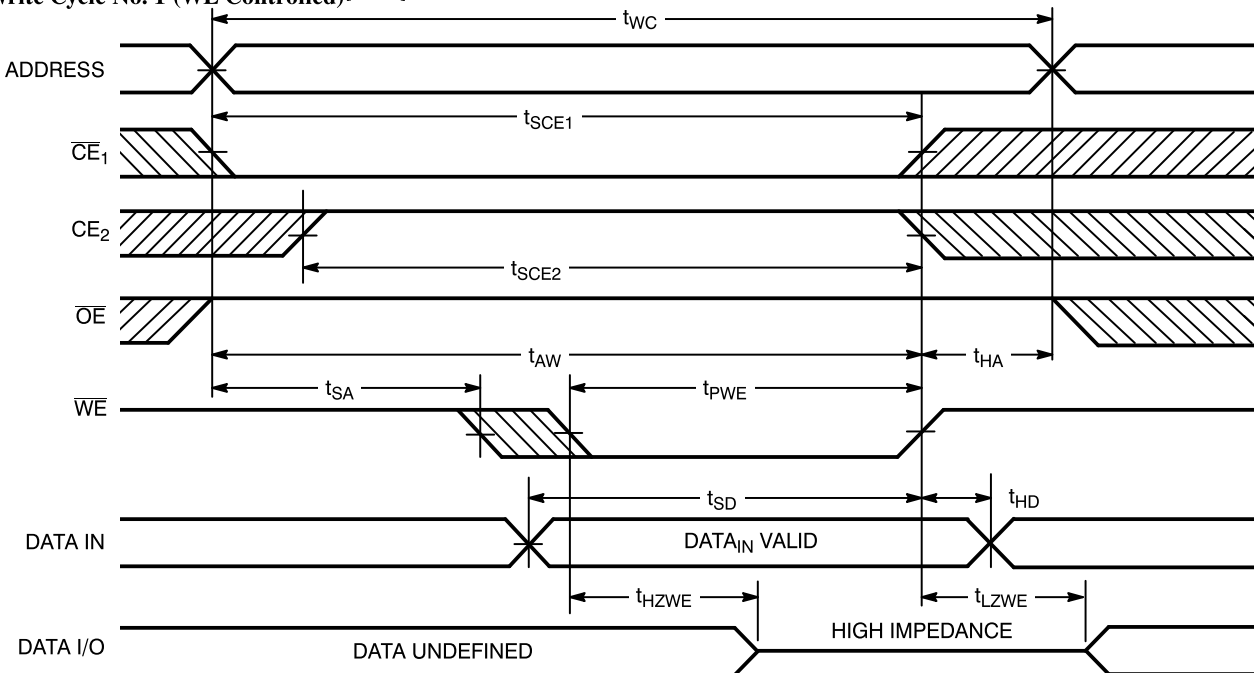
C185-6

Read Cycle No. 2^[11, 12]



C185-7

Write Cycle No. 1 (\overline{WE} Controlled)^[10, 12]



C185-8

Notes:

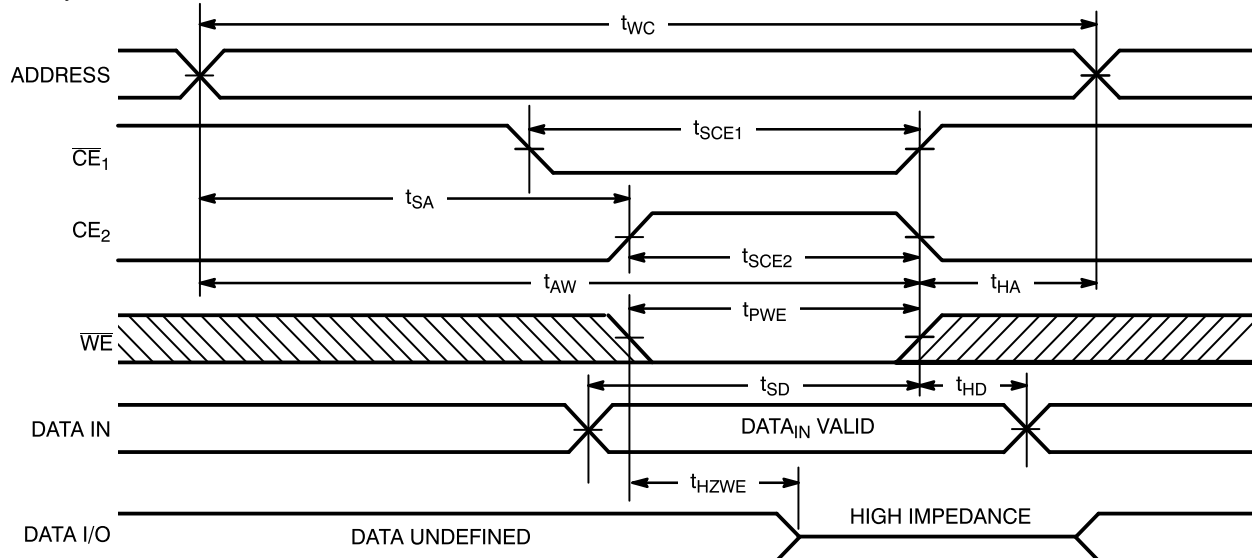
9. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$. $CE_2 = V_{IH}$.
 10. Address valid prior to or coincident with \overline{CE} transition LOW.

11. \overline{WE} is HIGH for read cycle.

12. Data I/O is High Z if $\overline{OE} = V_{IH}$, $\overline{CE}_1 = V_{IH}$, or $\overline{WE} = V_{IL}$.

Switching Waveforms (continued)

Write Cycle No. 2 (\overline{CE} Controlled) [10, 12, 13]



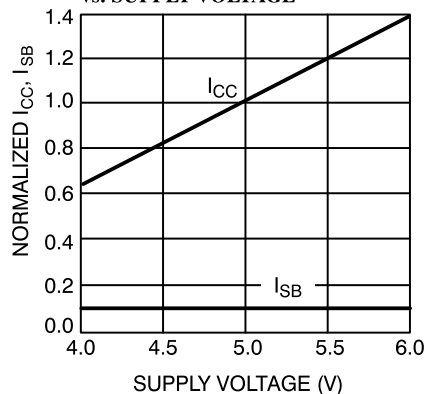
C185-9

Note:

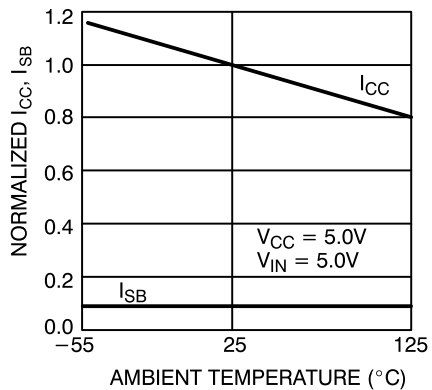
13. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics

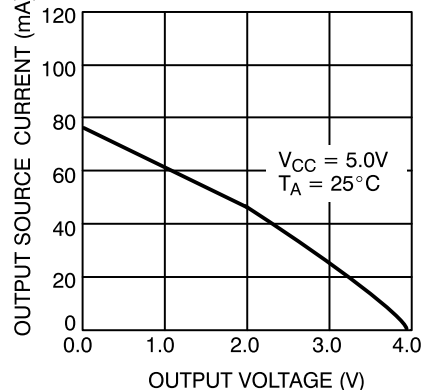
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



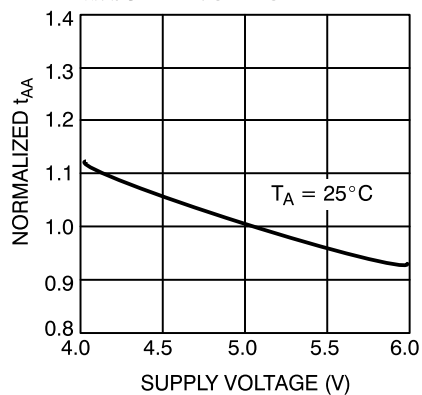
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



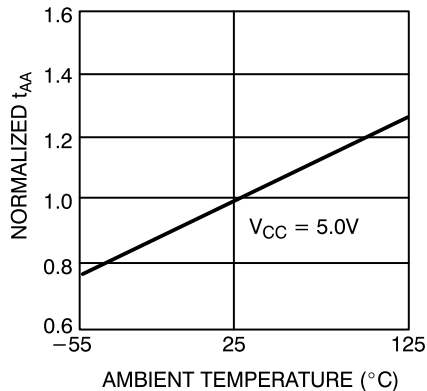
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



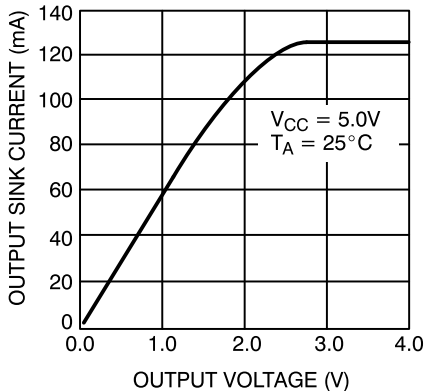
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

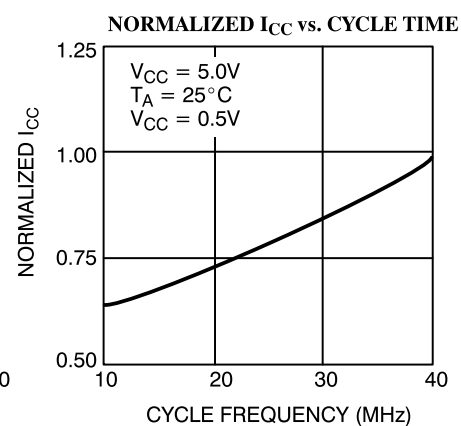
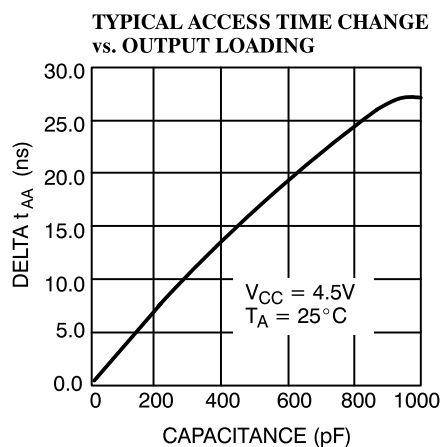
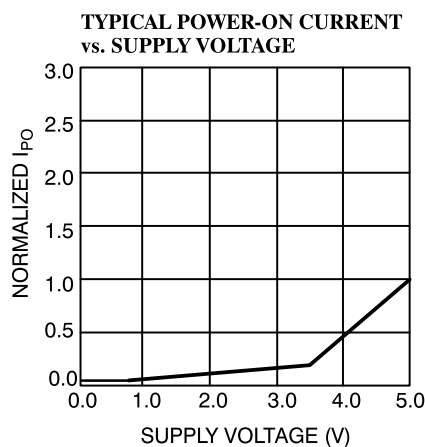


NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Typical DC and AC Characteristics (continued)

Truth Table

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

Ordering Information

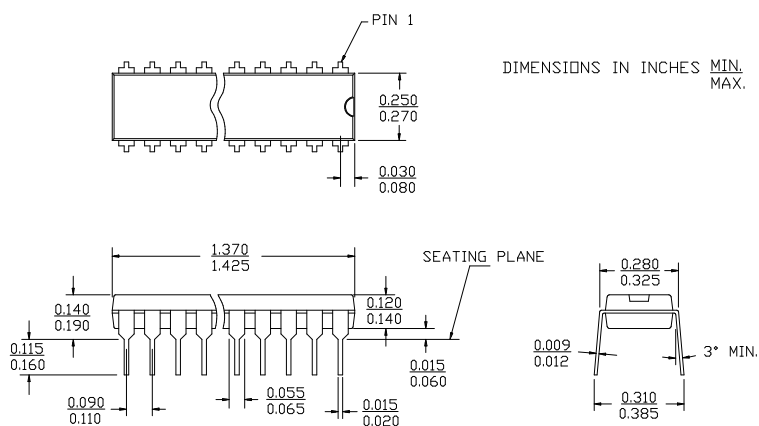
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C185-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185-12VC	V21	28-Lead Molded SOJ	
15	CY7C185-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185-15VC	V21	28-Lead Molded SOJ	
	CY7C185-15ZC	Z28	28-Lead Thin Small Outline Package	
20	CY7C185-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185-20VC	V21	28-Lead Molded SOJ	
	CY7C185-20ZC	Z28	28-Lead Thin Small Outline Package	
25	CY7C185-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185-25VC	V21	28-Lead Molded SOJ	
	CY7C185-25ZC	Z28	28-Lead Thin Small Outline Package	
35	CY7C185-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C185-35VC	V21	28-Lead Molded SOJ	
	CY7C185-35ZC	Z28	28-Lead Thin Small Outline Package	

Shaded areas contain preliminary information.

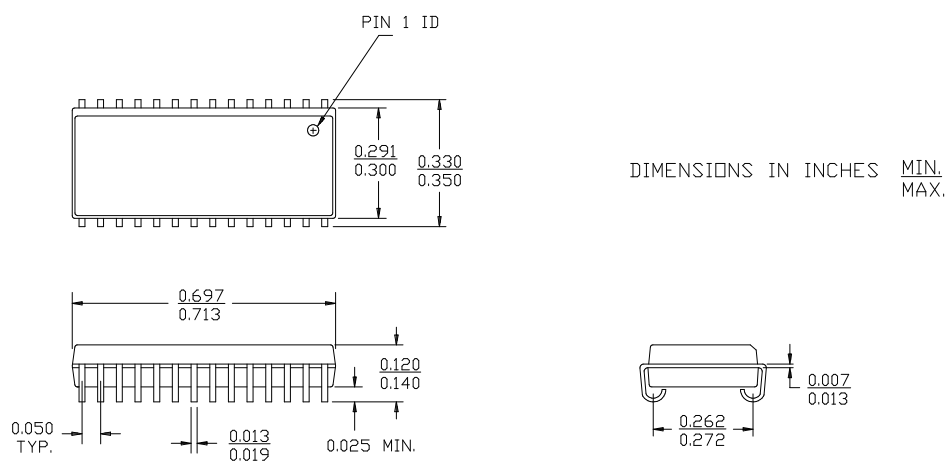
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Package Diagrams

28-Lead (300-Mil) Molded DIP P21



28-Lead Molded SOJ V21



Package Diagrams (continued)
28-Lead Thin Small Outline Package Z28
