CY7C187A

64K x 1 Static RAM

Features

- **High speed**
  - **— 20 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 495 mW**
- **Low standby power**
  - **— 220 mW**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C187A is a high-performance CMOS static RAM organized as 65,536 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C187A has an automatic power-down feature, reducing the power consumption by 55% when deselected.

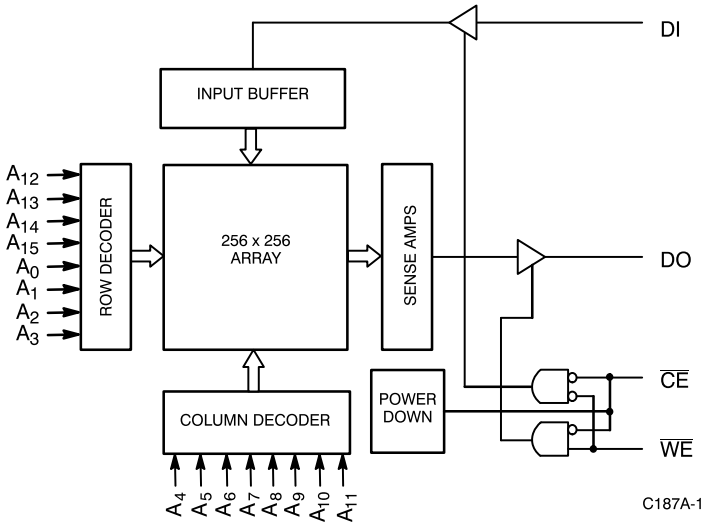
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

The 7C187A utilizes a die coat to insure alpha immunity.

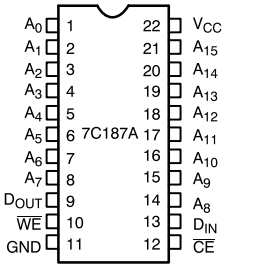
Logic Block Diagram



C187A-1

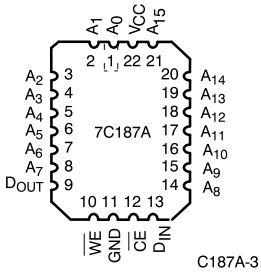
Pin Configurations

DIP
Top View



C187A-2

LCC
Top View



C187A-3

Selection Guide[1]

		7C187A−15	7C187A−20	7C187A−25	7C187A−35
Maximum Access Time (ns)		15	20	25	35
Maximum Operating Current (mA)	Military	160	90	80	80
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	30/20

Shaded area contains preliminary information.

Note:
1. For commercial specifications, see CY7C187 datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 11) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... −0.5V to +7.0V

DC Input Voltage[2] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Military[3]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C187A−15 Min.	7C187A−15 Max.	7C187A−20 Min.	7C187A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA	Mil		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Mil		160		90	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current[6]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Mil		40		40	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current[6]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Mil		20		20	mA

Shaded area contains preliminary information.

Notes:

2. V_{IL} (min.) = −3.0V for pulse durations less than 30 ns.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
6. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Electrical Characteristics Over the Operating Range[4] (continued)

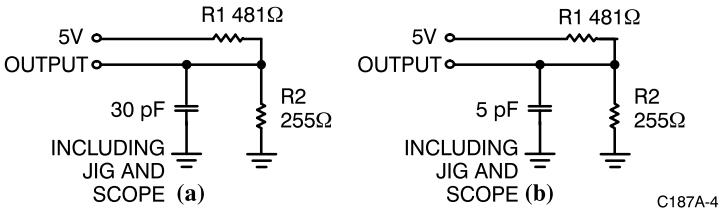
Parameter	Description	Test Conditions		7C187A−25 Min.	7C187A−25 Max.	7C187A−35 Min.	7C187A−35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Mil		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Mil		80		80	mA
I_{SB1}	Automatic $\overline{CE}$ Power−Down Current[6]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Mil		40		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current[6]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Mil		20		20	mA

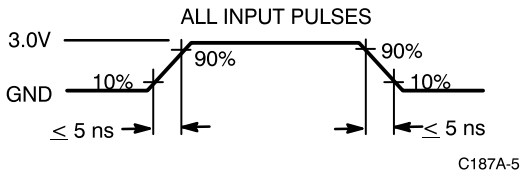
Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

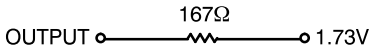
Note:
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4, 8]

Parameter	Description	7C187A−15		7C187A−20		7C187A−25		7C187A−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		20		25		35		ns
t_{AA}	Address to Data Valid		15		20		25		35	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		8		8		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20	ns
WRITE CYCLE[11]										
t_{WC}	Write Cycle Time	15		20		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		15		15		20		ns
t_{SD}	Data Set-Up to Write End	7		10		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 10]		7		7		7		10	ns

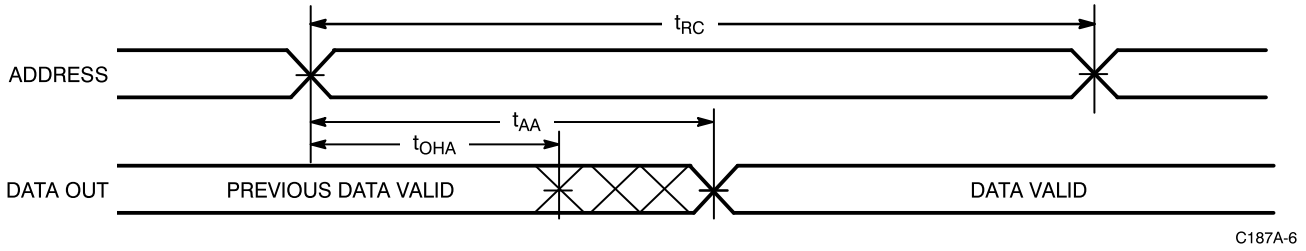
Shaded area contains preliminary information.

Notes:

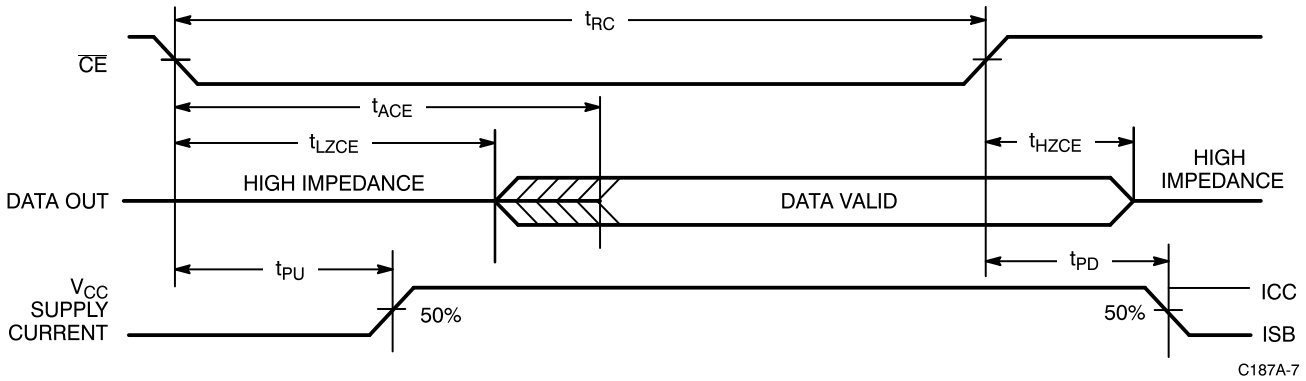
8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
10. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

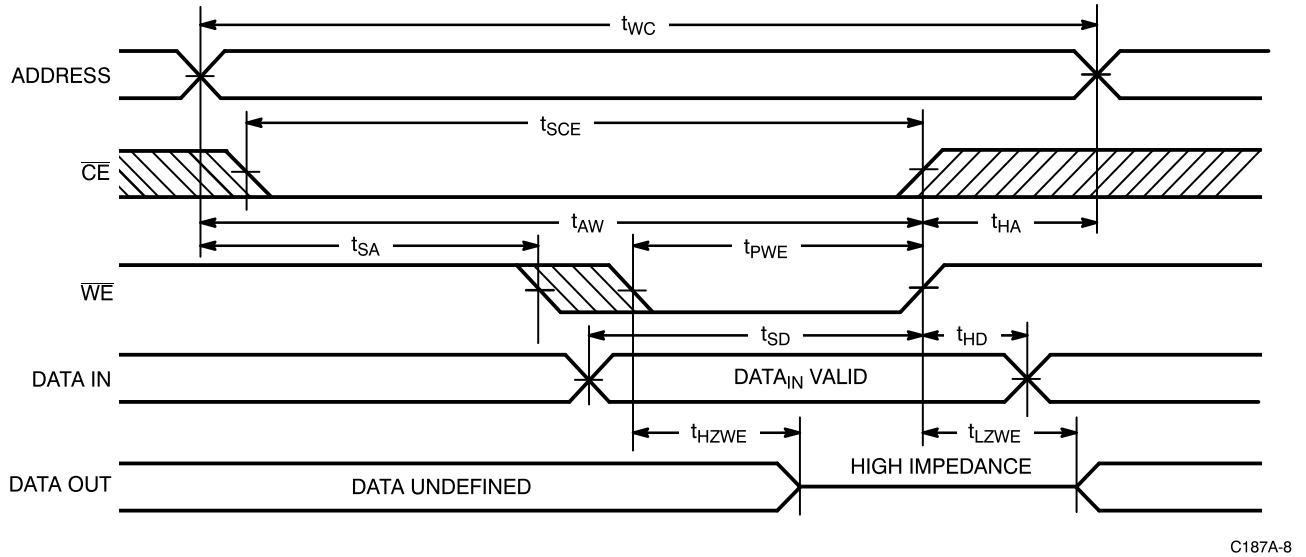
Read Cycle No. 1[12, 13]



Read Cycle No. 2[12, 14]



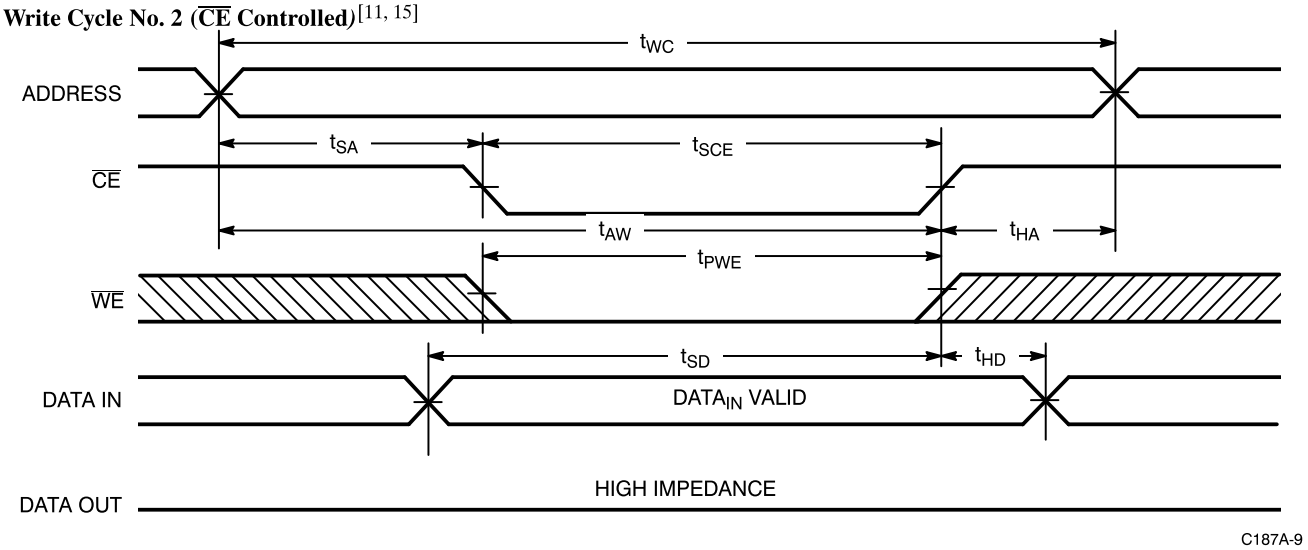
Write Cycle No. 1 ($\overline{WE}$ Controlled)[11]



Notes:
12. $\overline{WE}$ is HIGH for read cycle.
13. Device is continuously selected, $\overline{CE}$ = V_{IL}.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

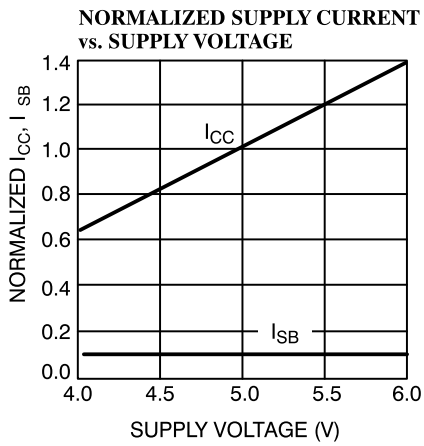
Switching Waveforms (continued)

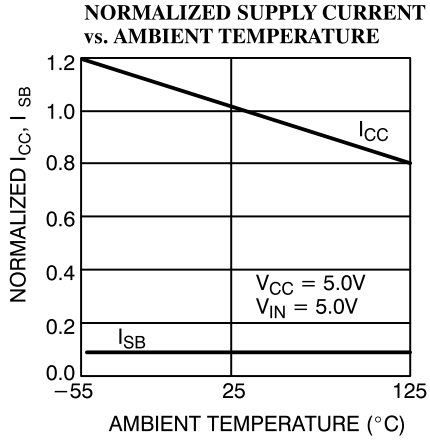
Write Cycle No. 2 ($\overline{CE}$ Controlled)[11, 15]

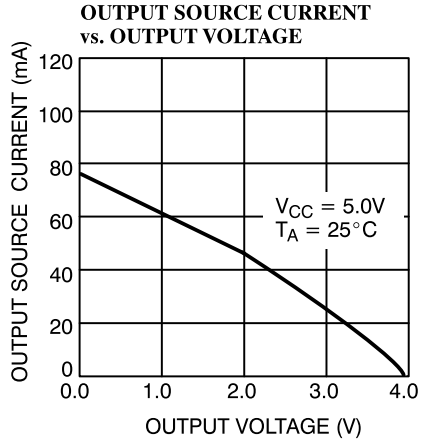


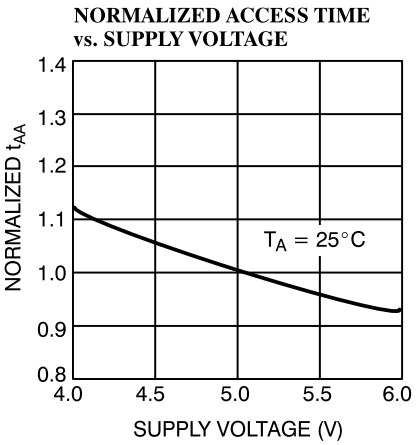
Note:
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

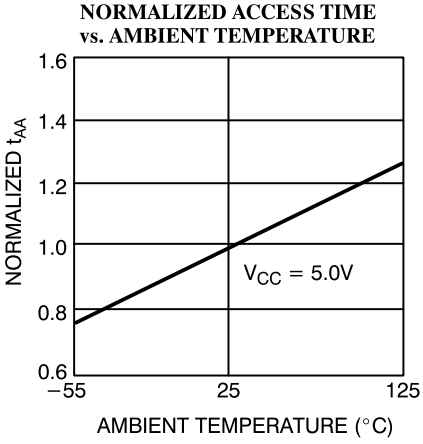
Typical DC and AC Characteristics

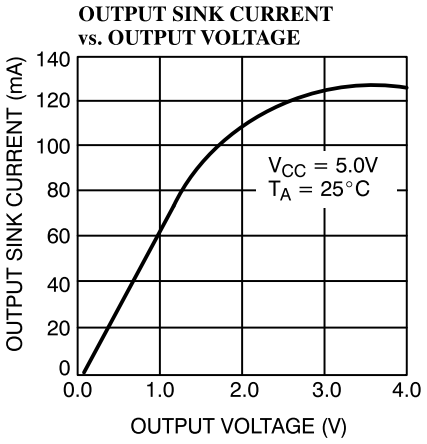






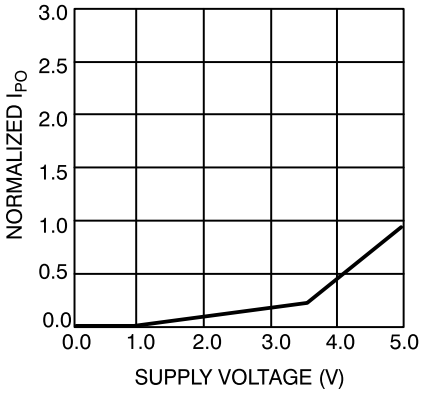




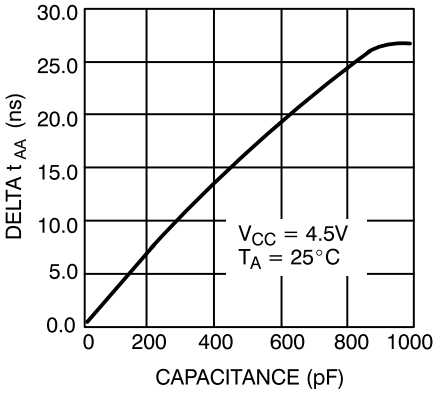


Typical DC and AC Characteristics (continued)

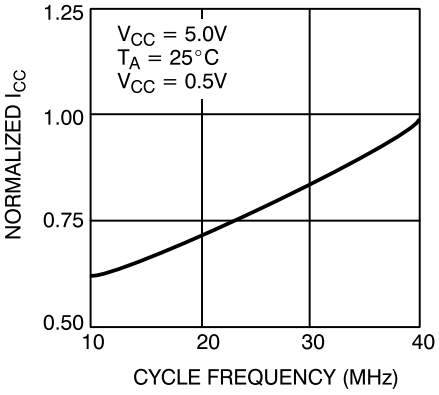
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Address Designators

Address Name	Address Function	Pin Number
A0	X3	1
A1	X4	2
A2	X5	3
A3	X6	4
A4	X7	5
A5	Y7	6
A6	Y6	7
A7	Y2	8
A8	Y3	14
A9	Y1	15
A10	Y0	16
A11	Y4	17
A12	Y5	18
A13	X0	19
A14	X1	20
A15	X2	21

Truth Table

$\overline{CE}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C187A−15DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C187A−15LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
20	CY7C187A−20DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C187A−20LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
25	CY7C187A−25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C187A−25LMB	L52	22-Pin Rectangular Leadless Chip Carrier	
35	CY7C187A−35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C187A−35LMB	L52	22-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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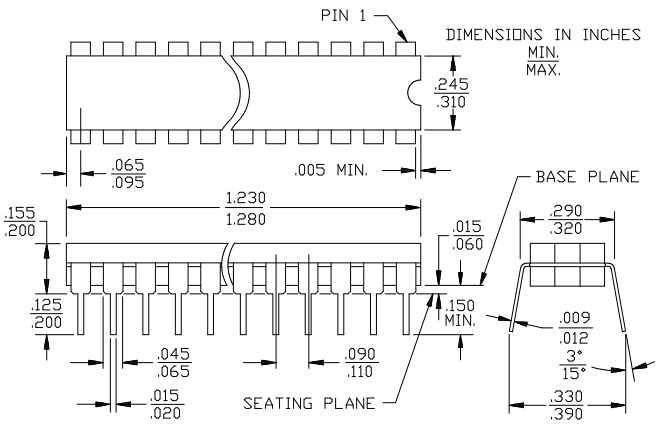
Package Diagrams

24-Lead (300-Mil) CerDIP D14
MIL−STD−1835 D−9 Config. A



22-Pin Rectangular Leadless Chip Carrier L52